

Data sheet acquired from Harris Semiconductor SCHS031B – Revised July 2003

CD4026B, CD4033B Types

CMOS **Decade Counters/Dividers**

High-Voltage Types (20-Volt Rating)

With Decoded 7-Segment Display Outputs and:

- Display Enable CD4026B
- Ripple Blanking CD4033B

CD4026B and CD4033B each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving one stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.

Inputs common to both types are CLOCK. RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026B include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the CD4033B are RIPPLE-BLANKING INPUT AND LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

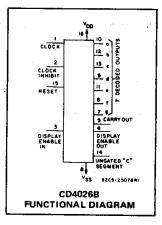
A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHI-BIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the JOHNSON counter. thus assuring proper counting sequence. The CARRY-OUT (Cout) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain. The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven

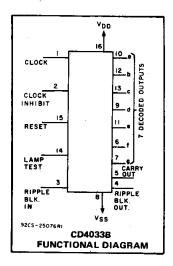
Features

- Counter and 7-segment decoding in one package
- Easily interfaced with 7-segment display types
- Fully static counter operation: DC to 6 MHz (typ.) at VDD=10 V
- Ideal for low-power displays
- Display enable output (CD4026B)
- "Ripple blanking" and lamp test (CD4033B)
- 100% tested for quiescent current at 20 V . ÷. Standardized, symmetrical output characteristics 3 1 1
- 5-V, 10-V, and 15-V parametric ratings
- Schmitt-triggered clock inputs
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices' **Applications**
- Decade counting 7-segment decimal display
- Frequency division 7-segment decimal displays
- Clocks, watches, timers (e.g. +60, + 60, + 12 counter/display)
- Counter/display driver for meter applications

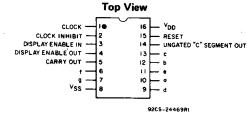
segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033B; in the CD4026B these outputs go high only when the DISPLAY ENABLE IN is high.

	DIS
MAXIMUM RATINGS, Absolute-Maximum Values:	
DC SUPPLY-VOLTAGE RANGE, (V _{DD})	
Voltages referenced to VSS Terminal)0.5V to +20	
INPUT VOLTAGE RANGE, ALL INPUTS0.5V to VDD +0.	5V
DC INPUT CURRENT, ANY ONE INPUT	
POWER DISSIPATION PER PACKAGE (PD):	
For T _A = -55°C to +100°C	w
For T _A = +100°C to +125°C Derate Linearity at 12mW/°C to 200m	w
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	RI
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	
OPERATING-TEMPERATURE RANGE (TA)55°C to +125°	уC
STORAGE TEMPERATURE RANGE (Tstg)65°C to +150°	
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +265	°C

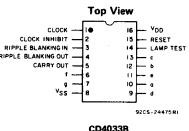




TERMINAL DIAGRAMS



CD4026B



CD4026B, CD4033B Types

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		VDD	L	UNITS	
and a second sec	· · · · ·	(V)	MIN.	MAX.	
Supply-Voltage Range (For Temperature Range)	T _A = Full Package		3	18	v
Clock Input Frequency,	fCL	5 10 15		2.5 5.5 8	MHz
Clock Pulse Width,	tWCL	5 10 15	220 100 80	- - -	
Clock Rise and Fall Time,	^t rCL ^{, t} fCL	5 10 15	- + -	Unlimited	
Clock Inhibit Set Up Time,	tSU	5 10 15	200 50 30	- -	ns
Reset Pulse Width,	tw	5 10 15	200 100 50	- - -	1
Reset Removal Time		5 10 15	30 15 10	-	

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER-	CONE	IS	LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
ISTIC	Vo	VIN	VDD								
	(V)	(V)	(V)	-55	-40	+85	+125	Min.	Тур.	Max.	
Quiescent Device	-	0,5	5	5	5	150	150		0.04	5	
Current,		0,10	10	10	10	300	300	-	0.04	10	
IDD Max.	-	0,15	15	20	20	600	600	-	0.04	20	μA
	_	0,20	20	100	100	3000	3000	-	0.08	100	
Output Low	0.4	0,5	· 5	0.64	0.61	0.42	0.36	0.51	1	-	
(Sink) Current	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	·	
IOL Min.	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current,	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	. –	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	:. —	
IOH Min.	13.5	0,15	15	-4.2	-4	2.8	-2.4	-3.4	-6.8	-	
Output Voltage:	-	0,5	5		0	.05		-	0	0.05	
Low-Level,	-	0,10	10		0	.05	_	-	· 0	0.05	v
VOL Max.	_	0,15	15		Ó	.05			0	0.05	
Output Voltage:	-	0,5	5	,	4	.95		4.95	5	-	
High Level,	-	0,10	10		9	.95		9.95	10	-	
VOH Min.	_	0,15	15		14	1.95		14.95	15	-	
Input Low	0.5, 4.5	-	5		1	1.5		. —		1.5	
Voltage,	1, 9	-	10			3				3	
VIL Max.	1.5,13.5	-	15			4		-	—	4	
Input High	0.5, 4.5		5			3.5		3.5		_	V
Voltage,	1, 9		10			7		7	—	-	
VIH Min.	1.5,13.5	-	15			11		11	-	· —	
Input Current IN Max.	-	0,18	18	±0.1	±0.1	±1,	±1		±10 ⁵	±0.1	μΑ

CD4026B

When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The CARRY OUT and UNGATED "C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

CD4033B

The CD4033B has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033B associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033B in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033B on the integer side of the display.

On the fraction side of the display the RBI of the CD4033B associated with the least significant bit is connected to a low-level voltage and the RBO of that CD4033B is connected to the RBI terminal of the CD4033B in the next more-significant-bit position. Again, this procedure is continued for all CD4033B's on the fraction side of the display.

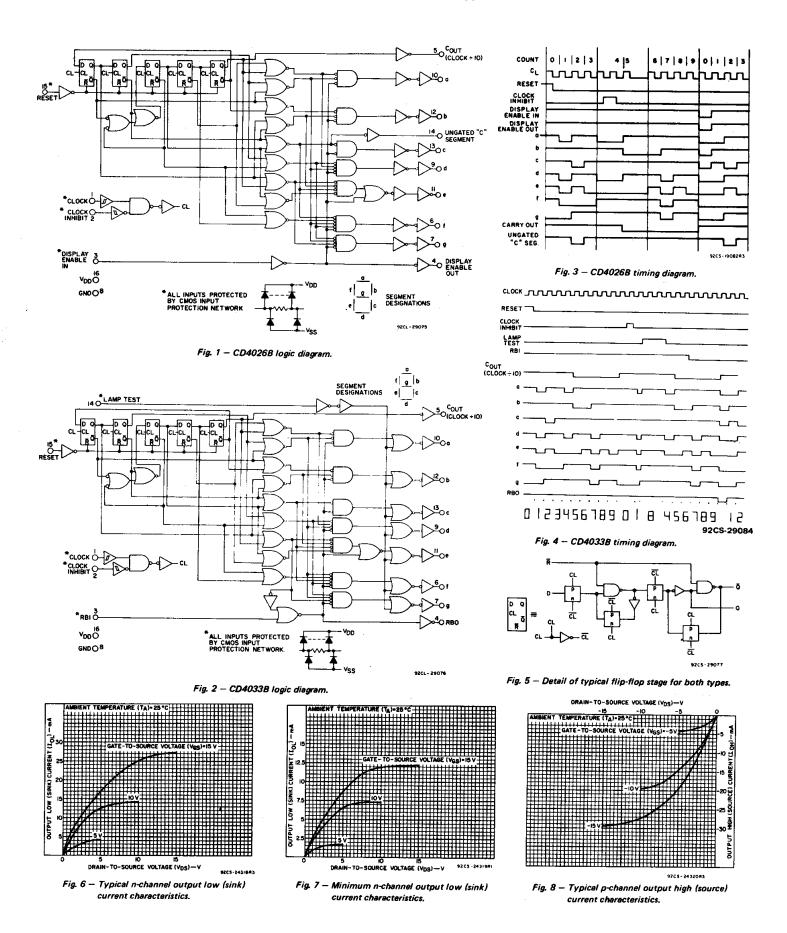
In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage (instead of to the RBO of the next more-significant-stage). For example: optional zero $\rightarrow 0.7346$. Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033B associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033B has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

The CD4026B- and CD4033B-series types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). 3

COMMERCIAL CMOS HIGH VOLTAGE ICs

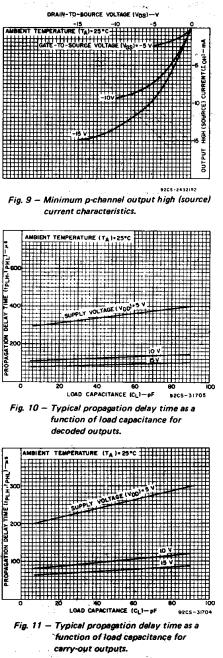


DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^{\circ}C$, Input t_r , $t_f = 20$ ns, $C_L = 50 \ pF$, $R_L = 200 \ k\Omega$

	TEST CONDITIONS	s	L		S	
CHARACTERISTIC		VDD (V)			Max.	UNITS
CLOCKED OPERATION						
Propagation Delay Time; tPLH, tPHL		5	– [250	500	
Carry-Out Line	•	10	_ `	100	200	
<u> </u>		15	_	75	150	
		5	_	350	700	
Decode Outlines		10	_	125	250	ns
		15	-	90	180	
Transition Time; tTHL, tTLH		5	_	100	200	
Carry-Out Line		10		50	100	
· · · · · · · · · · · · · · · · · · ·		15	-	25	50	
Maximum Clock Input Frequency, fCLA		5	2.5	5	-	
an a		10	5.5	11	_	MHz
		15	8	16	_	
Min. Clock Pulse Width, tw	:	5	_	110	220	
		10	_	50	100	
		15	_	40	80	
Clock and Clock Inhibit Rise or Fall Time;		5				
^t r GL ^{, t} fCL		10	Un	limite	d	ns
	·	15				
Average Input Capacitance, C _{IN}	Any Input		<u> </u>	5	7	рF
RESET OPERATION			L			
Propagation Delay Time;		5	_	275	550	
To Carry-Out Line, tpLH		10		120	240	
		15	_	80	160	
To Decode Out Lines, tPHL, tPLH		5	_	· · · · · ·	600	
		10	_	125	250	
		15			180	
Min. Reset Pulse Width, tw		5	_		120	ns
*		10	_	50	100	
		15	_	25	50	
Min. Reset Removal Time		5	_	0	30	
	i en die en die	10	-	0	15	
		15		0	10	

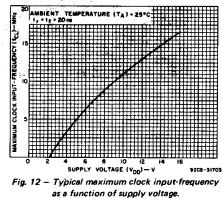
A Measured with respect to carry-out line.

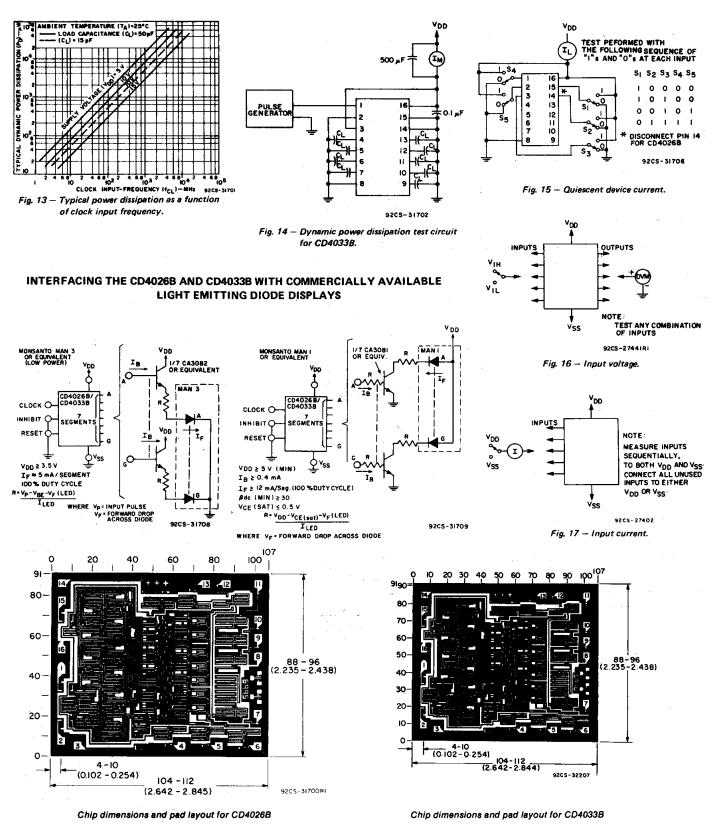
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3

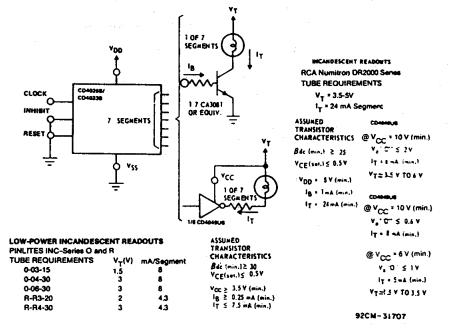
COMMERCIAL CMOS HIGH VOLTAGE ICS





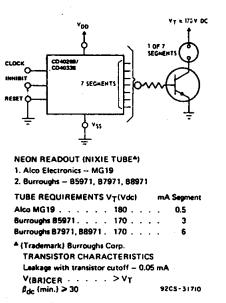
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch) .

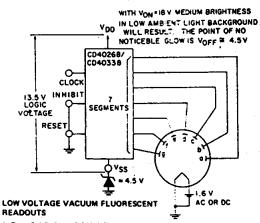
CD4026B, CD4033B Types



INTERFACING THE CD4026B AND CD4033B WITH COMMERCIALLY AVAILABLE 7-SEGMENT DISPLAY DEVICES*

* The interfacing buffers shown, while a necessity with the CD4026A and CD4033A, are not required when using the "B" devices; the "B" outputs (≈ 10 times the "A" outputs) can drive most display devices directly especially at voltages above 10 V.





1. Tung-Sol DIGIVAC S/G ‡ Type DT1704A or DT1705C 2. Nippon Electric (NEC); Type DG12E or LD915 TUBE REQUIREMENTS: 100 to 300 µA/segment at tube voltages of 12 V to 25 V depending on required brightness Filament requirement 45 m2 at 1.6 V, ac or dc.

‡ (Trademark) Wagner Electric Co.

92 65-31711

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11-Nov-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4026BE	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4026BEE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4026BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4033BE	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4033BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4033BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4033BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4033BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)



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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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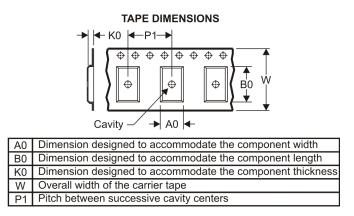
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4026BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4026BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

30-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4026BNSR	SO	NS	16	2000	346.0	346.0	33.0
CD4026BPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
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