SCHS319A - NOVEMBER 2002 - REVISED NOVEMBER 2004

- Inputs Are TTL-Voltage Compatible
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Greater Noise Immunity Than Standard Inverters
- Operates With Much Slower Than Standard Input Rise and Fall Slew Rates
- ±24-mA Output Drive Current
 - Fanout to 15 F Devices
- SCR Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

E OR M PACKAGE (TOP VIEW) 14 🛮 V_{CC} 1Y 🛮 2 13 6A 2A 🛮 3 12 6Y 2Y [4 ∏ 5A 3A 🛮 5 □ 5Y 3Y 🛮 6 9 🛮 4A GND Π 7 Π 4Υ

description/ordering information

The CD74ACT14 contains six independent inverters. This device performs the Boolean function $Y = \overline{A}$.

Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

ORDERING INFORMATION

TA	PACKA	GEŤ	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – E	Tube	CD74ACT14E	CD74ACT14E
–55°C to 125°C	SOIC - M	Tube	CD74ACT14M	ACT14M
	SOIC - IVI	Tape and reel	CD74ACT14M96	ACT 14WI

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

logic diagram, each inverter (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	\dots $-0.5\ V$ to 6 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	$\dots \dots \pm 20 \; mA$
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) (see Note 1)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	$\dots \dots \pm 100 \ mA$
Package thermal impedance, θ _{JA} (see Note 2): E package	80°C/W
M package	
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

		T _A = 25°C		–55°C TO 125°C		–40°C TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
VCC	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
VI	Input voltage	0	VCC	0	VCC	0	VCC	V
Vo	Output voltage	0	VCC	0	VCC	0	VCC	V
ІОН	High-level output current		-24		-24		-24	mA
loL	Low-level output current		24		24		24	mA
Δt/Δν	Input transition rise or fall rate		20		20		20	ns/V

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CON	V _{CC}	T _A = 3	25°C	-55 TO 12	-	–40°C TO 85°C		UNIT	
			00	MIN	MAX	MIN	MAX	MIN	MAX	
V _{T+} Positive-going threshold			5 V	1.4	2	1.4	2	1.4	2	٧
V _T – Negative-going threshold			5 V	0.8	1.3	0.8	1.3	0.8	1.3	V
ΔV_T Hysteresis $(V_{T+} - V_{T-})$			5 V	0.4		0.4		0.4		V
		ΙΟΗ = -50 μΑ	4.5 V	4.4		4.4		4.4		
.,,	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	I _{OH} = -24 mA	4.5 V	3.94		3.7		3.8		V
VOH	$V_I = V_{T+}$	$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V			3.85				V
		$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V					3.85		
		I _{OL} = 50 μA	4.5 V		0.1		0.1		0.1	
.,		I _{OL} = 24 mA	4.5 V		0.36		0.5		0.44	V
VOL	$V_I = V_{T-}$	I _{OL} = 50 mA [†]	5.5 V				1.65			V
		I _{OL} = 75 mA†	5.5 V						1.65	
lį	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND,	IO = 0	5.5 V		4		80		40	μΑ
Δl _{CC} ‡	V _I = V _{CC} - 2.1 V		4.5 V to 5.5 V		2.4		3		2.8	mA
Ci					10		10		10	pF

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C. ‡ Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

ACT INPUT LOAD TABLE

INPUT	UNIT LOAD
А	0.21

Unit load is Δl_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

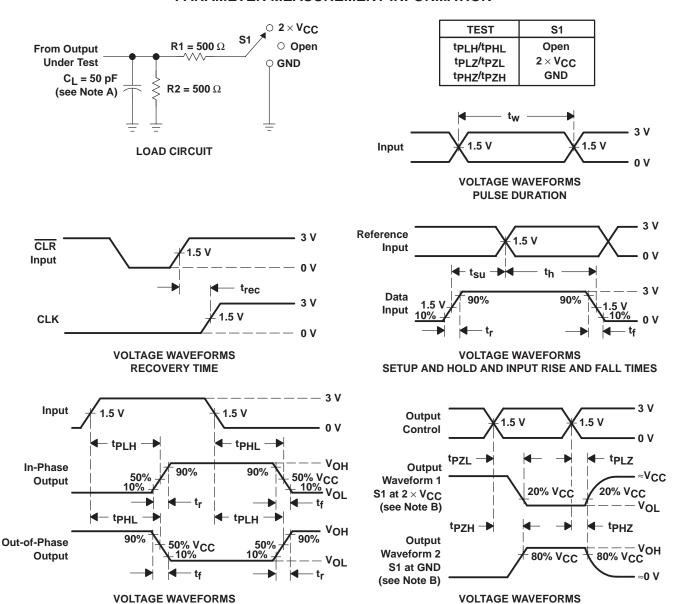
PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55 TO 12	-	–40 TO 8		UNIT
	(INPOT)	(OUTPUT)	MIN	MAX	MIN	MAX	
tPLH		V	3.6	14.5	3.7	13.2	
^t PHL	А	Y	2.4	9.5	2.4	8.6	ns

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TYP	UNIT
C _{pd}	Power dissipation capacitance	45	pF



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.

PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

OUTPUT ENABLE AND DISABLE TIMES

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_\Gamma = 3$ ns, $t_f = 3$ ns. Phase relationships between waveforms are arbitrary.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time, with one input transition per measurement.
- F. tpLH and tpHL are the same as tpd.
- G. tpzi and tpzH are the same as ten.
- H. tpLZ and tpHZ are the same as tdis.

Figure 1. Load Circuit and Voltage Waveforms







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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74ACT14E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT14EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT14M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT14M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT14M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT14M96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT14ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT14MG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

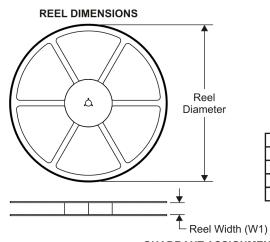
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT14M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT14M96	SOIC	D	14	2500	346.0	346.0	33.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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