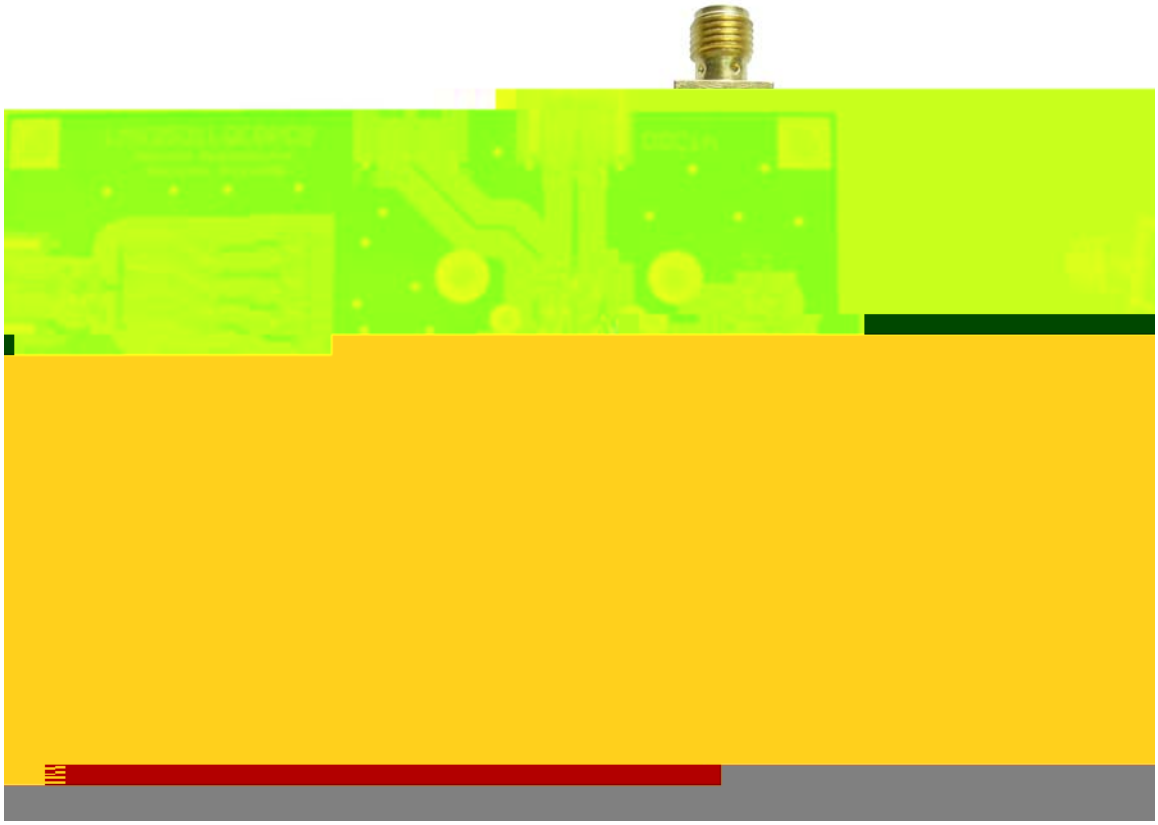
National Semiconductor

LMX2531LQ2265E

Evaluation Board Operating Instructions



National Semiconductor Corporation
Wireless Communications, RF Products Group

2900 Semiconductor Dr.
MS A2-600
Santa Clara, CA, 95052-8090

LMX2531LQ2265EFPEB Rev 1.19.2006

TABLE OF CONTENTS

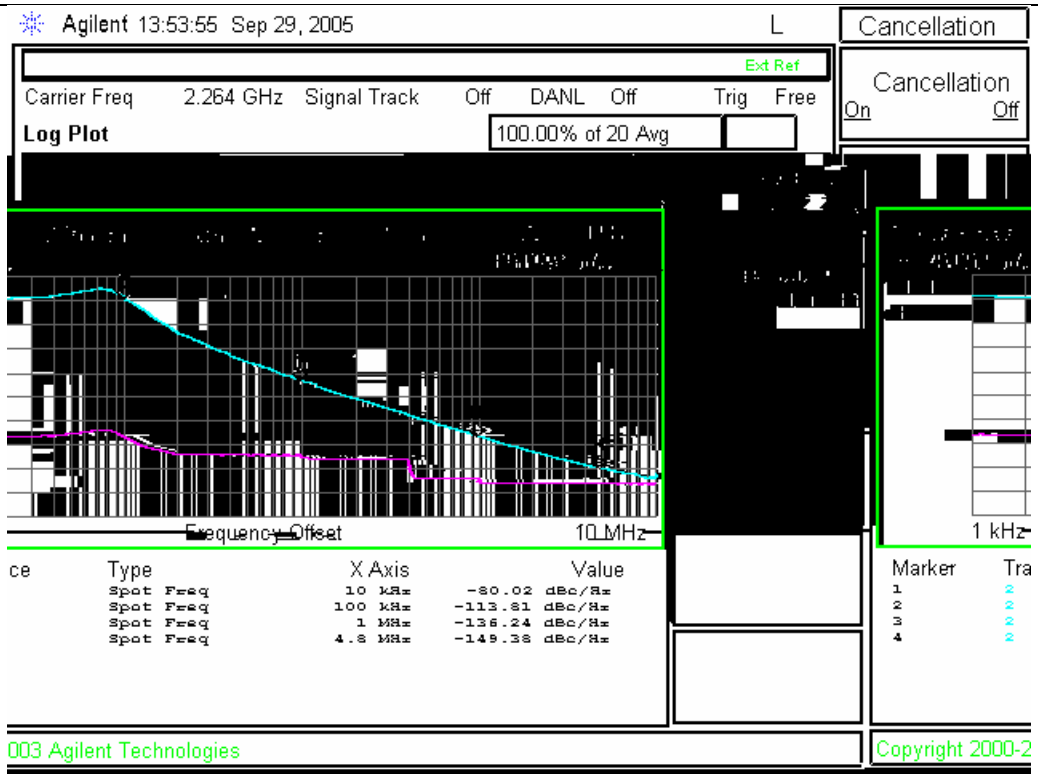
GENERAL DESCRIPTION 3
LOOP FILTER 3
PHASE NOISE 4
PHASE NOISE WITH NARROW LOOP FILTER 5
SPURS (INTERNAL DIVIDE BY 2 DISABLED) 6
SPURS (INTERNAL DIVIDE BY 2 ENABLED) 7
CODELOADER SETTINGS 8
SCHEMATIC 10
BILL OF MATERIALS 11
TOP LAYER 12
MID LAYER 2 "POWER" 14
BOTTOM LAYER "SIGNAL" 15
TOP BUILD DIAGRAM 16

General Description

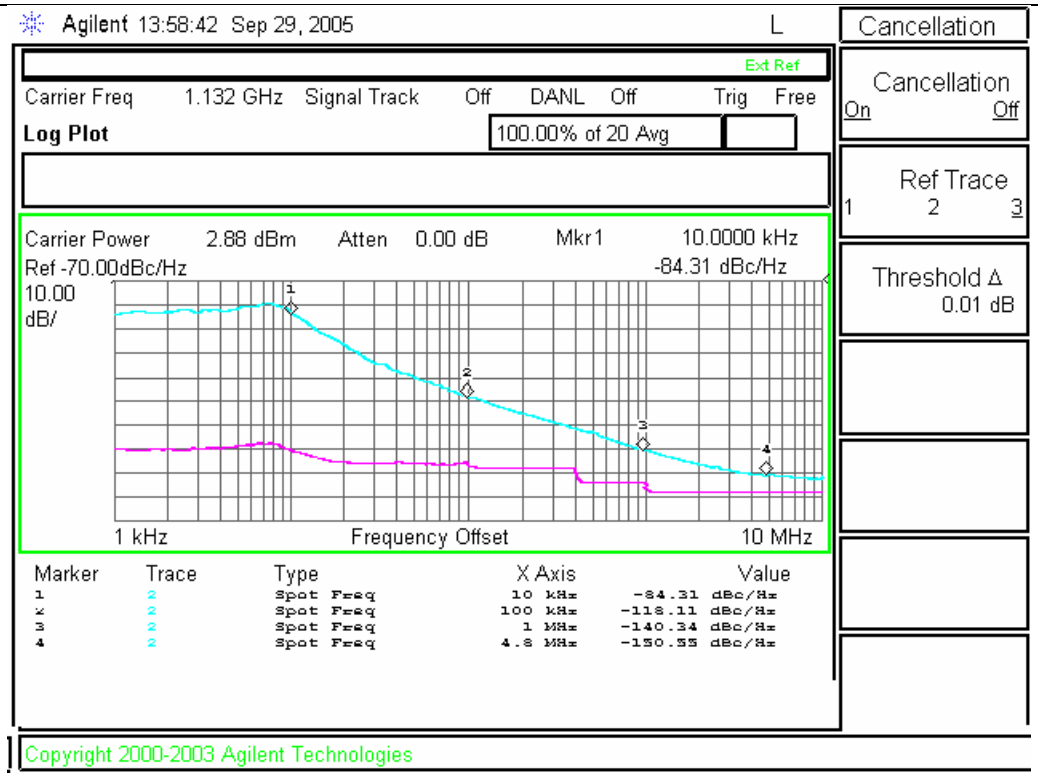
The LMX2531LQ2265E Evaluation Board simplifies evaluation of the LMX2531LQ2265E PLL/VCO synthesizer system. The board enables all performance measurements ith no additional support circuitry. The evaluation board consists of a LMX2531LQ2265E device, and a1O379 660.18 T4660.18 Tm(a)Tj1

Phase Noise

Output Frequency = 2264 MHz
Internal Divide by 2 Disabled (DIV2=0)



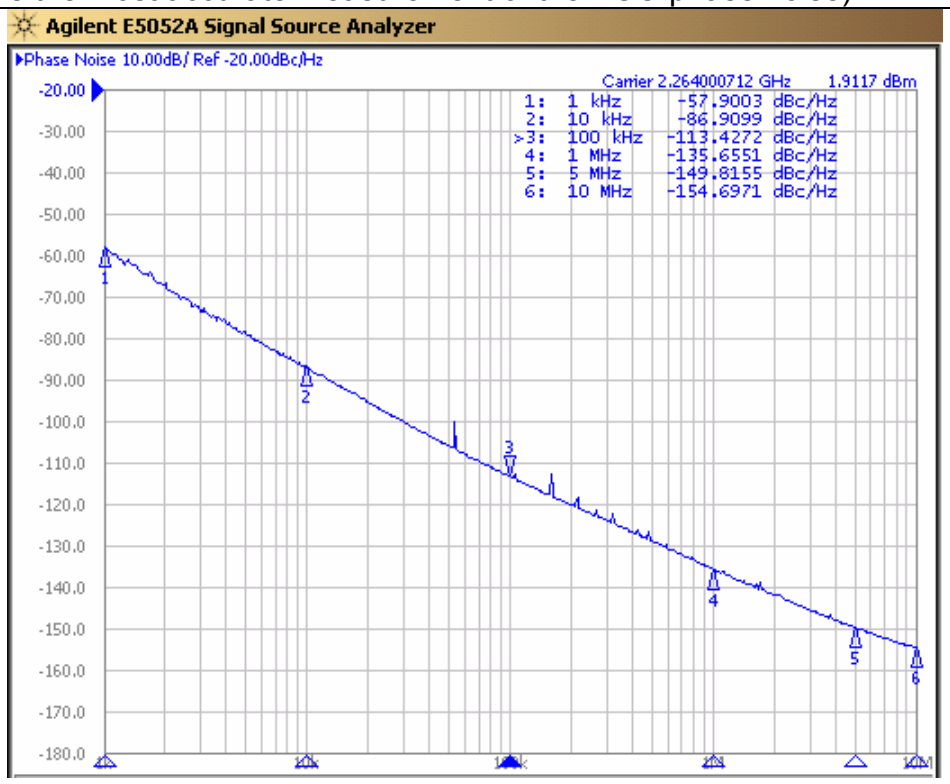
Output Frequency = 1132 MHz
Internal Divide by 2 Enabled (DIV2=1)



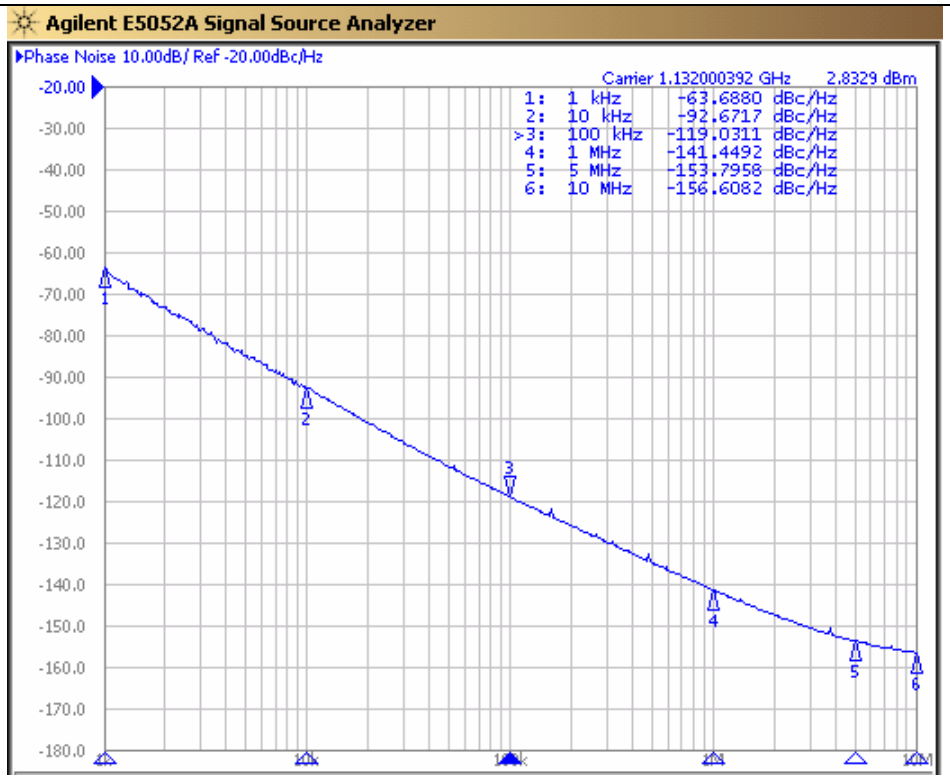
Phase Noise with Narrow Loop Filter

(This is the most accurate measurement of the VCO phase noise)

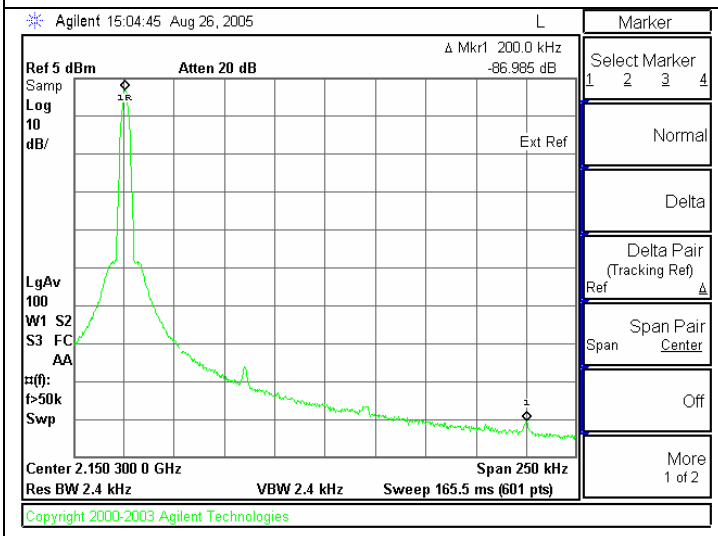
Output Frequency = 2264 MHz
Internal Divide by 2 Disabled (DIV2=0)



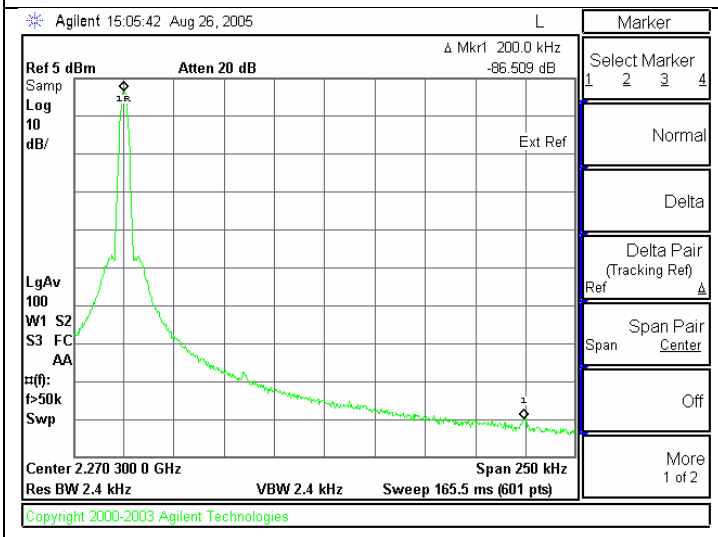
Output Frequency = 1132 MHz
Internal Divide by 2 Enabled (DIV2=1)



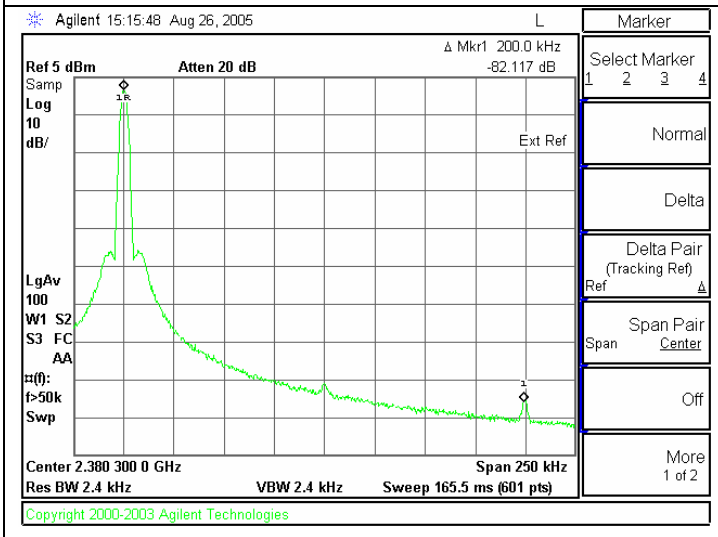
Spurs (Internal Divide by 2 Disabled)



Spur at 200 kHz offset at a orst case frequency of 2150.2 MHz is -86.9 dBc. Worst case channels occur at exactly one channel spacing above or belo a multiple of the crystal frequency (10 MHz).

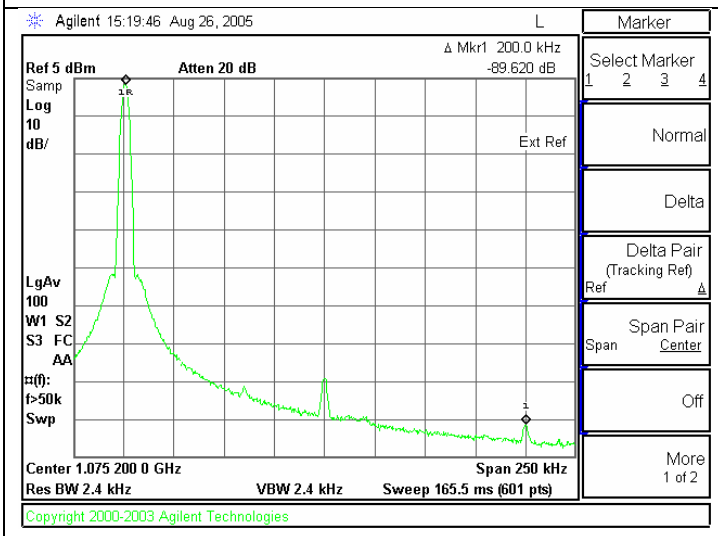


Spur at 200 kHz offset at a orst case frequency of 2270.2 MHz is -86.5 dBc.

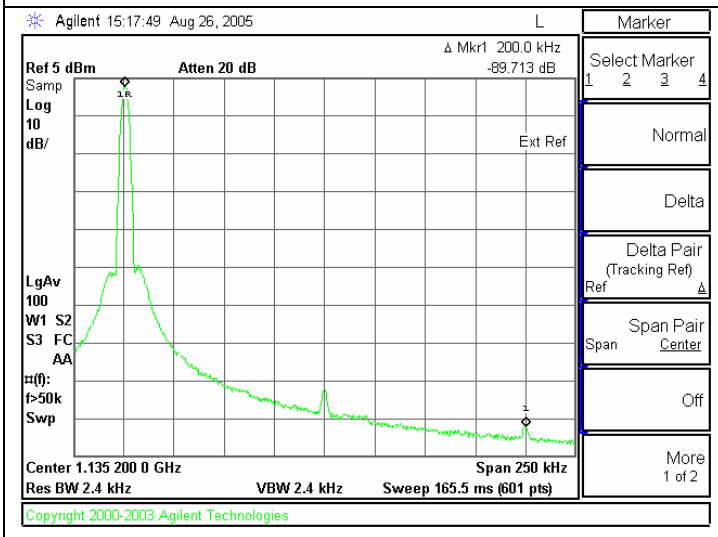


Spur at 200 kHz offset at a orst case frequency of 2380.2 MHz is -82.1 dBc.

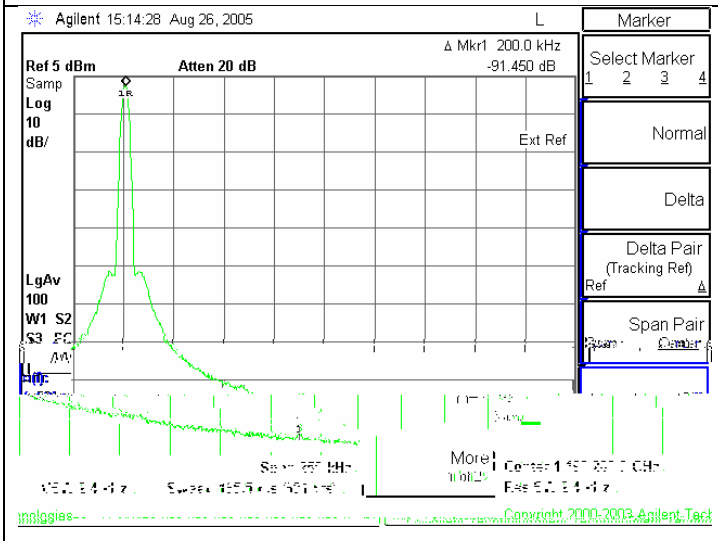
Spurs (Internal Divide by 2 Enabled)



Spur at 200 kHz offset at a frequency of 1075.1 MHz is –89.6 dBc. Since this mode uses the divide by 2 mode, the channel spacing here is actually 100 kHz. The spur at 100 kHz could be eliminated by doubling the channel spacing before the divider. The reason that the spur at 200 kHz is sho n is to illustrate theoretical 6 dB impact of the divider.



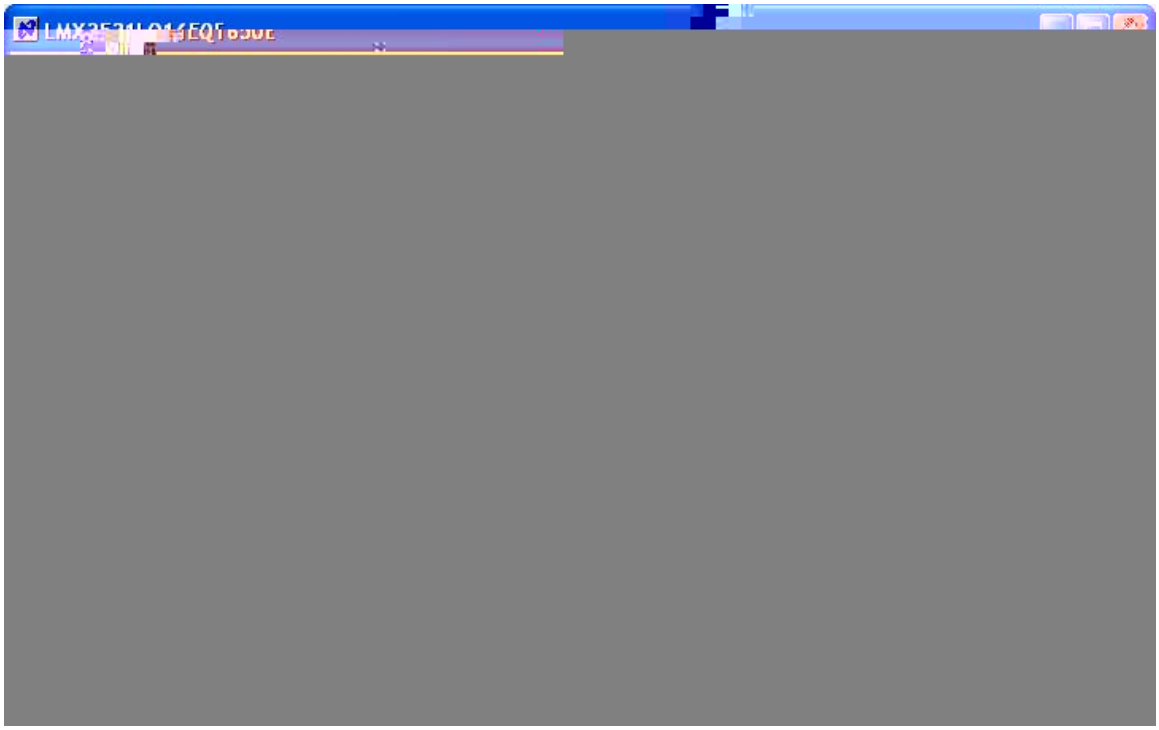
Spur at 200 kHz offset for a frequency of 1135.1 MHz is -89.7 dBc.



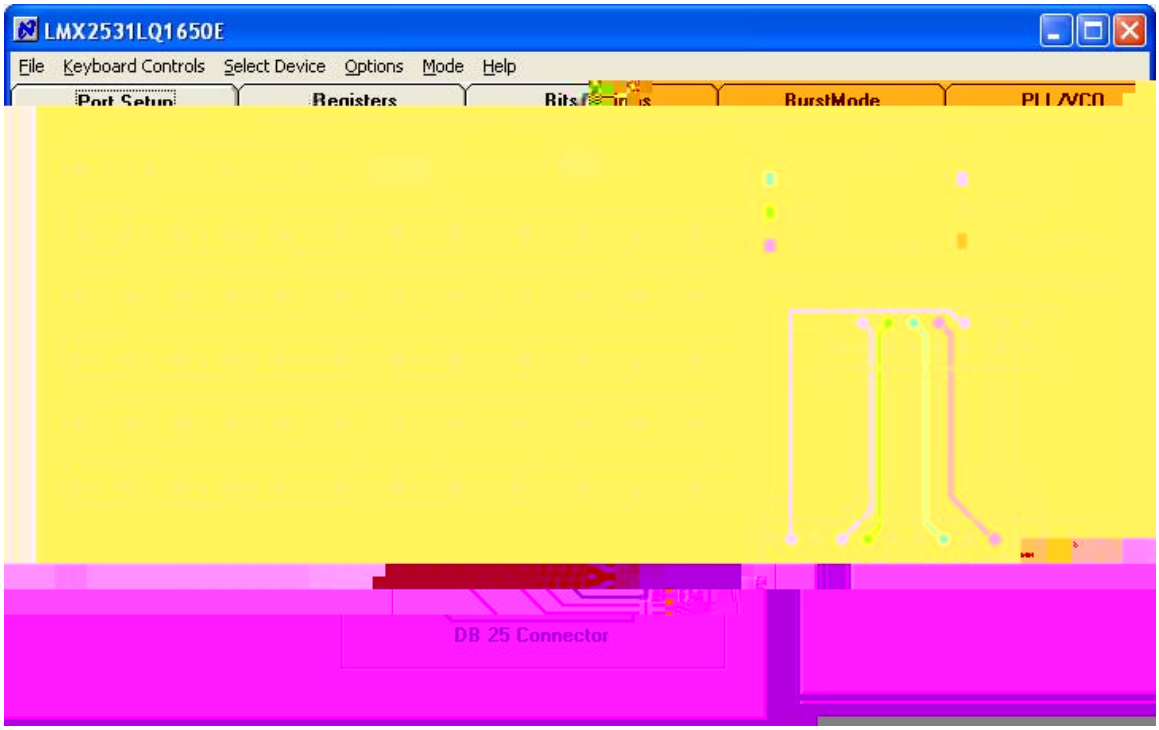
Spur at 200 kHz offset for a frequency of 1190.1 MHz is -91.4 dBc.

CodeLoader Settings

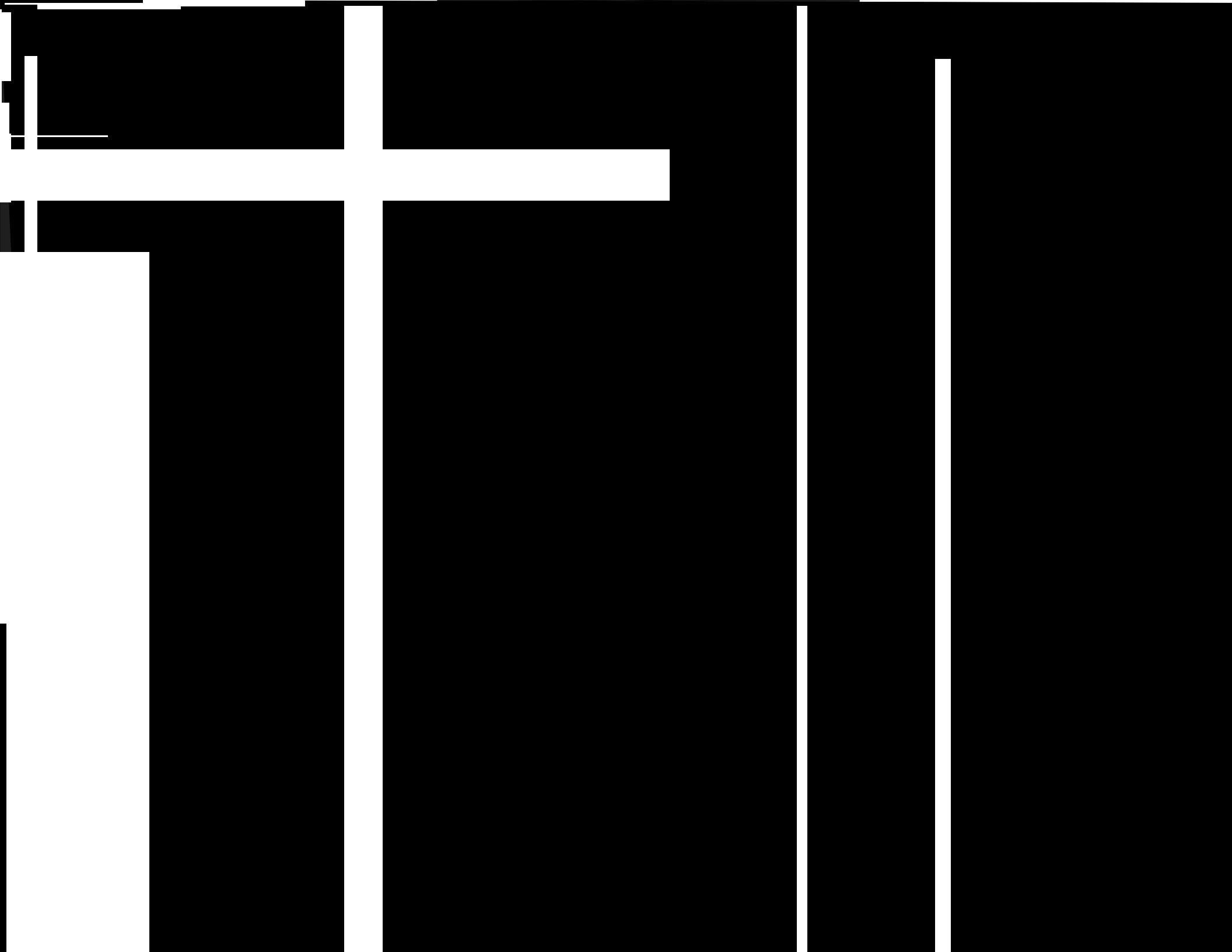
For the CodeLoader program, the default reference oscillator used for these instructions as 10 MHz, but there is a mode for a 61.44 MHz oscillator as ell. If the bits become scrambled, their original state may be recalled by choosing the appropriate mode. Note that if the internal divide by 2 is enabled, the VCO frequency still reflects the VCO frequency before the divide by 2.



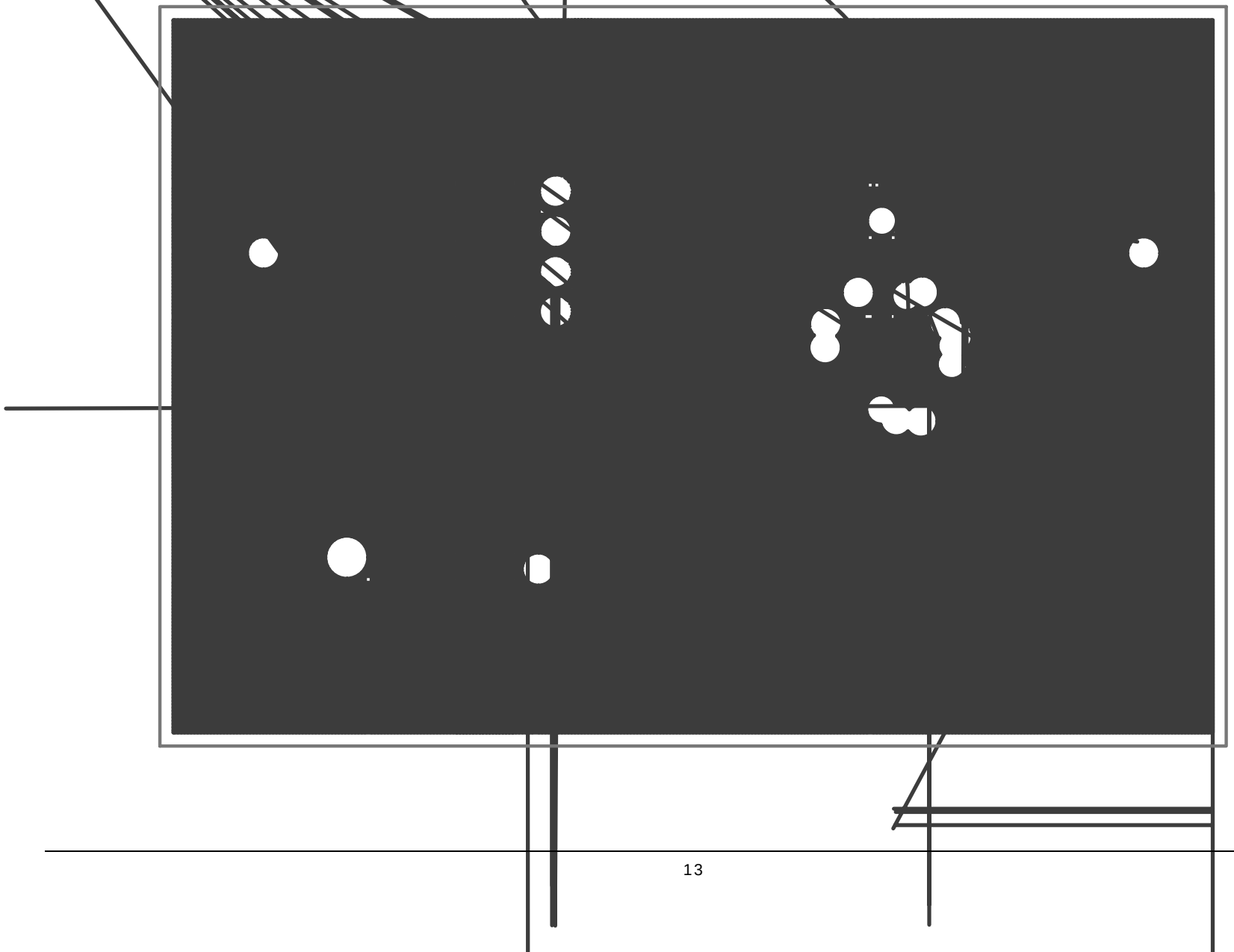
CodeLoader is set up to load the registers and initialize the part in the correct ay. R5 (INIT1) and R5 (INIT 2) are just the R5 register being used to properly initialize the part. So a single CNT+L should load the part.

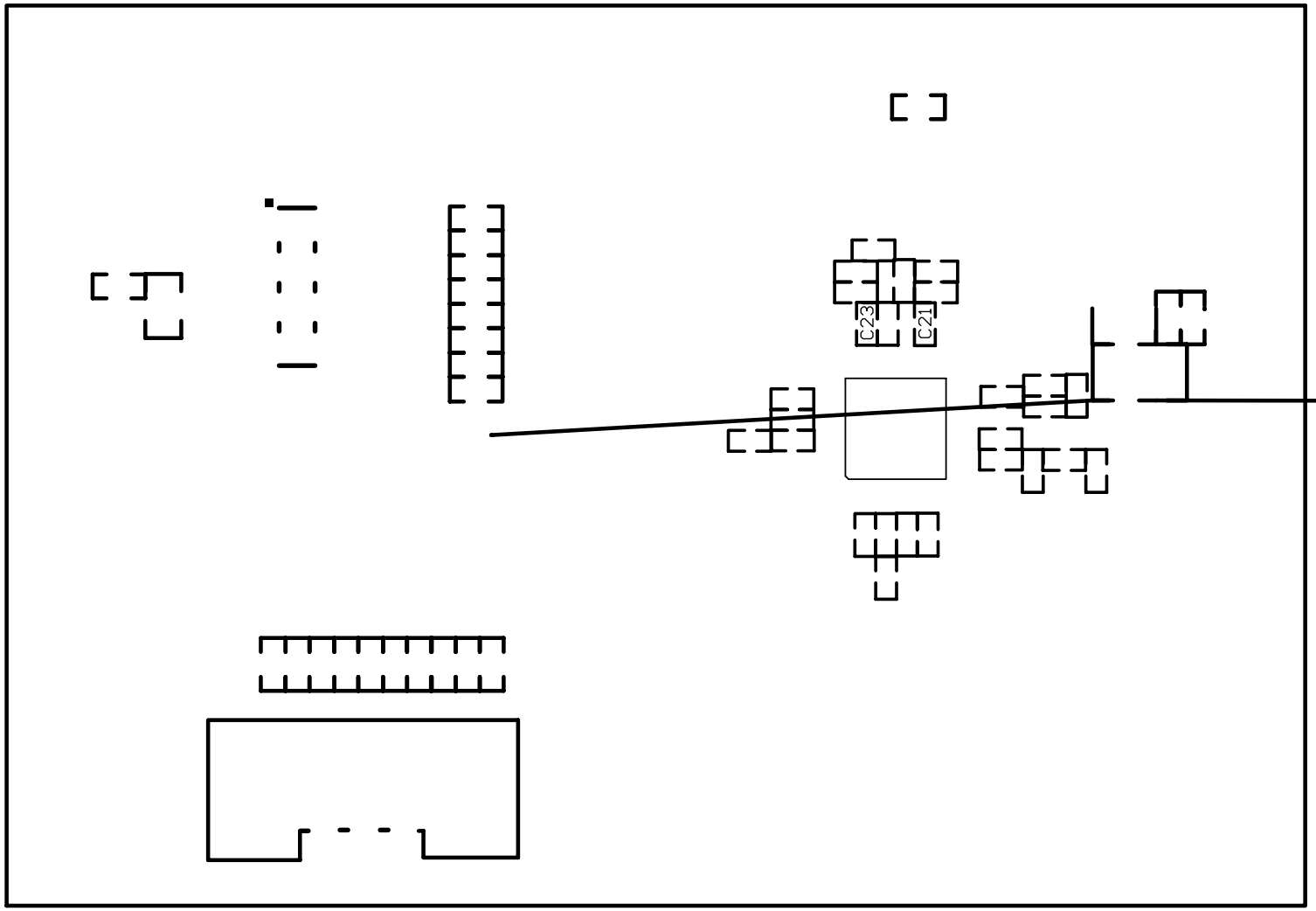


The port setup tells CodeLoader hat information goes here. If this is rong, the part ill not program. Although LPT1 is usually correct, CodeLoader does not autodetect the correct port. On some laptops, it may be LPT3.



Mid Layer 1 "Ground Plane" (15 Mils Down FR4)




C23
C21