# **ADS1298**R

# **ECG Front-End Performance Demonstration Kit**

# **User's Guide**



Literature Number: SBAU181 March 2011



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# ADS1298R

This user's guide describes the characteristics, operation, and use of the ADS1298R. This EVM is an evaluation module for the <u>ADS1298R</u>, an eight-channel, 24-bit, low-power, integrated analog front-end (AFE) designed for patient monitoring and portable and high-end electrocardiogram (ECG) and electroencephalogram (EEG) applications. The ADS1298R is intended for prototyping and evaluation. This user's guide includes a complete circuit description, schematic diagram, and bill of materials.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Device	Literature Number
ADS1298R, ADS1296R, ADS1294R	SBAS495

### 1 ADS1298R Overview

### 1.1 Important Disclaimer Information

### CAUTION

**NOTICE:** The ADS1298R is intended for feasibility and evaluation testing only in laboratory and development environments. This product is not for diagnostic use. This product is not for use with a defibrillator.

The ADS1298R is to be used only under these conditions:

- The ADS1298R is intended only for *electrical* evaluation of the features of the ADS1298R device in a laboratory, simulation, or development environment.
- The ADS1298R is **not** intended for direct interface with a patient, patient diagnostics, or with a defibrillator.
- The ADS1298R is intended for development purposes **ONLY**. It is not intended to be used as all or part of an end equipment application.
- The ADS1298R should be used only by qualified engineers and technicians who are familiar with the risks associated with handling electrical and mechanical components, systems, and subsystems.
- You are responsible for the safety of yourself, your fellow employees and contractors, and your co-workers when using or handling the ADS1298R. Furthermore, you are fully responsible for the contact interface between the human body and electronics; consequently, you are responsible for preventing electrical hazards such as shock, electrostatic discharge, and electrical overstress of electric circuit components.

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### **1.2** Information About Cautions and Warnings

This document contains caution statements. The information in a caution statement is provided for your protection. Be sure to read each caution carefully.

### CAUTION

This is an example of a caution statement. A caution statement describes a situation that could potentially damage your software or equipment.

### 2 Overview

### 2.1 Introduction

The ADS1298R is intended for evaluating the <u>ADS1298R</u> low-power, 24-bit, simultaneously sampling, eight-channel front-end for ECG and EEG applications. The digital SPI<sup>™</sup> control interface is provided by the MMB0 Modular EVM motherboard (Rev. C or higher) that connects to the ADS1298R ECG FE evaluation board (Rev. A). The ADS1298R (see Figure 1) is **NOT** a reference design for ECG and EEG applications; rather, its purpose is to expedite evaluation and system development. The output of the ADS1298R yields a raw, unfiltered ECG signal.

The MMB0 motherboard allows the ADS1298R to be connected to the computer via an available USB port. This manual shows how to use the MMB0 as part of the ADS1298R, but does not provide technical details about the MMB0 itself.

Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS1298R.

### 2.2 Supported Features

### Hardware Features:

- Configurable for bipolar or unipolar supply operation
- Configurable for internal and external clock and reference via jumper settings
- Configurable for ac- or dc-coupled inputs
- Configurable for up to 12 standard ECG leads
- External Right Leg Drive (RLD) Reference (V<sub>cc</sub> V<sub>EE</sub>)/2
- External shield drive amplifier
- External Wilson central voltage
- Easy connectivity to popular ECG simulators

### **Software Features:**

- Analysis tools including a virtual oscilloscope, histogram, FFT, and ECG display
- · File printing for post-processing of raw ECG data
- Sets the ADS1298R register settings via easy-to-use graphic user interface (GUI) software

q



### 2.3 Features Not Supported in Current Version

**NOTE:** The following features are NOT SUPPORTED by the current version of the firmware.

- Real-time data processing
- AC lead-off detection filters
- QRS detection algorithms
- Software PACE detection algorithms
- High-pass filtering
- 50Hz/60Hz notch filtering at rates other than 500SPS

### 2.4 ADS1298R Hardware

Figure 1 shows the hardware included in the ADS1298R kit. Contact the factory if any component is missing. The latest software is available on the TI website at <a href="http://www.ti.com">http://www.ti.com</a>; you should verify that you have the latest software before using the device.



### Figure 1. ADS1298R Kit

The complete kit includes the following items:

- ADS1298R ECG FE printed circuit board (PCB), Rev A
- MMB0 (Modular EVM motherboard, Rev C or higher)
- Universal ac to dc wall adapter, 120V to 240V ac to +6V dc



### **3** Software Installation

### 3.1 Minimum Requirements

Before installing the software, verify that your PC meets the minimum requirements outlined in this section.

### 3.1.1 Required Setup for ADS1298R Software

Install the software on a PC-compatible computer that meets these specifications:

- Pentium III®/ Celeron® processor, 866MHz or equivalent
- Minimum 256MB of RAM (512MB or greater recommended)
- USB 1.1-compatible input
- Hard disk drive with at least 200MB free space
- Microsoft<sup>®</sup> Windows<sup>®</sup> XP operating system with SP2 (Windows Vista and Windows 7 are NOT supported)
- Mouse or other pointing device
- 1280 x 960 minimum display resolution

### 3.2 Installing the Software

### CAUTION

Do not connect the ADS1298R before installing the software on a suitable PC. Failure to observe this caution may cause Microsoft Windows to not recognize the ADS1298R.

The latest software is available from the TI website at

<u>http://focus.ti.com/docs/toolsw/folders/print/ADS1298r.html</u>. Be sure to check the TI web site regularly for updated versions.

To install the ADS1298R software, click on the executable shown in Figure 2. Then follow the prompts illustrated in Figure 3 through Figure 6.

Name 🔺	Size Type	Date Modified
🖗 ads1298r-evm-0.6.1.0.exe	92,409 KB Application	1/24/2011 1:04 PM

Figure 2. Executable to Run ADS1298R Software Installation



Figure 3. Initialization of ADS1298R

You must accept the license agreement (shown in Figure 4) before you can proceed with the installation.

ADS1298R-EVM	
License Agreement Please review the license terms before installing ADS1298R-EVM.	ij.
Press Page Down to see the rest of the agreement.	
Common Public License Version 1.0	~
THE ACCOMPANYING PROGRAM IS PROVIDED UNDER THE TERMS OF THIS COMMON	-
PUBLIC LICENSE ("AGREEMENT"). ANY USE, REPRODUCTION OR DISTRIBUTION OF THE	
PROGRAM CONSTITUTES RECIPIENT'S ACCEPTANCE OF THIS AGREEMENT.	
1. DEFINITIONS	
"Contribution" means:	~
If you accept the terms of the agreement, click I Agree to continue. You must accept the agreement to install ADS1298R-EVM.	
AD51298R-EVM	
< Back I Agree Cance	

Figure 4. License Agreement



ADS1298R-EVM		
Installing Please wait while AD51298R-EVM is being insta	alled.	÷.
Extract: Create Interpolating Polynomial.vi		
AD51298R-EVM	< Back Next >	Cancel

Figure 5. Installation Process



Figure 6. Completion of ADS1298R Software Installation

## 4 ADS1298R Daughter Card Hardware Introduction

### CAUTION

Many of the components on the ADS1298R are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap, bootstraps, or mats at an approved ESD workstation. An electrostatic smock and safety glasses should also be worn.

The ADS1298R ECG front-end evaluation board is configured to be used with the TI MMB0 data converter evaluation platform. The key features of the ADS1298R system on a chip (SOC) are:

- Eight integrated INAs and eight 24-bit high-resolution ADCs
- Suitable for three-lead, five-lead and 12-lead ECG applications
- Low power consumption (1mW/channel)
- Data rates of 250SPS to 32kSPS
- 3V to 5V unipolar or bipolar analog supply, 1.8V to 3V digital supply.
- Lead off and PACE detection circuitry
- On-chip oscillator
- On-chip RLD amplifier
- On-chip WCT driver
- SPI data interface



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The ADS1298R can be used as a demonstration board for standard, 12-lead ECG applications with an input configuration of 10 electrodes. Users can also bypass the 12-lead configuration and provide any type of signal directly to the ADS1298R through a variety of hardware jumper settings (JP26-JP33; see Section 9.2). External support circuits are provided for testing purposes such as external references, clocks, lead-off resistors, and shield drive amplifiers.



Figure 7 shows the functional block diagram with important jumper names for the EVM.

Figure 7. ADS1298R Front-End Block Diagram

The ADS1298R board is a four-layer circuit board. The board layout is provided in Section 9; the schematics are appended to this document. The following sections explain some of the hardware settings possible with the EVM for evaluating the ADS1298R under various test conditions.

### 4.1 Power Supply

The ECG front-end EVM mounts on the MMB0 EVM with connectors J2, J3 and J4. The main power supplies (+5V, +3V and +1.8V) for the front-end board are supplied by the host board (MMB0) through connector J4. All other power supplies needed for the front-end board are generated on board by power management devices. The EVM is shipped in +3V unipolar supply configuration.

The ADS1298R can operate from +3.0V to +5.0V analog supply (AVDD/AVSS) and +1.8V to +3.0V digital supply (DVDD). A bipolar analog supply ( $\pm$ 1.5V to  $\pm$ 2.5V) can be used as well. The power consumption of the front-end board can be measured by using the JP4 jumper and JP28 jumper. The ADS1298R can be powered down by shorting jumper JP5.

Test points TP5, TP6, TP7, TP8, TP9, TP10, and TP14 are provided to verify that the host power supplies are correct. The corresponding voltages are shown in Table 1.

Test Point	Voltage	
TP7	+5.0V	
TP9	+1.8V	
TP10	+3.3V	
TP5	+3.0V	
TP13	+2.5V	
TP6	-2.5V	
TP8	GND	

### Table 1. Power-Supply Test Points

The front-end board must be properly configured in order to achieve the various power-supply schemes. The default power-supply setting for the ADS1298R is a unipolar analog supply of 3V or a bipolar analog supply of  $\pm 2.5V$  and DVDD of either  $\pm 3V$  or  $\pm 1.8V$ . Table 2 shows the board and component configurations for each analog power-supply scheme; Table 3 shows the board configurations for the digital supply.

	Unipolar An	alog Supply	Bipolar Ana	alog Supply	
AVDD/AVSS	3V	5V	±1.5V	±2.5V	
JP20	1-2	1-2	2-3	2-3	
JP2	2-3	2-3	1-2	1-2	
U7	TPS73230	TPS73250	Don't Care	Don't Care	
U9	Don't Care	Don't Care	TPS73201	TPS73201	
U8	Don't Care	Don't Care	TPS72301	TPS72301	
R52	Don't Care	Don't Care	21kΩ	47.5kΩ	
R53	Don't Care	Don't Care	78.7kΩ	43kΩ	
R56	Don't Care	Don't Care	23.3kΩ	49.9kΩ	
R57	Don't Care	Don't Care	95.3kΩ	46.4kΩ	
C87, C66, C62	Optional	Optional	Optional	Optional	

Table 2. Analog Supply Configurations (AVDD/AVSS)

### Table 3. Digital Supply Configurations (DVDD/DGND)

DVDD	+3.0V	+1.8V
JP24	1-2	2-3

or from an external clock source.

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### 4.2 Clock

The ADS1298R has an on-chip oscillator circuit that generates a 2.048MHz clock (nominal). This clock can vary by  $\pm 2\%$  over temperature. For applications that require higher accuracy, the ADS1298R can also accept an external clock signal. The ADS1298R provides an option to test both internal and external clock configurations. It also provides an option to generate the external clock from either the onboard oscillator

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The onboard oscillator is powered by the DVDD supply of the ADS1298R. Care must be taken to ensure that the external oscillator can operate either with +1.8V or +3.0V, depending on the DVDD supply configuration. Table 4 shows the jumper settings for the three options for the ADS1298R clocks.

ADS1298R Clock	Internal Clock	External OSC Clock	External Clock
JP18	Not Installed	2-3	1-2
JP23	Open or 2-3	1-2 (Disable)	Don't Care
J3 – pin 17	Don't Care	Don't Care	Clock Source

Table 4.	CLK	Jumper	Opt	ions
----------	-----	--------	-----	------

A 2.048MHz oscillator available for +3V and +1.8V DVDD is the FXO-HC735-2.048MHz and SiT8002AC-34-18E-2.048, respectively. The EVM is shipped with the external oscillator enabled.

### 4.3 Reference

The ADS1298R has an on-chip internal reference circuit that provides reference voltages to the device. Alternatively, the internal reference can be powered down and VREFP can be applied externally. This configuration is achieved with the external reference generators (U3 and U4) and driver buffer. The external reference voltage can be set to either 4.096V or 2.5V, depending on the analog supply voltage. Measure TP3 to make sure the external reference is correct. The setting for the external reference is described in Table 5.

Table 5. External Reference Jumper Option
---

Internal Reference		External Reference		
ADS1298R Reference	VREF = 2.5V	VREFP = 4.096V	VREFP = 2.5V	
JP25	Don't Care	2-3	1-2	
JP3	Not Installed	Installed	Installed	

The software uses the  $V_{REF}$  value entered in the Global Registers control tab (refer to Section 5.2) to calculate the input-referred voltage value for all the tests. The default value is 2.4V. If any other value is used, the user must update this field in the Global Registers control tab.

### 4.4 Accessing ADS1298R Analog Signals

Some ADS1298R output signals are provided as test points for probing purposes through J5. Table 6 lists the various test signals with the corresponding test points. The PACEOUT pins can also be used as an auxiliary differential input channel. These pins can also be used to perform PACE detection with external PACE detection circuitry, with appropriate user register settings (see Section 5.7.2).

Signal	J5 Pin	Number	Signal
PACEOUT1	1	2	PACEOUT2
RESERVE	3	4	RESERVE
GPIO4	5	6	PWDNB
GPIO3	7	8	DAISY_IN
GND	9	10	VCC_5V

### Table 6. Test Signals



### 4.5 Accessing ADS1298R Digital Signals

The ADS1298R digital signals (including SPI interface signals, some GPIO signals, and some of the control signals) are available at connector J3. These signals are used to interface to the MMB0 board DSP. The pinout for this connector is given in Table 7.

Signal	J3 Pin l	Number	Signal
START/CS	1	2	CLKSEL
CLK	3	4	GND
NC	5	6	GPIO1
CS	7	8	RESETB
NC	9	10	GND
DIN	11	12	GPIO2
DOUT	13	14	NC/START
DRDYB	15	16	SCL
NC	17	18	GND
NC	19	20	SDA

### Table 7. Serial Interface Pinout

### 4.6 Analog Inputs

The ADS1298R provides users the option to feed in standard ECG signals from a patient simulator to the DB15 connector, or to feed inputs from any arbitrary signal source directly to the ADS1298R.



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### 4.6.1 Patient Simulator Input

The output from any typical patient simulator can be directly fed in to the DB15 connector. For all measurements in this user guide, a Fluke medSim 300B simulator was used, as Figure 8 shows. The simulator is capable of generating ECG signals down to  $50\mu$ V of amplitude. Particular attention must be given to the common-mode value of the input signal for proper data capture. Refer to the <u>ADS1298R</u> product data sheet for the common-mode range for various programmable gain amplifier (PGA) gain settings. Section 7.1 explains the process used to capture 12-lead ECG data.



### Figure 8. Fluke Simulator Configuration

### 4.6.2 Arbitrary Input Signals

Arbitrary input signals can be fed to the ADS1298R by bypassing the DB15 connector and feeding the signal directly at jumpers JP26-JP33. Remove the set of 16 jumpers at JP26-JP33. The signal must be fed in differentially because all channel inputs are differential. If single-ended signals are used, bias the negative input of the channels to a mid-supply voltage. Again, care must be taken to ensure that the single-ended signal has an offset equal to the voltage supplied at the negative input of the channel.



### 5 Using the Software: ADS1298R Control Registers and GUI

Before starting to use the EVM software, there is one important feature that users should be aware of. The software GUI contains a *Save* tab that allows all data from any combination of channels to be saved in a given directory location with notes to describe the saved data. Figure 9 shows the *Save* tab options.

Analysis to Save		User Comments/Notes
relay as to save.		
		Record Number
Scope Analysis		30
FET Analysis		User Comments
Histogram Analysis		
Register Settings		
L		
Data to Save:		
Classe actor		
Data - Codes	Channels to Save	Directory to Save Files
Data - Volts	E CH 1	g C:\Program Files\ADS1296ECG-FE\saved
FFT Data		
- Hickory Data	VCH2	
Eriscograni baca	CH 3	
	CH 4	
	CH 5	
	CH 6	
	CH8	
		Click here to
		ave to file
		Save to me
Save to File		
1		

Figure 9. File Save Option Under Save Tab

### 5.1 Overview and Features

This section provides a quick overview of the various features and functions of the ADS1298R software package.

There are four primary tabs across the left side of the GUI:

- About tab: Provides information about the EVM and software version revisions.
- ADC Register tab: Includes all of the control registers for the ADS1298R, in a series of related sub-tabs:
  - Channel Registers tab
  - LOFF and RLD tab
  - GPIO and Other Registers tab
  - Register Map tab
- Analysis tab: Provides different ways to analyze captured data in the time or frequency domain, with a series of related sub-tabs:
  - Scope tab
  - FFT tab
  - Histogram tab
  - ECG Display tab



• **Save** tab: Provides options for saving data

### 5.2 Global Channel Registers

The first section under the *Channel Registers*→*Global Channel Registers* tab allows the user to manipulate all of the ADS1298R configuration and lead-off registers. The Global Channel Registers box includes Configuration Register 1 (controls resolution, daisy-chain/MRB mode, clock, and data rate); Configuration Register 2 (controls internal test source amplitude and frequency); Configuration Register 3 (controls the reference buffer power-up/-down processes, the reference voltage, the right leg drive (RLD) enable/disable, and the RLD reference); and the Lead Off Control Register, which controls the comparator threshold, lead-off detection mode (either resistive pull-up or current source), and the magnitude and frequency of the lead-off signal. Figure 10 shows the GUI panel to manipulate these registers and the respective settings for each.

High Resolution/Low Power Mode	Daisy-chain/Multip	le Readback Mode	CLKOUT Connection	Output Data Rate (Hz)	
Low Power Mode	Daisy Chain Mode	•	Output Disabled	f(MOD) /256	
Configuration Register 2 (CONFIG	2)				
TEST Source Test S	Signal Amplitude	Test Signal Fre	equency		
Driven Externally +1-1		contraction and the second			
The second secon	IMV (VREFP-VREFN)/2	.4 F(CLK)/2^21			
Configuration Register 3 (CONFIG	(WREFP-VREFN)/2 3)	.4 F(CLK)/2^21			
Configuration Register 3 (CONFIG Power-down Reference Buffer	3) Reference Voltage	RLD Measurement	RLDREF Signal Source	RLD Buffer Power	
Configuration Register 3 (CONFIG Power-down Reference Buffer Powered down	3) Reference Voltage VREFP = 2.4V	RLD Measurement	RLDREF Signal Source RLDREF fed externally	RLD Buffer Power	
Configuration Register 3 (CONFIG Power-down Reference Buffer Powered down Lead-Off Control Register (LOFF)	3) Reference Voltage VREFP = 2.4V	RLD Measurement	RLDREF Signal Source	RLD Buffer Power	
Configuration Register 3 (CONFIG Power-down Reference Buffer Powered down Lead-Off Control Register (LOFF) Comparator Threshold	(VREFP-VREFN)/2 3) Reference Voltage VREFP = 2.4V Lead-off D	RLD Measurement Open etection Mode Le	RLDREF Signal Source RLDREF fed externally ad-off Current Magnitude	RLD Buffer Power Powered down Lead-off Frequency	

## Figure 10. Channel Registers GUI for Global Channel Registers

Table 8 highlights the respective section of the Register Map table taken from the <u>ADS1298R product data</u> sheet.

ADDRESS	REGISTER	RESET VALUE (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Global Setti	ings Across Cl	nannels								
01h	CONFIG1	06	HR	DAISY_EN	CLK_EN	0	0	DR2	DR1	DR0
02h	CONFIG2	40	0	1	0 <sup>(1)</sup>	INT_TEST	0	TEST_AMP	TEST_FREQ1	TEST_FREQ0
03h	CONFIG3	40	PD_REFBµF	1	VREF_4V	RLD_MEAS	RLDREF_INT	PD_RLD	RLD_LOFF_ SENS	RLD_STAT
04h	LOFF	00	COMP_TH2	COMP_TH1	COMP_TH0	VLEAD_OFF_ EN	ILEAD_OFF1	ILEAD_OFF0	FLEAD_OFF1	FLEAD_OFF0

### Table 8. Register Assignments: Global Channel Registers

<sup>(1)</sup> This register bit must be written to '1' at power-up if hardware PACE detect is used on a lead using the WCT signal.

### 5.2.1 Lead-Off Control Register

The Lead-Off Control Register allows the user to configure the threshold for the lead-off comparator, resistive pull-up or current-source excitation, the lead-off current magnitude, and dc or ac detection. Figure 11 illustrates a simplified diagram of the resistive pull-up and excitation options for the lead-off detect feature.



Figure 11. Lead-Off Excitation Options

Table 9 shows the corresponding register and Figure 12 shows the respective GUI controls.

### Table 9. LOFF: Lead-Off Control Register (Address: 04h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMP_TH2	COMP_TH1	COMP_TH0	VLEAD_OFF_EN	ILEAD_OFF1	ILEAD_OFF0	FLEAD_OFF1	FLEAD_OFF0

Lead-Off Control Register (LOFF)			
Comparator Threshold L	ead-off Detection Mode	Lead-off Current Magnitude	Lead-off Frequency
Positive - 95% : Negative - 5%	Current Mode	6nA	DC Lead-off Detection ON

### Figure 12. Lead-Off Control Register GUI Controls

### 5.2.2 Configuration Register 1

Configuration Register 1enables the user to control the resolution mode (that is, high-resolution or low-power mode), enable the daisy-chain configuration options, and program the data rate. Table 10 shows the register settings. Figure 13 illustrates the respective GUI controls.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HR	DAISY_EN	CLK_EN	0	0	DR2	DR1	DR0

1	Configuration Register 1 (CONFIG1)			
	High Resolution/Low Power Mode	Daisy-chain/Multiple Readback Mode	CLKOUT Connection	Output Data Rate (Hz)
	High Resolution Mode	Daisy Chain Mode	Output Disabled	f(MOD) /1024

### Figure 13. Configuration Register 1 GUI Panel

### 5.2.3 Configuration Register 2

Configuration Register 2 enables the user to select and program an internal square wave test source amplitude to  $\pm 1$ mV or  $\pm 2$ mV and its frequency to dc, 2Hz, or 4Hz. Table 11 shows the register map for Configuration Register 2; the GUI controls are shown in Figure 14.

	Table 11. CONFIG2: Configuration Register 2 (Address = 02h)											
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0					
0	0	0	INT_TEST	0	TEST_AMP	TEST_FREQ1	TEST_FREQ0					

Configuration Register 2 (CONFIG2)				
TEST Source	Test Signal Amplitude	Test Signal Frequency		
Generated Internally	+/- 1mV (VREFP-VREFN)/2.4	f(CLK)/2^21		

### Figure 14. Configuration Register 2 GUI Controls

### 5.2.4 Configuration Register 3

Configuration Register 3 controls the bandgap reference (illustrated in Figure 15) and right leg drive (RLD) options. This register enables the user to select between an external or internal reference voltage, enable/disable the internal reference buffer, toggle between a 2.4V or a 4.0V output voltage, and to enable/disable the RLD as well as choose whether the RLD voltage is provided internally or externally. The register map is provided in Table 12; Figure 16 shows the GUI display for Configuration Register 3.



Figure 15. Internal Reference and Buffer Connections

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
PD_REFBµF	1	VREF_4V	RLD_MEAS	RLDREF_INT	PD_RLD	RLD_LOFF_SENS	RLD_STAT		
Configuration Re	gister 3 (CONFI	53)							
Power-down Re	Power-down Reference Buffer Reference Voltage RLD Measurement RLDREF Signal Source RLD Buffer Power								
Enabled		VREFP = 2.4	/ RLD_IN	Routed R	LDREF = AVDI	D/2 Enabled			

### Figure 16. Configuration Register 3 GUI Controls



### 5.3 Channel Control Registers

The second section under the Channel Registers tab is the *Channel Control Registers* box. This panel allows the user to uniquely configure the front-end MUX for each channel. Additionally, at the top of the Channel Control Registers box is the option to globally set all channels to the same setting. The channel-specific MUX is illustrated in Figure 17.



Figure 17. Input Multiplexer for a Single Channel

Table 8 lists the register map, while the GUI panel for this MUX and register map is given in Figure 18.

		RESET VALUE												
ADDRESS	REGISTER	(Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0				
Channel-Spe	Channel-Specific Settings													
05h	CH1SET	00	PD1	GAIN12	GAIN11	GAIN10	0	MUXn2	MUXn1	MUXn0				
06h	CH2SET	00	PD2	GAIN22	GAIN21	GAIN20	0	MUX22	MUX21	MUX20				
07h	CH3SET	00	PD3	GAIN32	GAIN31	GAIN30	0	MUX32	MUX31	MUX30				
08h	CH4SET	00	PD4	GAIN42	GAIN41	GAIN40	0	MUX42	MUX41	MUX40				
09h	CH5SET <sup>(1)</sup>	00	PD5	GAIN52	GAIN51	GAIN50	0	MUX52	MUX51	MUX50				
0Ah	CH6SET <sup>(1)</sup>	00	PD6	GAIN62	GAIN61	GAIN60	0	MUX62	MUX61	MUX60				
0Bh	CH7SET <sup>(1)</sup>	00	PD7	GAIN72	GAIN71	GAIN70	0	MUX72	MUX71	MUX70				
0Ch	CH8SET <sup>(1)</sup>	00	PD8	GAIN82	GAIN81	GAIN80	0	MUX82	MUX81	MUX80				
0Dh	RLD_SENSP (2)	00	RLD8P <sup>(1)</sup>	RLD7P <sup>(1)</sup>	RLD6P <sup>(1)</sup>	RLD5P <sup>(1)</sup>	RLD4P	RLD3P	RLD2P	RLD1P				
0Eh	RLD_SENSN <sup>(2)</sup>	00	RLD8N <sup>(1)</sup>	RLD7N <sup>(1)</sup>	RLD6N <sup>(1)</sup>	RLD5N <sup>(1)</sup>	RLD4N	RLD3N	RLD2N	RLD1N				
0Fh	LOFF_SENSP (2)	00	LOFF8P	LOFF7P	LOFF6P	LOFF5P	LOFF4P	LOFF3P	LOFF2P	LOFF1P				
10h	LOFF_SENSN (2)	00	LOFF8N	LOFF7N	LOFF6N	LOFF5N	LOFF4N	LOFF3N	LOFF2N	LOFF1N				
11h	LOFF_FLIP	00	LOFF_FLIP8	LOFF_FLIP7	LOFF_FLIP6	LOFF_FLIP5	LOFF_FLIP4	LOFF_FLIP3	LOFF_FLIP2	LOFF_FLIP1				

### Table 13. Register Assignments: Channel-Specific Settings

<sup>(1)</sup> CH5SET and CH6SET are not available for the ADS1294R. CH7SET and CH8SET registers are not available for the ADS1294R and ADS1296R.

<sup>(2)</sup> The RLD\_SENSP, PACE\_SENSP, LOFF\_SENSP, LOFF\_SENSN, and LOFF\_FLIP registers bits[5:4] are not available for the ADS1294R. Bits[7:6] are not available for the ADS1294R and ADS1296R.

Power-down	PGA Gain	Channel Input			
Normal Operation	6	✓ Normal Electrode			
normal operation	10	Input Short			
		RLD Measurement			
Channel 1 Control Regi	ster (CH1SET)	MVDD	Channel 2 Control Reg	ister (CH2SET)	
Power-down	PGA Gain	Temperature Sensor	Power-down	PGA Gain	Channel Input
Normal Operation	6	Test Signal	Normal Operation	6	Normal Electrode
	-	RLD Positive Electrode Driver	P		
Thannel 3 Control Reg	ister (CH3SET)	RLD Negative electrode Driver	Channel 4 Control Reg	ister (CH4SET)	
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input
Normal Operation	6	Normal Electrode	Normal Operation	6	Normal Electrode
Channel 5 Control Reg	ister (CH5SET)		Channel 6 Control Reg	ister (CH6SET)	
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input
Normal Operation	6	Normal Electrode	Normal Operation	6	Normal Electrode
Channel 7 Control Reg	ister (CH7SET)		Channel 8 Control Reg	ister (CH8SET)	
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input
Name al Calenakian	6	Name of Classica de	Normal Operation	6	Normal Electrode

### Figure 18. Channel Control Registers GUI Panel



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### 5.4 Internal Test Signals Input and the ECG Display Tab

Configuration Register 2 controls the signal amplitude and frequency of an internally-generated square wave test signal. The primary purpose of this test signal is to verify the functionality of the front-end MUX, the PGA, and the ADC. The test signals may be viewed on the *Analysis* $\rightarrow$ *ECG Display* tab, as Figure 19 shows. Detailed instructions for using the *Analysis* $\rightarrow$ *ECG Display* tab are provided in Section 6.1.4.



Figure 19. Example of Internal Test Signals Viewed on the ECG Display Tab



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### 5.5 Temperature Sensor and the Scope Tab

The internal temperature sensor on the ADS1298R is shown in Figure 20. When the internal MUX is routed to the temperature sensor input, the output voltage of the ADC may be converted to a temperature value, using Equation 1.

Temperature (°C) =  $\left(\frac{\text{Temperature Reading }(\mu V) - 145,300\mu V}{490\mu V/^{\circ}C}\right) + 25^{\circ}C$ 

AVSS Figure 20. Internal Temperature Sensor

The output voltage corresponding to a given temperature can be read by selecting the *Temperature* Sensor option on the Channel Control Registers GUI (see Figure 18) and verified using the *Analysis* $\rightarrow$ *Scope* tab as shown in Figure 21. The number **0.1447V** (on the y-axis) can be calculated as a temperature using Equation 1:

Temperature = (0.1447 - 0.145300) / 0.00049 + 25 = 23.78°C A more detailed description of the Scope tab is provided in Section 6.1.1.



Figure 21. Eight-Channel Read of Internal Temperature

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### 5.6 Normal Electrode Input and the ECG Display Tab

The *Normal electrode* input on the MUX routes the inputs (VINP and VINN) differentially to the internal PGA, as Figure 17 illustrates. In this mode, an ECG, sine wave, or pulse generator may be connected to test the ADS1298R.



Figure 22 shows a typical six-lead output when connected to a 5mV<sub>PEAK</sub>, 80BPM ECG signal.

Figure 22. Normal Electrode ECG Connection in ECG Display Tab

### 5.6.1 MV<sub>DD</sub> Input and the Scope Tab

The MV<sub>DD</sub> input option allows the measurement of the supply voltage  $V_S = (AV_{DD} + AV_{SS})/2$  for channels 1, 2, 5, 6, 7, and 8; however, the supply voltage for channel 3 will be  $DV_{DD}/2$ . As an example, in bipolar supply mode,  $AV_{DD} = 3.0V$  and  $AV_{SS} = -2.5V$ . Therefore, with the PGA gain = 1, the output voltage measured by the ADC will be approximately 0.25V.

### 5.6.2 RLD Measurement, RLD Positive Electrode Driver, and RLD Negative Electrode Driver

This measurement takes the voltage at the RLDIN pin and measures it on the PGA with respect to  $(AV_{DD} + AV_{SS})/2$ . This feature is beneficial if the user would like to optimize the gain of the RLD loop. The voltage used to derive the right leg drive for both the positive and negative electrodes may also be measured with respect to  $(AV_{DD} + AV_{SS})/2$ .

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### 5.7 GPIO and Other Registers

The *GPIO* and *Other Registers* tab, located under the *Analysis* tab, includes controls for GPIO1 through GPIO4, respiration phase and frequency, routing of the Wilson amplifiers, and derivation of the Goldberger terminals.

### 5.7.1 General-Purpose I/O Register (GPIO)

The GPIO registers control four general-purpose I/O pins; Table 14 shows the respective register to control these pins. Note that if respiration mode is enabled, these GPIO pins become dedicated to respiration functions and are not available for other use. Figure 23 illustrates the GPIO Control Register GUI panel.

Table 14. GPIO: General-Purpose I/O Register (Address = 14h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1



Figure 23. GPIO Control Register GUI Panel

### 5.7.2 PACE Detect Register

The PACE Detect Register **does not** enable a special PACE measurement mode; rather, it configures Pace Amplifier 1 to connect to input channels 1-4 *or* Pace Amplifier 2 to connect to input channels 5-8. Table 15 and Figure 24 show register settings (from the data sheet) and the GUI controls, respectively, for setting the PACE Register amplifiers.

Table 15. PACE: PACE Detect Register (Address = 15h)										
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0			
0	0	0	PACEE1	PACEE0	PACEO1	PACEO0	PD_PACE			

PACE Detect Register (P	ACE)	
PACE_OUT2 Odd	PACE_OUT1 Even	Pace Detect Buffer Enable
CH1	CH2	Buffer Off

### Figure 24. PACE Detect Register GUI Controls



#### 5.7.3 **Respiration Control Register**

The Respiration Control Register allows the user to configure the respiration frequency, single-shot or continuous-conversion mode, routing of the Wilson Central terminals to the RLD reference, and enabling/disabling the lead-off comparators. The register table is given in Table 16, and the Respiration Register GUI controls are illustrated in Figure 25.

			. Respiration	i control heg	ister (Addres	5 - 1011)	
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RESP_ DEMOD_EN1	RESP_MOD_ EN1	RESP_MOD_ VREFP	RESP_PH2	RESP_PH1	RESP_PH0	RESP_CTRL1	RESP_CTRL0

### Table 16 RESP: Respiration Control Register (Address - 16h)

Configuration Register 4	(CONFIG4)

toringuration Register + (Colvir 14+)			
Respiration Frequency	Pulse Mode Enable	Lead-off Comparator Power-down	
64kHz	Disable	Enable	

### Figure 25. Respiration Control Register GUI Panel

#### 5.7.4 Wilson Central and Augmented Lead Registers

The Wilson Central Voltage (an average voltage between the right arm [RA], left arm [LA], and left leg [LL] connections) can be derived from any combination of positive and negative terminals from channels 1-4 and routed to the WCT pin. Likewise, the Augmented Leads (AVF, AVL, AVR) may be derived from channels 1-4 and routed to the negative terminal of channels 5, 6, and 7. Figure 26 shows these configurations; Figure 26a illustrates the central lead routing, and Figure 26b shows the augmented lead routing.



### Figure 26. Wilson Central and Augmented Lead Routing Diagrams

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Table 17 and Table 18 show the respective register settings. Figure 27 illustrates the GUI control panel for these registers.

. . .

I able	17. WC11: W	lison Center	i erminai ar	na Augmentea	Lead Control I	Register (Add	aress = 18h)		
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
aVF_CH6	aVL_CH5	aVR_CH7	aVR_CH4	PD_WCTA	WCTA2	WCTA1	WCTA0		
Table 18. WCT2: Wilson Center Terminal Control Register (Address = 19h)									
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
PD_WCTC	PD_WCTBC	WCTB2	WCTB1	WCTB0	WCTC2	WCTC1	WCTC0		
Wilson Center Terminal a	Wilson Center Terminal and Augmented Lead Register (WCT1)								
Left Leg (aVF) to CH6	Left Arm (aVL)	o CH5 Right Ar	m (aVR) to CH7 💦 R	light Arm (aVR) to CH4	Power-down WCTA	WCT Amplifier C	hannel A		
Disable	Disab	le	Disable	Disable	Powered down	CH1 Po	sitive Input		
Wilson Center Terminal Register (WCT2)									
Powered down	Power	red down	CH2 Positive Input	CH3 Positive	Input				

Figure 27. Wilson Central and Augmented Lead Register GUI Controls

### 5.8 Lead-Off and RLD Registers

The Lead-Off Detection and Current Control Registers and the Right Leg Derivation Control Registers are located under the ADC Register $\rightarrow$ LOFF and RLD tab.

### 5.8.1 Lead-Off Sense (LOFF\_SENSP and LOFF\_SENSN) Registers

These registers enable lead-off detection for both the positive and negative channels. Figure 11 describes the mode for Lead-Off Detection (that is, resistive or current source) and the 4-bit DAC settings to configure the lead-off threshold. Note that the LOFF\_FLIPx bits change the direction of the lead-off current if this option is selected. Figure 28 illustrates the connections from the positive and negative inputs to the lead-off comparators. Table 19 through Table 21 list the register tables for the lead-off comparators, and Figure 29 shows the respective GUI panel on the EVM software.



Figure 28. LOFF\_STATP and LOFF\_STATN Comparators



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Table 19. LOFF_SENSP (Address = 0Fh)											
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0				
LOFF8P	LOFF7P	LOFF6P	LOFF5P	LOFF4P	LOFF3P	LOFF2P	LOFF1P				
	Table 20. LOFF_SENSN (Address = 10h)										
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0				
LOFF8N	LOFF7N	LOFF6N	LOFF5N	LOFF4N	LOFF3N	LOFF2N	LOFF1N				
	Table 21. LOFF_FLIP (Address = 11h)										
LOFT_FLIF6		LOFF_FLIF0	LOFF_FLIF5	LOFF_FLIF4	LOFF_FLIF5	LOFF_FLIFZ	LOFF_FLIFT				
Set All LOFFP DISABLE Set All LOFFN DISABLE Set All LOFF F	Bits ED EBIts ED ELIP Bits	LOFFP8 LO Lead Off Sense Positiv LOFFN8 LO Lead Off Sense Negati LOFF_FLIP8 LOF Lead Off Current Direct	FFP7 LOFFP6  FFN7 LOFFN6  FFN7 LOFFN6  FF_FLIP7 LOFF_FLIP6  Ff_FLIP7 LOFF_FLIP6  Ction	LOFFNS LO	OFFP4 LOFFP3	LOFFP2 LO LOFFN2 LO LOFF_FLIP2 LOF	FFP1				

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Figure 29. LOFF\_SENSP and LOFF\_SENSN Registers GUI Controls

#### 5.8.2 Lead-Off Status Registers (LOFF STATP and LOFF STATN)

These registers (shown in Table 22 and Table 23) store the output of the lead-off comparator that corresponds with each input. When a lead is disconnected, the corresponding register bit activates low. The GUI for this feature is enabled by clicking in the upper right-hand corner of the EVM software on the Show/Poll Lead-Off Status button. Pressing this button causes a pop-up box that shows the status of the lead-off registers. The GUI shows when a lead is disconnected by turning its bit from green to red. Figure 30 illustrates the Lead-Off Status Registers GUI controls.

Table 22. LOFF_STATP (Read-Only; Address = 12h)									
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
IN8P_OFF	IN7P_OFF	IN6P_OFF	IN5P_OFF	IN4P_OFF	IN3P_OFF	IN2P_OFF	IN1P_OFF		

Table 23. LOFF_STATN (Read-Only; Address = 13h)									
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
IN8N_OFF	IN7N_OFF	IN6N_OFF	IN5N_OFF	IN4N_OFF	IN3N_OFF	IN2N_OFF	IN1N_OFF		







#### 5.8.3 **Right Leg Drive Derivation Control Registers**

The Right Leg Drive Derivation Control Registers enable the user to set any combination of positive and/or negative electrodes to derive the RLD voltage that is fed to the internal right leg drive amplifier. Table 24 and Table 25 list the RLD\_SENSP and RLD\_SENSN registers, respectively, that control these bits. Figure 31 shows the corresponding GUI controls.

#### Table 24. RLD\_SENSP (Address = 0Dh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RLD8P	RLD7P	RLD6P	RLD5P	RLD4P	RLD3P	RLD2P	RLD1P

Table 25. RLD_SENSN (Address = 0Eh)									
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
RLD8N	RLD7N	RLD6N	RLD5N	RLD4N	RLD3N	RLD2N	RLD1N		



### Figure 31. RLD\_SENSP and RLD\_SENSN GUI Controls



### 5.9 Register Map

The Register Map $\rightarrow$  Device Registers tab is a helpful debug feature that allows the user to view the state of all the internal registers. This tab is illustrated in Figure 32.

Device Registers										
Register	Address	Value	D7	D6	D5	D4	D3	D2	D1	DO
ID	0x00	0x52	0	1	0	1	0	0	1	0
CONFIG1	0×01	0x86	1	0	0	0	0	1	1	0
CONFIG2	0×02	0×10	0	0	0	1	0	0	0	0
CONFIG3	0x03	0xDC	1	1	0	1	1	1	0	0
LOFF	0x04	0×03	0	0	0	0	0	0	1	1
CH1SET	0×05	0×01	0	0	0	0	0	0	0	1
CH2SET	0×06	0×01	0	0	0	0	0	0	0	1
CH3SET	0×07	0×01	0	0	0	0	0	0	0	1
CH4SET	0×08	0×01	0	0	0	0	0	0	0	1
CH5SET	0×09	0×01	0	0	0	0	0	0	0	1
CH6SET	0×0A	0×01	0	0	0	0	0	0	0	1
CH7SET	0×0B	0×01	0	0	0	0	0	0	0	1
CH8SET	0x0C	0×01	0	0	0	0	0	0	0	1
RLD_SENSP	0x0D	0×00	0	0	0	0	0	0	0	0
RLD_SENSN	0×0E	0×00	0	0	0	0	0	0	0	0
LOFF_SENSP	0×0F	0×FF	1	1	1	1	1	1	1	1
LOFF_SENSN	0×10	0×02	0	0	0	0	0	0	1	0
LOFF_FLIP	0×11	0x00	0	0	0	0	0	0	0	0
LOFF_STATP	0×12	0×FF	1	1	1	1	1	1	1	1
LOFF_STATN	0×13	0×06	0	0	0	0	0	1	1	0
GPIO	0×14	0×00	0	0	0	0	0	0	0	0
PACE	0×15	0×00	0	0	0	0	0	0	0	0
RESP	0×16	0x00	0	0	0	0	0	0	0	0
CONFIG4	0×17	0x02	0	0	0	0	0	0	1	0
WCT1	0×18	0×0A	0	0	0	0	1	0	1	0
WCT2	0×19	0×E3	1	1	1	0	0	0	1	1

Refresh Registers

(automatically updates if coming from another page)

Figure 32. Device Registers Settings


## 6 ADS1298R Analysis Tools

Under the *Analysis* tab in the ADS1298R GUI software, there are four different analysis tools shown that enable a detailed examination of the signals selected by the front-end MUX:

- Scope
- Analysis
- Histogram
- FFT

These tools are detailed in the following subsections.

## 6.1 Scope Tab

## 6.1.1 Using the Analysis→Scope Tool

The Scope tool (available under the *Analysis* tab) is a very useful means of examining the exact amplitude of the measured input signals from each channel. Additionally, users can determine the noise contribution from each channel at a given resolution, and review the sampling rate, the PGA gain, and the input signal amplitude. Figure 33 illustrates the Scope tool features.



Figure 33. Scope Tool Features



#### 6.1.2 Scope Analysis Button

In the *Scope Analysis* tab, as Figure 34 illustrates, the different noise levels are displayed when the MUX is selected as *Input Short*, PGA gain is set to 6 (default), and the sample rate is set to 500 samples per second (SPS).

🏘 Scope Analys	is								>
	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8	T
Mean (V)	206.80E-6	-437.53E-6	-242.57E-6	-17.42E-6	-82.47E-6	-113.94E-6	-248.07E-6	-247.12E-6	7
Vrms	606.39E-9	574.31E-9	564.89E-9	541.24E-9	598.63E-9	561.82E-9	547.32E-9	581.58E-9	-
Vpp	4.20E-6	3.62E-6	3.43E-6	3.34E-6	3.86E-6	3.62E-6	3.24E-6	3.67E-6	
Vpp	4.20E-6	3.62E-6	3.43E-6	3.34E-6	3.86E-6	3.62E-6	3.24E-6	3.67E-6	_
								Сюсе	
								CIUSE	
									_

Figure 34. Scope Analysis Tab (Noise Levels for Each Channel Shown)

#### 6.1.3 Waveform Examination Tool

The waveform examination tool allows the user to zoom in either on all channels simultaneously or on a single channel. Figure 35 shows an example of the waveform examination tool with the magnifying glass zoomed in on Channel 2. In this case, the tool makes it much easier to determine that the noise seen on the ECG waveform is a result of 50Hz/60Hz line cycle noise.



Figure 35. Zoom Option on the Waveform Examination Tool



## 6.1.4 ECG Display Tool

The ECG display tool is located under the Analysis  $\rightarrow$  ECG Display tab.

## 6.1.4.1 Using the Analysis→Scope Tool

This tool allows the user to examine the input signal according to the different lead configurations. For a detailed description of the lead configurations, see Table 26 in Section 7.2. Figure 36 shows Leads I-III and the Augmented Lead outputs with the input MUX configured in *Normal Electrode* mode. Figure 36 also shows numerical annotations 1 to 4, which highlight the different features of this tool. These features are described in detail in the following subsections.



Figure 36. ECG Display Tab Showing LEAD I-III and Augmented Leads

### Plot Set Feature: 1

The Plot Set feature, indicated by Box 1 in Figure 36, allows the user to change the visual selection between the Leads I-III and the augmented leads, and the chest leads.

### **ECG Separation Feature: 2**

The ECG Separation feature (marked as Box 2) toggles the vertical distance between the input plots. This capability is useful when ECG signals are large and require more separation to avoid overlap, or to collapse the range between signals when the ECG signals are small.

### **Notch Filter Feature: 3**

The Notch Filter is a finite-impulse response (FIR) filter that may be enabled only at sample rates greater than 500SPS. To activate this feature, check the box *Filter Enable* and select the notch frequency of either 50Hz or 60Hz.



## ECG Signal Zoom Feature: 4

The ECG Signal Zoom feature, similar to the waveform examination tool, may be enabled by moving the mouse (which appears as a magnifying glass) over the lead of interest and clicking on it. As Figure 37 illustrates, a pop-up box will appear with the signal analysis options in the lower right-hand corner. Using these options allows a much closer zoom on the waveform.



Figure 37. ECG Signal Zoom Feature for Lead 1





The ECG Signal Zoom feature may also be used on all six leads, as shown in Figure 38.

Figure 38. ECG Signal Zoom Feature for Six Leads

## 6.2 Histogram Tool

The Histogram tool is located under the Analysis $\rightarrow$  Histogram tab.

#### 6.2.1 Using the Analysis→Histogram Tool

The Analysis→Histogram tool is used primarily to see the bin separation of the different amplitudes of the ECG waveform harmonics. Figure 39 illustrates the histogram output for a 12-lead signal. The same ECG Signal Zoom analysis may be used on the histogram plots for a more detailed examination of the amplitude bins.



Figure 39. Histogram Bins for 12-Lead ECG Signal

Figure 40 describes how clicking on the **Histogram Analysis** button (at the bottom of the screen in Figure 39) yields the mean,  $V_{RMS}$ , and  $V_{PP}$  channel amplitude bins.

PHistogram Analysis									
	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8	ľ
Mean (V)	727.79E-6	189.47E-6	165.72E-6	508.89E-6	472.35E-6	429.38E-6	260.73E-6	248.17E-6	
Vrms	155.08E-6	91.03E-6	129.77E-6	177.65E-6	217.76E-6	199.50E-6	185.8/E-6	137.15E-6	
_ vpp	1.22E-3	700.02E-0	1.10E-3	1.746-3	1.90E-3	1.01E-3	1.556-5	1.10E-3	i.
									-
								Close	





# 6.3 FFT Tool

The FFT tool is located under the *Analysis* $\rightarrow$ *FFT* tab.

## 6.3.1 Using the Analysis→FFT Tool

The Analysis→FFT tool allows the user to examine the channel-specific spectrum as well as typical figures of merit such as SNR, THD, ENOB, and CMRR. Each feature is numbered below and described in detail in the following subsections. Figure 41 illustrates an Analysis→FFT plot for a normal electrode configuration.



Figure 41. Analysis→FFT Graph of Normal Electrode Configuration

## **Coherent Frequency Calculator: 1**

Coherent sampling in an FFT is defined as  $F_{AIN}/F_{SAMPLE} = N_{WINDOW}/N_{TOTAL}$ , where:

- F<sub>AIN</sub> is the input frequency
- F<sub>SAMPLE</sub> is the sampling frequency of the ADS1298R
- N<sub>WINDOW</sub> is the number of odd integer cycles during a given sampling period
- N<sub>TOTAL</sub> is the number of data points (in powers of 2) that is used to create the FFT If the conditions for coherent sampling can be met, the FFT results for a periodic signal will be optimized. The *Ideal A<sub>IN</sub> Frequency* is a value that is calculated based on the sampling rate, such that the coherent sampling criteria can be met.

ADS1298R Analysis Tools



#### ADS1298R Analysis Tools

#### AC Analysis Parameters: 2

This section of the tool allows the user to dictate the number of harmonics, dc leakage bins, harmonic leakage bins, and fundamental leakage bins that are used in the creation of various histograms. Pressing the *Windowing* button, illustrated in Figure 42, allows the user to evaluate the FFT graph under a variety of different windows. Note that pressing the **Reference** button toggles between dBFS (decibels, full-scale) and dBc (decibels to carrier).

Number of Harmonics	$\left(\frac{h}{r}\right)_{6}$	Windowing	√ None
DC Leakage Bins	÷)5	P	Hanning Hamming
Harmarminc Leakage Bins	<u>(</u> )3	, in the second s	Blackman-Harris
Fundamental Leakage Bins	<u>/</u> 15		Exact Blackman Blackman
			Flat Top
-Coherent Frequency Cal	culator		4 Term B-Harris
Desired Martineses			7 Term B-Harris
Desired Ain Frequency	5160.000Hz		Low Sidelobe
Ideal Ain Frequen	cy 60.222222	Hz	

Figure 42. Analysis→FFT→AC Analysis Parameters: Windowing Options

### FFT Analysis: 3

Pressing the **FFT Analysis** button pulls up the window shown in Figure 43. This window can be useful because the different tabulated figures of merit can show more detailed information about the channel-to-channel noise.

	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8
SNR (dBFS)	-12.34	-15.84	-13.95	-10.83	-10.77	-10.56	-12.10	-13.52
5NRD(dB)	-12.64	-16.22	-14.39	-11.30	-11.07	-10.86	-12.44	-13.88
THD (dBc)	0.45	-3.71	-2.30	0.74	2.96	3.37	0.76	-1.50
SFDR (dBc)	5.72	2.26	4.51	6.75	8.43	8.69	6.02	3.25
ENOB	-2.39	-2.99	-2.68	-2.17	-2.13	-2.10	-2.36	-2.60
enob	-2.34	-2.92	-2.61	-2.09	-2.08	-2.05	-2.30	-2.54
# of Harmonics (SNR)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Worst Spur (dB)	17.11	14.01	10.90	0.97	10.15	0.17	16.76	6.92
2nd HD (dBc)	7.62	2.26	5.01	10.77	13.41	9.53	8.51	3.25
3rd HD (dBc)	5.72	3.88	4.51	6.75	9.03	18.37	9.14	6.22
4th HD (dBc)	8.68	3.37	6.87	7.63	10.15	10.50	6.02	10.24
5th HD (dBc)	8.01	4.70	6.96	8.58	10.74	12.12	8.60	9.03
Fundamental (dB)	-100.74	-101.21	-101.21	-101.39	-101.21	-100.47	-100.97	-101.76
PGA Setting	12	12	12	12	12	12	12	12
CMRR	165.70	161.35	161.37	150.92	159.06	149.57	164.26	155.70

Figure 43. Analysis→FFT→FFT Analysis: Input Short Condition



## User-Defined Dynamic Range: 4

This section enables the user to examine the SNR of a specific channel within a given frequency band defined by *Low Frequency* and *High Frequency*. The SNR displayed in this window will also show under the *Dynamic Range* heading as Figure 44 illustrates.



Figure 44. Changing the User-Defined Dynamic Range for Channel 1

## **Input Amplitude: 5**

This field is a user input that is important for accurately calculating the CMRR of each channel.

## Waveform Zoom Tool: 6

As with the Analysis, Histogram, and Scope tool, this zoom function allows a closer examination of the FFT at frequencies of interest, as shown in Figure 45.



Figure 45. FFT Plot Using Zoom Tool

## 7 Evaluation of Specific ECG Functions

**NOTE:** Before evaluating specific ECG functions, it is recommended that the user acquire data with inputs shorted internally. This configuration ensures that the board is operating properly.

By default, when the board is powered up, it sets the individual channels to an internal short with a data rate of 500SPS and a PGA gain of 6. Once the **Acquire** button is pressed, the Scope tab under the Tests tab should reflect input-referred  $V_{PP}$  values less than  $5\mu V_{PP}$ , as Figure 46 illustrates.

Scope Analys								
	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8
Mean (V)	205.86E-6	-437.44E-6	-245.42E-6	-21.38E-6	-82.34E-6	-113.51E-6	-246.04E-6	-247.09E-6
Vrms	645.85E-9	583.58E-9	554.97E-9	579.27E-9	575.02E-9	629.22E-9	555.44E-9	547.49E-9
Vpp	4.34E-6	3.72E-6	3.62E-6	3.81E-6	3.67E-6	3.86E-6	3.29E-6	3.29E-6
1 vhh	4.342-0	J.72E-0	J.02E-0	3.01E-0	3.072-0	3.00E-0	3.292-0	3.292-0
								Close

### Figure 46. Input Short Data for Two Seconds Sampled at 500SPS

# 7.1 Capturing 12-Lead ECG Signals

To capture signals from external inputs, configure the inputs of each channel to *Normal Electrode* as shown in Figure 47.

ower-down	PGA Gain	Channel Input			
Normal Operation	6	✓ Normal Electrode			
		Input Short			
		RLD Measurement			
hannel 1 Control Reg	ster (CH1SET)	MVDD	Channel 2 Control Reg	ister (CH2SET)	
Power-down	PGA Gain	Temperature Sensor	Power-down	PGA Gain	Channel Input
Normal Operation	6	Test Signal	Normal Operation	6	Normal Electrode
		RLD Positive Electrode Driver	· · · · · · · · · · · · · · · · · · ·		
hannel 3 Control Reg	ister (CH3SET)	RLD Negative electrode Driver	Channel 4 Control Reg	ister (CH4SET)	
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input
Normal Operation	6	Normal Electrode	Normal Operation	6	Normal Electrode
Ihannel 5 Control Reg	ister (CH5SET)		Channel 6 Control Reg	ister (CH6SET)	
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input
Normal Operation	6	Normal Electrode	Normal Operation	6	Normal Electrode
Thannel 7 Control Reg	ister (CH7SET)		Channel 8 Control Reg	ister (CH8SET)	
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input
			Maxmal Onevation	6	Newson J. Electron de

## Figure 47. MUX Configured with All Inputs Set to Normal Electrode

The 10 ECG electrodes from the Fluke simulator are provided through the DB15 connector (J1). Refer to Section 9.3 for the ECG cable details. The ECG electrode signals are passed through a single pole RC filter followed by the lead configuration. For ECG signal processing, the electrode signals are routed through J5 to the ADS1298R input. The signal path in the board can be chosen by jumper settings, depending on the application.

## 7.2 Lead Derivation

The EVM is configured to generate 12 leads of ECG signals from the 10 electrodes using the eight channels of the ADS1298R. Two of the limb leads and the six chest leads are computed purely in the analog domain (Leads I, II, V1, V2, V3, V4, V5 and V6). The augmented leads and Lead III are computed digitally. The channel assignments are described in Table 26.

ADS1298R Input Channels	Derived Lead <sup>(1)</sup>
1	V6 = V6 – WCT
2	LI = LA - RA
3	LII = LL – RA
4	V2 = V2 – WCT
5	V3 = V3 – WCT
6	V4 = V4 – WCT
7	V5 = V5 – WCT
8	V1 = V1 – WCT
4 5 6 7 8	

## Table 26. Lead Generations

<sup>(1)</sup> WCT = (LA + RA + LL)/3

# 7.3 Wilson Center Terminal (WCT)

The Wilson Center Terminal voltage is internally generated by the ADS1298R device. The device gives register bit controls so that any of the eight inputs (CH1P to CH4P, CH1M to CH4M) can be routed to the three integrated amplifiers to generate the WCT signal.

The ADS1298R is configured for 12-lead ECG inputs, with the limb electrodes connected as shown in Table 26. During EVM power-up, the firmware sets up the register bits such that the CH2P, CH2M, and CH3P (RA, LA, LL) bits are routed to the internal buffers. This arrangement creates the (RA + LA + LL)/3 signal at the WCT pin. This signal is routed back to the negative inputs of channels 1, 3 to 8 by setting the jumper J3 to the 2-3 position.

# 7.4 Measured 12 -Lead ECG Outputs

**NOTE:** The current firmware does not support digital dc removal (high-pass filtering). Data can be saved and post-processed with a digital high-pass filter and a 60Hz notch filter for analysis.

Data presented in this section are captured for two amplitudes. The 5mV ECG signal is a widely-used test condition that is reliable enough for doing basic QRS detection. Data with a 50 $\mu$ V ECG signal (the lowest that the Fluke simulator can generate) shows the full capability of the ADS1298R integrated front-end. Graphs in this section show the measured ECG signal under the following conditions:

- 1. DC-coupled input with RLD (5mV ECG signal)
- 2. DC-coupled input with RLD and bipolar supply (1mV ECG signal)
- 3. DC-coupled input with RLD (50µV ECG signal, zoomed in on one channel)

Evaluation of Specific ECG Functions



#### Evaluation of Specific ECG Functions

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# DC-Coupled with Right Leg Drive: 5mV ECG Signal

Figure 48 shows the acquisition of a 5mV ECG signal with a dc-coupled input.



Figure 48. Acquisition of 5mV ECG Signal with DC-Coupled Inputs



## DC-Coupled with Right Leg Drive: 1mV ECG Signal

Figure 49 illustrates the acquisition of a 1mV ECG signal with dc-coupled inputs.



Figure 49. Acquisition of 1mV ECG Signal with DC-Coupled Inputs



## DC-Coupled with Right Leg Drive: 50µV ECG Signal

Acquisition of a 50µV ECG signal with a dc-coupled inputs is shown in Figure 50.





Figure 50 shows the output measured a 50µV ECG input signal measured in a Lead I configuration. This signal is the minimum ECG signal amplitude that the Fluke Medsim simulator can generate. It can be seen that the ADS1298R integrated front end can resolve ECG signals down to 50µV. With the default right-leg drive (RLD) loop in the EVM, the power line (50Hz/60Hz) interference is limited to approximately  $20\mu V_{PP}$ . This interference can be removed by using a 50Hz/60Hz digital notch filter. Alternatively, the RLD loop can be further optimized to reduce the interference as well.



## 7.5 Right Leg Drive

Evaluation of Specific ECG Functions

Typically, the RLD is implemented by choosing the average of RA, LA, and LL. The ADS1298R, however, offers full flexibility by letting the user select any combination of the electrodes to generate the RLD. Refer to the ADS1298R data sheet for more details.

The reference voltage for the on-chip right leg drive can be driven externally. The on-chip voltage is set to mid-supply. If the application requires the common mode to be set to any other voltage, this configuration can be accomplished by setting the appropriate bit in the Configuration 3 Register. The external RLDREF voltage is set by resistor R1 and adjustable resistor R2.

By default at power-up, the firmware sets all the registers needed for proper RLD operation. In the event of a reset signal, the register values return to the device defaults. In such a scenario, the following procedure can be applied to reactivate the RLD circuitry.

Step 1. Verify that the input multiplexer is set to the Normal Electrode mode, as Figure 51 shows.

annei Control Reg	isters				
alobally Set Channels					
Power-down	PGA Gain	Channel Input	Globally	y set to	
Normal Operation	6	Normal Electrode	Normal	Electrode	
Thannel 1 Control Reg	jister (CH1SET)	L	Channel 2 Control Rec	ister (CH2SET)	
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input
Normal Operation	6	Normal Electrode	Normal Operation	6	Normal Electrode
Channel 3 Control Reg	gister (CH3SET)		Channel 4 Control Reg	jister (CH4SET)	
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input
Normal Operation	6	Normal Electrode	Normal Operation	6	Normal Electrode
Channel 5 Control Reg	gister (CH5SET)		Channel 6 Control Reg	jister (CH6SET)	
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input
Normal Operation	6	Normal Electrode	Normal Operation	6	Normal Electrode
Channel 7 Control Reg	gister (CH7SET)		Channel 8 Control Reg	jister (CH85ET)	
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input
Normal Operation	6	Normal Electrode	Normal Operation	6	Normal Electrode

# Figure 51. Settings for Normal Electrode

Step 2. Turn on the RLD buffer and set the internal RLD reference; refer to Figure 52.

Configuration Register 3 (CONFIG	3)			
Power-down Reference Buffer	Reference Voltage	RLD Measurement	RLDREF Signal Source	RLD Buffer Power
Enabled	VREFP = 2.4V	RLD_IN Routed	RLDREF = AVDD/2	Enabled

# Figure 52. Configuring RLDREF and RLD Buffer



Step 3. Select the electrodes to be chosen for the RLD loop. In this case, the RA, LA, and LL signals are used (as Figure 53 shows).



Figure 53. Setting Up the RLD Loop

Once these steps are completed, measure and verify that the voltage on either side of R34 is close to mid-supply. This measurement confirms whether the RLD loop is functional.

Apart from the RLD signal, the ADS1298R also offers three options to drive the cable shield. The ECG cable shield signal can be connected to either the in-phase or out-of-phase RLD signal, or the board AGND using jumpers JP19 and JP21. Table 27 summarizes these options.

Table 27. RLD Jumper Options

ECG Cable ELEC_SHD signal	JP19	JP21
AGND	1-2	Don't Care
RLD (0: In phase)	2-3	2-3
RLD (180: Out of phase)	2-3	1-2

The on-chip RLD signal can be fed back into the ADS1298R by shorting JP1. This RLD signal can then be sent to the ADC (to measure for debug purposes) or to other electrodes for driving (to change the reference drive in case the RL electrode falls off). Refer to the <u>ADS1298R product data sheet</u> for additional details.

# 7.6 Lead-Off Detection

The ADS1298R provides multiple schemes to implement the lead-off detection function. These techniques include current source dc, current source ac, pull-up resistor dc, and pull-up resistor ac lead-off detection options. Refer to the ADS1298R product data sheet for additional details.

While attempting to use the lead-off detection, care must be taken to analyze the input signal. If the input signal is dc-coupled, the dc lead-off scheme can be used. If the input signal is ac-coupled, the ac lead-off scheme must be used. When using the dc lead-off scheme, be sure to turn on the RLD loop to set the input common-mode before activating lead-off detection.

The EVM gives flexibility to exercise any of the above schemes. The two schemes discussed in the following sections show a typical sequence to activate the current source dc lead-off circuitry and V/R mode ac lead-off circuitry.

#### 7.6.1 DC Lead-Off

At board power-up, the firmware sets the appropriate registers so that dc lead-off is selected. In the event of a reset signal, the register values default to the device default settings. In such a scenario, follow this procedure to reactivate the lead-off circuitry.

Evaluation of Specific ECG Functions

- Step 1. Make sure the input is dc-coupled and that the RLD circuit is operational, as explained in Section 7.5.
- Step 2. Choose the lead-off scheme by setting the respective bits in the LOFF register (in the LOFF control tab). Select the *DC Lead-Off Detect, 6.25nA, Current Source* scheme, and set the comparator threshold to 95%. Select the appropriate inputs for lead-off detection by clicking the bits of the LOFF\_SENSP and LOFF\_SENSM Registers. The LOFF tab should appear as shown in Figure 54.

Lead-Off Control Register (LOFF)									
Comparator Threshold	Lead-off Det	ection Mode	Lead-off Cu	Lead-off Current Magnitude Lead-o		ead-off Frequency			
Positive - 95% : Negative - 5%	Current Mod	le	6nA	nA		DC Lead-off Detection ON			
7									
-Lead-Off Detection and Current Direction	on Control Rec	isters —							
Set All LOFFP Bits	LOFFP8	LOFFP7	LOFFP6	LOFFP5	LOFFP4	LOFFP3	LOFFP2	LOFFP1	
ENIARIED	$\bigcirc$	$\bigcirc$	0	0	0	0	0	$\bigcirc$	
ENMOLED	-		-			-			
L	ead Off Sense F	ositive Electrod	e						
Set All LOFFN Bits	LOFFN8	LOFFN7	LOFFN6	LOFFN5	LOFFN4	LOFFN3	LOFFN2	LOFFN1	
DISABLED							$\bigcirc$		
L	ead Off Sense N	legative Electro	de						
Set All LOFF FLIP Bits	LOFF_FLIP8	LOFF_FLIP7	LOFF_FLIP6	LOFF_FLIP5	LOFF_FLIP4	LOFF_FLIP3	LOFF_FLIP2	LOFF_FLIP1	
	-	-	-	-	-	-	-		
DISABLED	9	9	-	-	-	-	9	9	
L	ead Off Current	Direction							

## Figure 54. Setting the LOFF Register Bits

Step 3. Turn on the lead-off comparator by setting the bit in the Configuration 4 Register in the Global Registers control tab, as Figure 55 shows.

Configuration Register 4 (CONFIG4)									
Respiration Frequency	Pulse Mode Enable	Lead-off Comparator Power-down							
64kHz	Disable	Enable							

### Figure 55. Configuring the Lead-Off Comparator

Step 4. The software has an option where the LOFF\_STATP and LOFF\_STATM Registers are continuously polled (set the *Read Status Registers* switch as shown in Figure 56). This option allows the user to see the lead-off detection scheme work in real time.



#### Evaluation of Specific ECG Functions

Set All LOFFP Bits	LOFFP8	LOFFP7	LOFFP6	LOFFP5	LOFFP4	LOFFP3	LOFFP2	LOFFP1
ENABLED	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$
	Lead Off Sense	Positive Electro	de					
Set All LOFFN Bits	LOFFN8	LOFFN7	LOFFN6	LOFFN5	LOFFN4	LOFFN3	LOFFN2	LOFFN1
ENABLED	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$
Lead Off Sense Negative Electrode								

Figure 56. Setting the Lead-Off Bits to Work in Real Time

When the simulator is disconnected from the DB15 connector, the LOFF\_STAT registers automatically update. They may be viewed in real time by clicking on the **Show/Poll Lead Off Status** button, as shown in Figure 57. The LOFF\_STATM (bit7 to bit2) are driven by the WCT amplifiers and thus do not show a LEAD OFF status.



🏘 Lead-Off Status Registers 🛛 🗙						
Positive Electrode		Negative Electrode				
LEAD OFF	IN8×	LEAD ON				
LEAD OFF	IN7×	LEAD ON				
LEAD OFF	IN6×	LEAD ON				
LEAD OFF	IN5×	LEAD ON				
LEAD OFF	IN4×	LEAD ON				
LEAD OFF	IN3×	LEAD OFF				
LEAD OFF	IN2×	LEAD OFF				
LEAD OFF	IN1×	LEAD ON				
		-				

Figure 57. Lead-Off Status Registers

## 7.6.2 AC Lead-Off Detection

Follow these steps to configure ac lead-off detection.

- Step 1. If dc-coupled input is used, turn on the RLD loop as explained in Section 7.5.
- Step 2. Choose the lead-off scheme by setting the bits in the LOFF register (in the LOFF control tab). Select the *AC Lead-Off Detect at f<sub>s</sub>/4, V/R mode* scheme. The state of the other bits in the register does not matter. Select all the channels for lead-off detection by clicking the respective bits of the LOFF\_SENSP and LOFF\_SENSM Registers. The LOFF tab should now appear as shown in Figure 58.

Lead-Off Control Register (LOFF)

Comparator Threshold	Lead-off Detection Mode	Lead-off Current Magnitude	Lead-off Frequency
Positive - 95% : Negative - 5%	Current Mode	6nA	AC Lead-off Detection at f(DR)/4

### Figure 58. Setting the Lead-Off Register for AC Lead-Off Detection

Step 3. Once the frequency of the ac lead-off is determined, the data rate must be chosen to be four times the lead-off frequency. As an example, a data rate of 8kHz is chosen by setting the DR bit in the Configuration 1 Register in the Global Registers control tab.

Once these steps are completed, data can be captured with the patient simulator connected. A typical time domain waveform (65,536 points) is shown in Figure 59.



### Figure 59. AC Lead-Off Time Domain Waveform for Lead I (DR = 8kSPS)

- Step 4. Post-processing must be done to extract the lead-off signal and the ECG signal from the waveform. In future versions of the ADS1298R firmware, it is planned to incorporate post-processing filters. In the meantime, the raw channel data can be saved to a file by enabling the *Save Sorted Raw Channel (V)* option in the Print Options tab and pressing the *Print to File* button. Post-processing can be done using tools such as MATLAB<sup>®</sup>.
- **NOTE:** The ADS1298R does **not** include software to extract the ECG signal from the lead-off signal.



#### 7.7 Pace Detection

The ADS1298R supports data rates up to 32kSPS to allow for software pace detection, which typically requires a data rate of at least 8kSPS.

NOTE: The ADS1298R does not include software PACE detection algorithms.

The ADS1298R provides the user the flexibility of doing hardware pace detection with external circuitry. Pace detection can be done simultaneously on two channels: one from the odd channels and one from the even channels. Refer to the <u>ADS1298R product data sheet</u> for additional details. To turn on the Pace buffer and select the channels, set the PACE Register from the PACE tab as shown in Figure 60. The PGA outputs of the selected channels are available at connectors J5, pins 1 and 2.

PACE Detect Register (PACE)						
PACE_OUT2 Odd	PACE_OUT1 Even	Pace Detect Buffer Enable				
CH1	CH2	Buffer On				

Figure 60. Setting the Pace Register

Figure 61 shows an example waveform created by a Fluke Medsim 300B processed by the ADS1298R at a data rate of 8kSPS. Using higher data rates increases power consumption because all channels must sample at this data rate simultaneously; thus, the PACE buffers offer the flexibility to process PACE signals separately from the ADS1298R.



Figure 61. Example Processing of PACE Detect with ECG Waveform



# 8 Evaluation of the ADS1298R Respiration Function

# 8.1 Introduction

The ADS1298R allows for the measurement of respiration rate based on the principle of impedance pneumography. The key concept of this approach is to measure the change in impedance of the thoracic cavity during breathing (respiration). The ADS1298REVM provides two ways to test the respiration circuitry: first, using onboard circuitry; and second, using a patient simulator with respiration outputs. This section describe both approaches.

# 8.2 Testing with Onboard Circuitry

## 8.2.1 Hardware Configuration

The ADS1298REVM has onboard circuitry to test a respiration circuit. A simplified diagram illustrating only the respiration portion of the circuit is shown in Figure 62; the onboard circuitry to generate the respiration signal is within the red dotted box. By default, jumpers JP34 and JP35 connect the onboard circuitry for respiration evaluation. R77 models the baseline impedance of the thoracic cavity. This component is a surface-mount resistor located on the underside of the board; it can be changed if desired. R78 and R79 model the cable resistance (typically 1k $\Omega$  for patient monitoring). Capacitors C97 and C98 are used to model the parasitic capacitance that may be present when real cables are used. Capacitors C113 and C114 serve as a secondary means to prevent a single fault (such as a shorted C112 capacitor from a carrier generator) from causing excessive dc currents through the electrodes.

The parameter of interest is the change in impedance during breathing. This change in impedance is accomplished by switching  $1M\Omega$  impedance in parallel to R77 using an analog switch, U11. Two  $1M\Omega$  resistors (R82 and R83) have been added to provide a dc bias to this switch. Switch U11 must have a control signal that toggles between AVSS and AVDD at the desired respiration frequency. This control signal can be fed from either an onboard signal source or an external function generator via JP36.



Figure 62. Respiration Evaluation with Onboard Circuitry



#### Evaluation of the ADS1298R Respiration Function

The remainder of the circuit is necessary for respiration measurements with both the onboard circuitry and patient simulator. Resistors R96 and R97 limit the amount of ac current that flows into the body. Capacitors C108 and C109 block any dc current from flowing into the body from the transmission side. Capacitors C99 and C100 serve the same purpose on the receiver side. The respiration capability is available on Channel 1. The respiration signals are routed to Channel 1 when the two shunts on JP33 are in the respective default locations, shorting pins 5-6 and 7-8 as shown in Figure 62.

#### 8.2.2 Software Configuration

The Respiration Control Register works in conjunction with Configuration Register 4 (CONFIG4). Certain bit changes must be done in order to activate the respiration circuitry of the ADS1298R. The respiration frequency should be set to 32kHz in Configuration Register 4 (refer to Figure 64).

For internal respiration with an internal clock, the channels must be configured to *Normal Electrode* and the gain should be set to 6, as shown in Figure 63.

	201L									Displaying Respiration (
,	Progress		Si	amples/OH						
500SP5	_		100% )]2	20000		ACQUERE	CONTINUOUS	$\subset$	Show/Poll Le	ad Off Status
	Global Channel Regist Configuration Register 1 High Resolution(Low Pow	ers (CONFIG1) ver Mode Dai	sy-chain/Multiple Readback Moo	de <u>CUKOUT Conn</u>	ection Output	Data Rate				Standby Reset Options
5	High Resolution Mode	Di	aisy Chain Mode	Output Disab	ied [[f(MOD	)/1024				Reset
9	Configuration Register 2	(CONFIG2)								Reset Mode
8	TEST Source Driven Externally	Test Signal A	Implitude Test Sign EFN//2.4 F(CUC)/2	nal Frequency 2021						C Device Defaults
5	Configuration Register 3	(CONFIG3)								K Programmed Def
и Б	Power-down Reference	Buffer Refer	ence Voltage RLD Measuren	ment RLDREF Sig	gnal Source RLI	D Buffer Power				
	Enabled	VRE	PP = 2.4V RLD_IN Rout	ed RLDREF =	AVDD/2 Er	nabled				
ŝ	Lead-Off Control Register	< 0.0PP)								
5	book off born official	1 (2011)								
	Comparator Threshold Positive - 95% : Negati	we - 5%	Lead-off Detection Mode Current Mode	Lead-off Curren	t Magnitude Le	ad-off Frequency XC Lead-off Detection	n ON			
	Comparator Threshold Positive - 95% : Negati Channel Control Regis Globaly Set Channels	ve - 5%	Lead-off Detection Mode	Lead-off Curren	t Magnitude Le	ad-off Frequency IC Lead-off Detectio	n ON			
vegster map	Comparator Threshold Positive - 95% : Negati Channel Control Regis Globaly Set Channels Power-down	ve - 5% sters	Lead-off Detection Mode Current Mode	Lead-off Curren	t Magnitude Le	ad-off Frequency IC Lead-off Detection	n ON			
Hegistermap Groot and Circle	Comparator Threshold Positive - 95% : Negati Channel Control Regis Globally Set Channels Power-down Normal Operation	Ne - 5% ders PGA Gen 6	Lead-off Detection Mode Current Mode	Lead-off Curren	t Magnitude Le	ad-off Frequency IC Lead-off Detection	n ON			
Register map	Comparator Threshold Positive - 95% : Negati Channel Control Regis Globaly Set Channels Power-down Normal Operation Channel 1 Control Regis	Aters PGA Gain 6 cter (CHISET)	Lead-off Detection Mode Current Mode	Lead-off Curren	t Magnitude Le	ad-off Frequency IC Lead-off Detection	n ON			
Kegstermap erto and Unite	Comparator Threshold Positive - 95% : Negati Channel Control Regis Globaly Set Channels Power-down Normal Operation Channel 1 Control Regis Power-down	PGA Gain PGA Gain PGA Gain PGA Gain	Lead-off Detection Node Current Mode	Lead-off Curren	t Magnitude Le D Global Set Channel Channel 2 Control I Power-down	ad-off Frequency IC Lead-off Detection is to configure all Ch Register (CH2SET) PGA Gain	n CN			
Hegister map	Comparator Threshold Positive - 95% : Negati Channel Control Regis Globally Set Channels Power-down Normal Operation Channel 1 Control Regis Power-down Normal Operation	PGA Gan 6 PGA Gan 6 PGA Gan 6	Lead-off Detection Mode Current Mode	Lead-off Current	Channel 2 Control I Power-down Normal Operation	ad-off Frequency CC Lead-off Detection is to configure all Ch Register (CH2SET) PGA Gain n 6	n ON			
	Comparator Threshold Positive - 95% : Negati Globally Set Channels Rower-down Normal Operation Channel 1 Control Regis Power-down Normal Operation Channel 3 Control Regis	PGA Gain 6 cters cter (CHISET) PGA Gain 6 ster (CHISET)	Lead-off Detection Node Current Mode	Lead-off Current	t Magnitude Le D Global Set Channel Channel 2 Control I Power-down Normal Operation Channel 4 Control I	ad-off Frequency IC Lead-off Detection is to configure all Ch Register (CH2SET) PGA Gain 5 6 Register (CH4SET)	Channel Input			
	Comparator Threshold Positive - 95% : Negati Globally Set Channels Rower-down Normal Operation Channel 1 Control Regis Power-down Normal Operation Channel 3 Control Regis Power-down	PGA Gen           # </td <td>Lead-off Detection Node Current Mode Chernel Input Normal Electrode Channel Input Normal Electrode</td> <td>Lead-off Current</td> <td>t Magnitude Le Global Set Channel Channel 2 Control I Power-down Normal Operation Channel 4 Control I Power-down</td> <td>ad-off Frequency CC Lead-off Detection is to configure all Ch Register (CH2SET) PGA Gain 6 Register (CH3ET) PGA Gain</td> <td>Channel Input</td> <td></td> <td></td> <td></td>	Lead-off Detection Node Current Mode Chernel Input Normal Electrode Channel Input Normal Electrode	Lead-off Current	t Magnitude Le Global Set Channel Channel 2 Control I Power-down Normal Operation Channel 4 Control I Power-down	ad-off Frequency CC Lead-off Detection is to configure all Ch Register (CH2SET) PGA Gain 6 Register (CH3ET) PGA Gain	Channel Input			
Hegister map   we'ld and Ultra	Comparator Threshold Positive - 95% : Negati Globally Set Channels Rower-down Normal Operation Channel 1 Control Regis Power-down Normal Operation Channel 3 Control Regis Power-down Normal Operation	PGA Gen           # </td <td>Lead-off Detection Node Current Mode Chernel Input Normal Electrode Channel Input Normal Electrode</td> <td>Lead-off Current</td> <td>t Magnitude Le Channel 2 Control I Power-down Normal Operation Channel 4 Control I Power-down Normal Operation</td> <td>ad-off Frequency CC Lead-off Detection is to configure all Ch Register (CH2SET) PGA Gain 6 Register (CH3ET) PGA Gain 6</td> <td>Channel Input Normal Electrode</td> <td></td> <td></td> <td></td>	Lead-off Detection Node Current Mode Chernel Input Normal Electrode Channel Input Normal Electrode	Lead-off Current	t Magnitude Le Channel 2 Control I Power-down Normal Operation Channel 4 Control I Power-down Normal Operation	ad-off Frequency CC Lead-off Detection is to configure all Ch Register (CH2SET) PGA Gain 6 Register (CH3ET) PGA Gain 6	Channel Input Normal Electrode			
	Comparator Threshold Positive - 95% : Negati Globally Set Channels Rower-down Normal Operation Channel 1 Control Regis Power-down Normal Operation Channel 3 Control Regis Power-down Normal Operation Channel 3 Control Regis Power-down Normal Operation Channel 5 Control Regi	PGA Gen           0           ders           PGA Gen           0           ster (CHISET)           PGA Gan           5           ster (CHISET)           PGA Gan           6           ster (CHISET)           PGA Gan           6           ster (CHISET)           PGA Gan           6	Lead-off Detection Node Current Mode Chernel Input Normal Electrode Channel Input Normal Electrode Channel Input Normal Electrode	Lead-off Current	t Magnitude Le Channel 2 Control I Power-down Normal Operation Normal Operation Normal Operation Normal Operation Normal Operation	ad-off Frequency CC Lead-off Detection is to configure all Ch Register (CH2SET) PGA Gain 6 Register (CH4SET) PGA Gain 6 Register (CH4SET)	Channel Input Normal Electrode			
	Comparator Threshold Positive - 95% : Negati Channel Control Regis Globaly Set Channels Power-down Normal Operation Channel 1 Control Regis Power-down Normal Operation Channel 3 Control Regis Power-down Normal Operation Channel 5 Control Regis Power-down	PGA Gen         6           #er (CHISET)         PGA Gan           6         6           ster (CHISET)         PGA Gan           6         6           ster (CHISET)         PGA Gan           6         6           ster (CHISET)         PGA Gan           6         6	Lead-off Detection Node Current Mode Channel Input Normal Electrode Channel Input Normal Electrode Channel Input Normal Electrode	Lead-off Current	t Magnitude Le Channel 2 Control I Power-down Normal Operation Normal Operation Normal Operation Channel 6 Control I Power-down	ad-off Frequency CC Lead-off Detection is to configure all Ch PGA Gain 6 Register (CHSET) PGA Gain 6 Register (CHSET) PGA Gain 6	Channel Input Normal Electrode Channel Input Normal Electrode			
	Comparator Threshold Positive - 95% : Nepati Channel Control Regis Globaly Set Channels Power-down Normal Operation Channel 1 Control Regis Power-down Normal Operation Channel 3 Control Regis Power-down Normal Operation Channel 5 Control Regis Power-down Normal Operation	PGA Gen         6           Rer CH1SET)         PGA Gen           6         6           ster (CH3ET)         PGA Gen           6         6	Lead-off Detection Node Current Mode Chernel Input Normal Electrode Channel Input Normal Electrode Channel Input Normal Electrode	Lead-off Current	t Magnitude Le Channel 2 Control I Poser-down Normal Operation Channel 4 Control I Poser-down Normal Operation Channel 6 Control I Poser-down Normal Operation	Ad-off Frequency CC Lead-off Detection is to configure all Ch Register (CH2SET) PGA Gain 6 Register (CH4SET) PGA Gain 6 Register (CH4SET) PGA Gain 6	Channel Input Normal Electrode Channel Input Normal Electrode			
	Comparator Threshold Positive - 95% : Negati Channel Control Regis Globaly Set Channels Power-down Normal Operation Channel 1 Control Regis Power-down Normal Operation Channel 3 Control Regis Power-down Normal Operation Channel 5 Control Regis Power-down Normal Operation Channel 7 Control Regis	PGA Gen         6           ders         6           der (CH1SET)         PGA Gan           6         6           ster (CH3ET)         PGA Gan	Lead-off Detection Node Current Mode Chennel Input Normal Electrode Channel Input Normal Electrode Channel Input Normal Electrode Channel Input Normal Electrode	Lead-off Current	t Magnitude Le Channel 2 Control I Poser-down Normal Operation Channel 6 Control I Poser-down Normal Operation Channel 6 Control I Poser-down Normal Operation Channel 8 Control I	ad-off Frequency CC Lead-off Detection is to configure all Ch Register (CH2SET) PGA Gain m 6 Register (CH4SET) PGA Gain m 6 Register (CH4SET) PGA Gain m 6 Register (CH4SET)	Channel Input Channel Input Normal Electrode Channel Input Normal Electrode			
	Comparator Threshold Positive - 95% : Nepati Globaly Set Channels Rower-down Normal Operation Channel 1 Control Regis Power-down Normal Operation Channel 3 Control Regis Power-down Normal Operation Channel 5 Control Regis Power-down Normal Operation Channel 7 Control Regis Power-down	PGA Gen         6           ders         6           der (CH1SET)         PGA Gan           6         6           ster (CH5ET)         PGA Gan           6         6           ster (CH5ET)         PGA Gan           6         6           ster (CH5ET)         PGA Gan           6         6	Lead-off Detection Node Current Mode Channel Input Normal Electrode Channel Input Normal Electrode Channel Input Normal Electrode	Lead-off Current GnA	t Magnitude Le Channel 2 Control I Power-down Normal Operation Channel 4 Control I Power-down Normal Operation Channel 6 Control I Power-down Normal Operation Channel 8 Control I Power-down	ad-off Frequency CC Lead-off Detection is to configure all Ch PGA Gain b 6 Register (CH2SET) PGA Gain b 6 Register (CH5SET) PGA Gain b 6 Register (CH5SET) PGA Gain b 6	Channel Input Channel Input Normal Electrode Channel Input Normal Electrode Channel Input Normal Electrode			

Figure 63. Global and Channel Specific Register Settings for Respiration



The Respiration Control Register must be configured as shown in Figure 64.

5005P5	Progress Samples/CH 100% 20000 ACQUIRE CONTINUOUS Show(	Poll Lead Off Status
Register Map GPIO and ONER Registers LOPF and RLD Channel Registers	General-Purpose I/O Register (GPIO)	Reset Options Reset Option Reset Node Programmed Def
	espiración requency Puse mode Ladore Lead-or Comparación Power-down ISintz Disable Enable	
	spiration Control Register (RESP)	
	spiration Demodulation Respiration Modulation VRDP Respiration Phase Respiration Control nable Enable VREPP 112.5 deg Int. Resp. with Int. CLK	
L .	son Center Terminal and Augmented Lead Register (WCT1)	
	aft Leg (aVF) to CH6 Left Arm (aVL) to CH5 Right Arm (aVR) to CH7 Right Arm (aVR) to CH4 Power-down WCTA WCT Amplifier Channel A	
	Disable Disable Disable Disable Powered on CH2 Positive Input	
	son Center Terminal Redister (WCT2)	
	wer-down WCTB Power-down WCTC WCT Analifier B WCT Analifier C	

Figure 64. Respiration Register Settings for Internal Respiration Measurements

Next, switch U11 must be toggled at the desired respiration frequency by applying a square wave via JP36. An onboard MSP430G2121 is provided to give approximately 0.1Hz through 0.5Hz. The MSP430 circuitry is selected when JP36 is loaded with a shunt jumper that shorts pins 1-2 (default). An external function generator can also be used for this purpose by applying a signal to SMA connector J6 and moving the shunt jumper on JP36 to cover pins 2-3. Data can be acquired by clicking on the *Acquire* tab. Figure 65 shows the results for a 0.5Hz toggling of the switch.

The expected dc output can be calculated using Equation 2.

$$DC_V = \frac{R77 + R78 + R79}{R96 + R97 + R77 + R78 + R79} \bullet (VREFP - VREFM)$$
$$= \frac{0.33k + 1k + 1k}{40k + 40k + 0.33k + 1k + 1k} \bullet 2.4 = 67.9mV$$

(2)



Evaluation of the ADS1298R Respiration Function

The expected peak-to-peak output as a result of the impedance change can be calculated with Equation 3; this value is the current flowing through the body:

$$I_{B} = \frac{VREFP - VREFM}{R77 + R78 + R79 + R96 + R97} = \frac{2.4}{82.33k} = 29.15\mu A$$
(3)

The  $\Delta$  impedance and peak-to-peak output can be calculated with Equation 4 and Equation 5.  $\Delta R = R77 - R77 \parallel R76 = 330 - 329.89 = 0.11\Omega$ 

$$\Delta V = \Delta R \cdot I_{B} = 0.11 \cdot 29.15 = 3.2 \mu V$$

(5)

(4)

The results shown in Figure 65 are taken using a data rate of 500SPS. To obtain better resolution, these results must be low-pass filtered.



Figure 65. Channel 1 & Impedance Measurement





## Figure 66 shows the result after the signal has been processed through a 2Hz low-pass filter.

Figure 66. Results After Low-Pass Filtering



## 8.3 Testing with Patient Simulator

## 8.3.1 Hardware Configuration

The output from any typical patient simulator can be directly fed into the DB15 connector. Figure 67 illustrates the connection with Fluke MedSim 300B simulator used as an example. The shunts on jumpers JP34 and JP35 should be moved from the respective default positions (shorting pins 1-2) so that these components now short pins 2-3.



Figure 67. Respiration with Fluke Simulator



## 8.3.2 Software Configuration

We then must write to the following registers before we take any data. Under the *ADC Register, Channel Registers* tab, the Global Channel Registers should be configured as shown in Figure 68.

High Resolution/Low Power Mode	Daisy-chain/Multip	le Readback Mode	CLKOUT Connection	Output Data Rate	
High Resolution Mode	Daisy Chain Mode	9	Output Disabled	f(MOD) /1024	
onfiguration Register 2 (CONFIG2	)				
TEST Source Test Si Generated Internally (VREF	gnal Amplitude P-VREFN)/2.4	Test Signal	Frequency 21		
Configuration Register 3 (CONFIG3	)				
Power-down Reference Buffer	Reference Voltage	RLD Measureme	nt RLDREF Signal Source	e RLD Buffer Power	
Enabled	VREFP = 2.4V	RLD_IN Routed	RLDREF = AVDD/2	Enabled	
ead-Off Control Register (LOFF)					
Comparator Threshold	Lead-off D	etection Mode	Lead-off Current Magnitud	e Lead-off Frequency	

Figure 68. Global Register Settings

The channels must be configured for Normal Electrode operation and the gain should be set to 6, as Figure 69 indicates.

annel Control Reg	isters							
ilobally Set Channels								
Power-down	PGA Gain	Channel Input	Set Global Set Channels to	Set Global Set Channels to configure all Channel X Control registers				
Normal Operation	6	Normal Electrode						
Channel 1 Control Reg	ister (CH1SET)		Channel 2 Control Reg	gister (CH2SET)				
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input			
Normal Operation	6	Normal Electrode	Normal Operation	6	Normal Electrode			
Channel 3 Control Reg	jister (CH3SET)		Channel 4 Control Reg	gister (CH4SET)				
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input			
Normal Operation	6	Normal Electrode	Normal Operation	6	Normal Electrode			
Channel 5 Control Reg	jister (CH5SET)		Channel 6 Control Reg	gister (CH6SET)				
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input			
Normal Operation	6	Normal Electrode	Normal Operation	6	Normal Electrode			
Channel 7 Control Reg	jister (CH7SET)		Channel 8 Control Reg	gister (CH8SET)				
Power-down	PGA Gain	Channel Input	Power-down	PGA Gain	Channel Input			
Name of Operation	6	Normal Electrode	Normal Operation	6	Normal Electrode			

## Figure 69. Channel-Specific Register Settings



Under the *ADC Register, GPIO and OTHER Registers* tab, the respiration frequency should be set to 32kHz in the CONFIG4 Register field as indicated in Figure 70. For internal respiration measurements with an internal clock, the respiration control register should be configured as shown in Figure 70.

Configuration Register 4 (CONFIG4)								
Respiration Frequency	Pulse Mode Enable	Lead-off Comparator	ad-off Comparator Power-down					
32kHz	Disable	Enable						
·								
Respiration Control Register	(RESP)							
Respiration Demodulation	Respiration Modulation	VREF	Respiration Phase	Respiration Control	1			
Enable	Enable	VREFP	112.5 deg	Int. Resp. with Int. CLK				

## Figure 70. Respiration Register Setting (for Internal Respiration)

There are several options that permit users to choose different base impedance ( $R_B$ ) and delta impedance ( $\Delta R$ ) on the simulator. For illustration purposes, a base impedance  $R_B$  of 500 $\Omega$  is chosen.

Figure 71 shows the results with  $R_B = 500\Omega$  and  $\Delta R = 1\Omega$ . The expected dc output can be calculated with Equation 6:

$$DC_V = \frac{R_B}{R_B + R96 + R97} \cdot (VREFP - VREFM)$$
$$= \frac{0.5k}{0.5k + 40k + 40k} \cdot 2.4 = 14.9mV$$
(6)

Current flowing through the body is calculated by Equation 7:

$$I_{B} = \frac{VREFP - VREFM}{R96 + R97 + R_{B}} = \frac{2.4}{80.5k} = 29.81 \mu A$$

The peak-to-peak output can then be calculated as shown in Equation 8:  $\Delta V = \Delta R \bullet I_B = 1 \bullet 29.15 = 29.1 \mu V$ 

(8)

(7)



Figure 71 and Figure 72 show the results with  $R_B = 500\Omega$  and  $\Delta R = 1\Omega$  and with  $R_B = 500\Omega$  and  $\Delta R = 0.1\Omega$ , respectively.



Figure 71. Channel 1 Result for  $R_B = 500\Omega$  and  $\Delta R = 1\Omega$ 



Figure 72. Channel 1 Result for  $R_B = 500\Omega$  and  $\Delta R = 0.1\Omega$ 

## 8.4 Summary

These two approaches to performing respiration measurements show that the internal respiration circuitry of the ADS1298R can resolve down to  $100m\Omega$ .



## 9 BOM, Layout, and Schematics

This section contains the complete bill of materials, printed circuit board (PCB) layouts, and schematic diagrams for the ADS1298R.

**NOTE:** Board layouts are not to scale. These are intended to show how the board is laid out; they are not intended to be used for manufacturing ADS1298R PCBs.

## 9.1 ADS1298R Front-End Board Schematics

The ADS1298R schematic is appended to this document.

## 9.2 Printed Circuit Board Layout

Figure 73 through Figure 76 show the ADS1298R PCB layouts.



Figure 73. Top Component Placement





Figure 74. Bottom Component Placement and Routing



Figure 75. Internal Ground Plane (Layer 2)





Figure 76. Internal Power Plane (Layer 3)



## 9.3 ECG Cable Details

Figure 77 shows the details of the recommended ECG cable.

### Cable details:

- 10-lead ECG cable for Philips/HP-snap, button (Part No: 010302013); http://www.biometriccables.com/index.php?productID=692
- 10-lead ECG cable for Philips/HP-Clip-on type (Part No: 010303013A); http://www.biometriccables.com/index.php?productID=693

Another compatible cable for the ADS1298R: HP/Philips/Agilent-compatible 10-lead ECG cable.



Figure 77. ECG Cable Schematic

BOM, Layout, and Schematics



BOM, Layout, and Schematics

## 9.4 Bill of Materials

Table 28 lists the bill of materials for the ADS1298R.

Table 28.	Bill of	Materials:	ADS1298R
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ltem	Quantity	Reference Designator	ence nator Description		Part Number		
1	1	NA	Printed Wiring Board	TI	6522881		
2	16	C1, C2, C3, C4, C5, C6, C11, C17, C47, C48, C49, C52, C58, C76, C77, C96	Capacitor, ceramic 1µF 25V 10% X5R 0603	Murata	GRM188R61E105KA12D		
3	0	C7, C8, C15, C19, C21, C22, C25, C27, C34, C36, C38, C40, C41, C42, C43, C44, C56, C62, C67, C78, C79, C81, C83, C85, C87, C89, C92, C101 - C107, C110, C111	Not installed				
4	1	C9	Capacitor, ceramic 22µF 6.3V 10% X5R 0805	Taiyo Yuden	JMK212BJ226KG-T		
5	11	C10, C45, C46, C50, C51, C54, C55, C60, C61, C65, C66	Capacitor, ceramic 10µF 10V 10% X5R 0805	Murata	GRM219R61A106KE44D		
6	13	C12, C13. C14, C16, C18, C57, C69, C70, C94, C95, C112, C113, C114	Capacitor, ceramic 0.1µF 50V 10% X7R 0603	Murata	GRM188R71H104KA93D		
7	1	C20	Capacitor, ceramic 1500pF 50V 5% C0G 0603	Murata	GRM1885C1H152JA01D		
8	19	C23, C24, C26, C28, C29, C30, C31, C32, C72, C73, C74, C75, C80, C82, C84, C86, C88, C91, C93	Capacitor, ceramic 47pF 50V 5% C0G 0603	Murata	GRM1885C1H470JA01D		
9	0	C33, C35, C37	Not installed				
10	0	C39	Not installed				
11	4	C53, C59, C63, C64	Capacitor, ceramic 2.2µF 6.3V 10% X5R 0603	Murata	GRM185R60J225KE26D		
12	2	C68, C71	Capacitor, ceramic 100µF 10V 20% X5R 1210	Taiyo Yuden	LMK325BJ107MM-T		
13	1	C90	Capacitor, ceramic 1000pF 50V 5% C0G 0603	Murata	GRM1885C1H102JA01D		
14	2	C97, C98	Capacitor, ceramic 560pF 50V 5% C0G 0603	Murata	GRM1885C1H561JA01D		
15	4	C99, C100, C108, C109	Capacitor, ceramic 2200pF 50V 5% C0G 0603	Murata	GRM1885C1H222JA01D		
16	0	D1 - D10	Not installed				
17	1	D11	LED 565nm Green DIFF 0603 SMD	Lumex	SML-LX0603GW-TR		
18	1	J1	CONN D-SUB RCPT 15-Position R/A PCB SLD	FCI	D15S13A4GV00LF		
			CONN D-SUB RCPT R/A 15-Position Gold	Тусо	5747845-3		
19	2	J2, J3 (Bottom)	10-Pin, Dual Row, SM Header (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K		
20	1	J3 (Top)	10-Pin, Dual Row, SM Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P		
21	1	J4 (Bottom)	5-Pin, Dual Row, SM Header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K		
22	0	J5	Not Installed				
23	1	J6	Connector, SMA Jack Straight PCB	Amphenol Emerson	132134 142-0701-201		
24	1	J7(TOP)	Connector, Socket RT ANG 50-Pos .050 (Cut to 4 pins)	Mill-Max	851-43-050-20-001000		
25	4	JP1, JP4, JP5, JP16	2-Position Jumper _ 0.1" spacing	Samtec	TSW-102-07-T-S		
26	0	JP3	Not installed				
27	0	JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP17, JP25	Not installed				
28	12	JP2, JP15, JP18, JP19, JP20, JP21, JP22, JP23, JP24, JP34, JP35, JP36	3-Position Jumper _ 0.1" spacing	Samtec	TSW-103-07-T-S		
29	7	JP26 - JP32	2x2x.1. 2-Pin Dual Row Header	Samtec	TSW-102-07-T-D		

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Table 28	. Bill of	Materials:	ADS1298R	(continued)
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Item	Quantity	Reference Designator	Description	Manufacturer	Part Number
30	1	JP34	4x2x.1, 4-Pin Dual Row Header	Samtec	TSW-104-07-T-D
31	5	L1 - L5	Ferrite bead 470 Ω 0805	Taiyo Yuden	BK2125HM471-T
32	0	R1, R4, R5, R11, R12, R15, R16, R19, R20, R23, R24, R27, R28, R31, R32, R35, R36, R41, R42, R45, R46, R47 - R51, R54, R55, R58 - R66, R68, R69, R70, R89, R90, R91, R92	Not installed		
33	0	R2	Not installed		
34	9	R3, R71, R72, R73, R74, R88, R93, R94, R95	Resistor, 0.0Ω 1/10W 5% 0603 SMD	Yageo	RC0603JR-070RL
35	17	R6, R7, R10, R14, R18, R22, R26, R30, R34, R38, R40, R44, R67, R75, R100, R101, R102	Resistor, 10.0kΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-0710KL
36	10	R9, R13, R17, R21, R25, R29, R33, R37, R39, R43	Resistor, 22.1kΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-0722K1L
37	1	R52	Resistor, 47.5kΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-0747K5L
38	1	R53	Resistor, 43.2kΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-0743K2L
39	1	R56	Resistor, 49.9kΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-0749K9L
40	1	R57	Resistor, 46.4kΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-0746K4L
41	1	R76	Resistor, 1.00MΩ 1/8W 1% 0805 SMD	Yageo	RC0805FR-071ML
42	1	R77	Resistor, 330Ω 1/8W 1% 0805 SMD	Yageo	RC0805FR-07330RL
43	2	R78, R79	Resistor, 1.00kΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-071KL
44	5	R8, R80, R81, R82, R83	Resistor, 1.00MΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-071ML
45	4	R84, R85, R86, R87	Resistor, 10.0MΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-0710ML
46	2	R96, R97	Resistor, 40.2kΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-0740K2L
47	1	R98	Resistor, 330Ω 1/10W 1% 0603 SMD	Yageo	RC0603FR-07330RL
48	1	R99	Resistor, 47.0kΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-0747KL
49	5	TP1, TP2, TP8, TP11, TP12	Test Point PC Mini .040"D Black	Keystone	5001
50	8	TP3, TP4, TP5, TP6, TP7, TP9, TP10, TP13	Test Point PC Mini .040"D Red	Keystone	5000
51	1	U1	8-Channel, 24-Bit Analog-To-Digital Converter with Integrated ECG Front End	ТІ	ADS1298RIZXG
52	0	U2	Not installed		
53	0	U3, U4, U5, U13	Not installed		
54	1	U6	IC, Unreg Chrg Pump V Inv SOT23-5	ТІ	TPS60403DBVR
55	1	U7	IC LDO Reg 250mA 3.0V SOT23-5	ТІ	TPS73230DBVR
56	1	U8	IC LDO Reg Neg 200mA ADJ SOT23-5	ТІ	TPS72301DBVT
57	1	U9	IC LDO Reg 250mA ADJ-V SOT23-5	ТІ	TPS73201DBV
58	1	U10	IC EEPROM 256kBit 400kHZ 8TSSOP	Microchip	24AA256-I/ST
59	1	U11	IC Switch SPST SOT23-5	ТІ	TS5A3166DBVR
60	1	U12	IC Comparator P-P Nanopwr 8-SOIC	ТІ	TLV3491AID
61	1	U14	IC MCU 16-Bit 14TSSOP	ТІ	MSP430G2121IPW14R
62	1	OSC1	OSC 2.0480 MHz 3.3V HCMOS SMT	Fox	FXO-HC735-2.048MHz



Appendix

## 10 Appendix

# 10.1 Optional External Hardware (Not Included)

The input of the ADS1298R requires a DB15 connector. Figure 78 illustrates the most optimal cable connection to the ADS1298R. Figure 79 and Figure 80 show two alternate ways that cables can be constructed to interface with the ADS1298R. Figure 81 shows an alternate testing tool to the instrument used in the tests for this user guide (refer to Section 4.6.1).



Figure 78. 15-Pin, Shielded Connector from Biometric Cables


www.ti.com



Figure 79. 15-Pin, Twisted Wire Cable to Banana Jacks



Figure 80. 15-Pin, Twisted Wire Cable



Figure 81. Cardiosim ECG Simulator Tool

Appendix



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## 10.2 ADS1298R Power-Supply Recommendations

Figure 82 shows a +6V power-supply cable (not provided in the EVM kit) connected to a battery pack with four 1.5V batteries connected in series. Connecting to a wall-powered source (provided in the EVM kit) makes the ADS1298R more susceptible to 50Hz/60Hz noise pickup; therefore, for best performance, it is recommended to power the ADS1298R with a battery source. This configuration minimizes the amount of noise pickup seen at the digitized output of the ADS1298R.



Figure 82. Recommended Power Supply for ADS1298R













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It is important to operate this EVM within the input voltage range of -2.5V to +5V and the output voltage range of 0V to 5V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +30°C. The EVM is designed to operate properly with certain components above +30°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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