

DAC34H84 EVM

Contents

1	Introduction	2
1.1	Overview	2
1.2	EVM Block Diagram	2
2	Software Control	3
2.1	Installation Instructions	3
2.2	Software Operation	3
3	Basic Test Procedure	8
3.1	Test Block Diagram	8
3.2	Test Set-Up Connection	9
3.3	TSW3100 Quick Start Operation	9
3.4	DAC34H84 Software Quick Start Guide	10
4	Optional Configuration	11
4.1	Configuring and Testing the DAC34H84 Transformer Coupled Output	11

List of Figures

1	DAC34H84 EVM Block Diagram.....	2
2	Input Control Options.....	3
3	PLL Configuration.....	4
4	Digital Block Options	5
5	Output Control Options.....	6
6	CDCE62005 Tab Configured for 4x Interpolation.....	7
7	Test Set-up Block Diagram	8
8	TSW3100 CommsSignalPattern (WCDMA) Programming GUI	10
9	DAC34H84 + Modulator WCDMA Output	11
10	Locations of DAC34H84 to Transformer Output Jumper Locations	12
11	DAC34H84 Transformer Coupled Output at 60MHz IF	13
12	DAC34H84 Transformer Coupled Output at 30MHz IF	13

1 Introduction

1.1 Overview

This document is intended to serve as a basic user's guide for the DAC34H84 EVM Revision A. The EVM provides a basic platform to evaluate the DAC34H84, a 1.25GSPS, up to 16x interpolation, 16-bit high speed digital-to-analog converter. With the 32-bit wide LVDS bus interface, the DAC34H84 is capable of up to 625MSPS of input data rate.

The EVM includes the CDCE62005 clocking source which provides the clocks required for the DAC and the pattern generator. The on-board modulators provide IF-to-RF upconversion for basic transmitter evaluation. This EVM is ideally suited for mating with the TSW3100 pattern generation card for evaluating WCDMA, LTE, or other high performance modulation schemes.

1.2 EVM Block Diagram

Figure 1 shows the configuration of the EVM with the TSW3100 used for pattern generation.

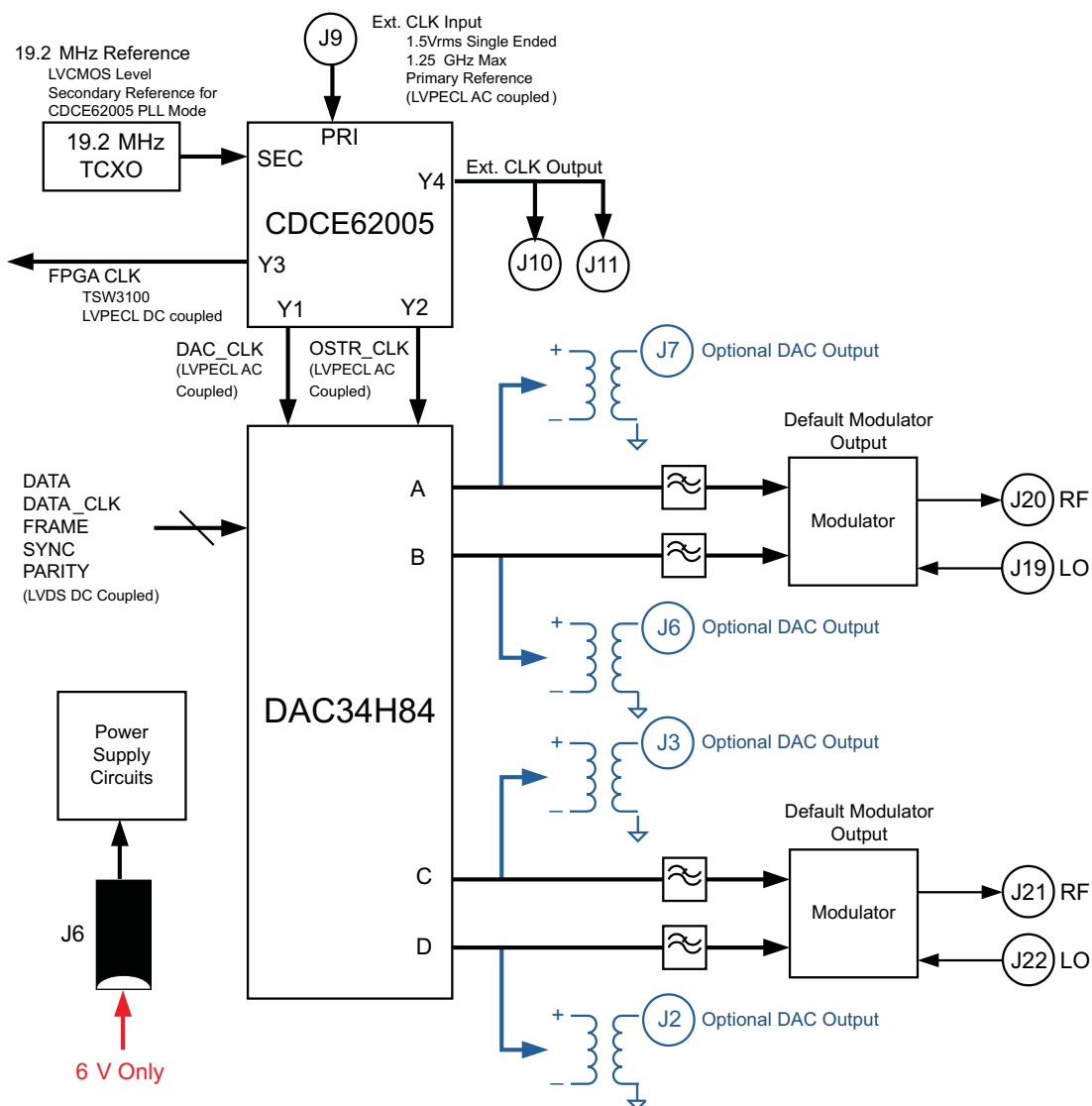


Figure 1. DAC34H84 EVM Block Diagram

2 Software Control

2.1 Installation Instructions

- Open folder named DAC348x_Installer_vxpx (xpx represents the latest version)
- Run Setup.exe
- Follow the on-screen instructions
- Once installed, launch by clicking on the DAC348x_GUI_vxpx program in Start>Texas Instruments DACs
- When plugging in the USB cable for the first time, you will be prompted to install the USB drivers.
 - When a pop-up screen opens, select “Continue Downloading”.
 - Follow the on screen instructions to install the USB drivers
 - If needed, you can access the drivers directly in the install directory

2.2 Software Operation

The software allows programming control of the DAC device and the CDC device. The front panel provides a tab for full programming of each device. The GUI tabs provide more convenient and simplified interface to the most used registers of each device.

Each device, including the DAC3484, DAC3482, and DAC34H84, has its own custom control interface. Select the device option from the top left-hand corner. The *DAC34H84 EVM Software Control* is described in this section.

2.2.1 Input Control Options

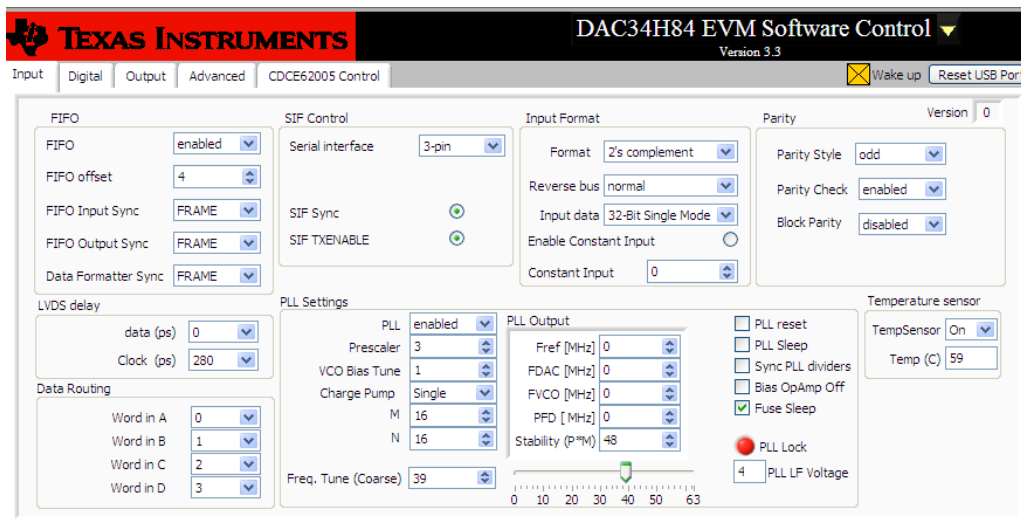


Figure 2. Input Control Options

- FIFO: allows the configuration of the FIFO and FIFO sync sources.
- LVDS delay: provides internal delay of either the LVDS DATA or LVDS DATACLK to help meet the input setup/hold time.
- Data Routing: provides flexible routing of the A, B, C, and D sample input data to the appropriate digital path.
- SIF Control: provides control of the Serial Interface (3-wires or 4-wires) and Serial Interface Sync (*SIF Sync*).
- Input Format: provides control of the input data format (i.e., 2's complement or offset binary).
- Parity: provides configuration of the parity input.
- PLL Settings: provides configuration of the on-chip PLL circuitry.
- Temperature Sensor: provides temperature monitoring of DAC34H84 die temperature.

2.2.1.1 LVDS Delay Settings

The TSW3100 pattern generator sends out LVDS DATA and DATACLK as edge-aligned signal. The following options can be implemented to meet the minimum setup and hold time of DAC348x data latching:

- Set the on-chip LVDS DATALOCK delay. Typical setting of 160ps will help meet the timing requirement for most of the TSW3100 + DAC34H8x EVM setup. This LVDS DATALOCK delay does not account for additional PCB trace-to-trace delay variation, only the internal DATACLK delay.
- Modify the external LVDS DATACLK PCB trace delay: Additional trace length on the bottom side of the PCB can be added to the LVDS DATACLK PCB trace length. Set SJP9, SJP10, SJP11, and SJP12 to 2-3 position for approximately 220ps of trace delay.

2.2.1.2 PLL Settings

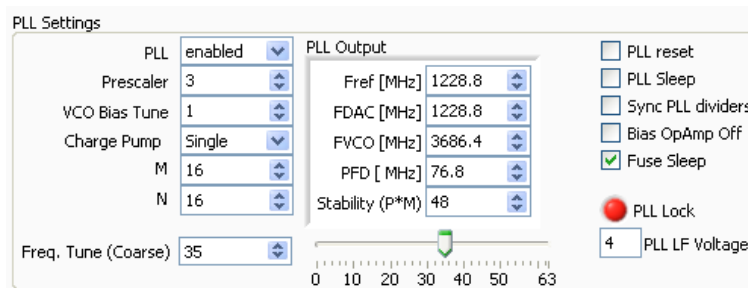


Figure 3. PLL Configuration

Follow the steps below to configure the PLL.

- Enable PLL
- Uncheck *PLL reset* and *PLL sleep*
- Set *M* and *N* ratio such that $F_{DAC} = (M)/(N) \times F_{ref}$
- Set the *prescaler* such that the $F_{DAC} \times \text{prescaler}$ is within 3.3GHz and 4.0GHz
- Set *VCO Bias Tune* to "1"
- *Charge Pump* setting
 - If stability ($P \times M$) is less than 120, then set to "Single"
 - If stability ($P \times M$) is greater than 120, then set to "Double" or install external loop filter
- Adjust the *Freq. Tune (coarse tune)* accordingly.

2.2.2 Digital Block Options

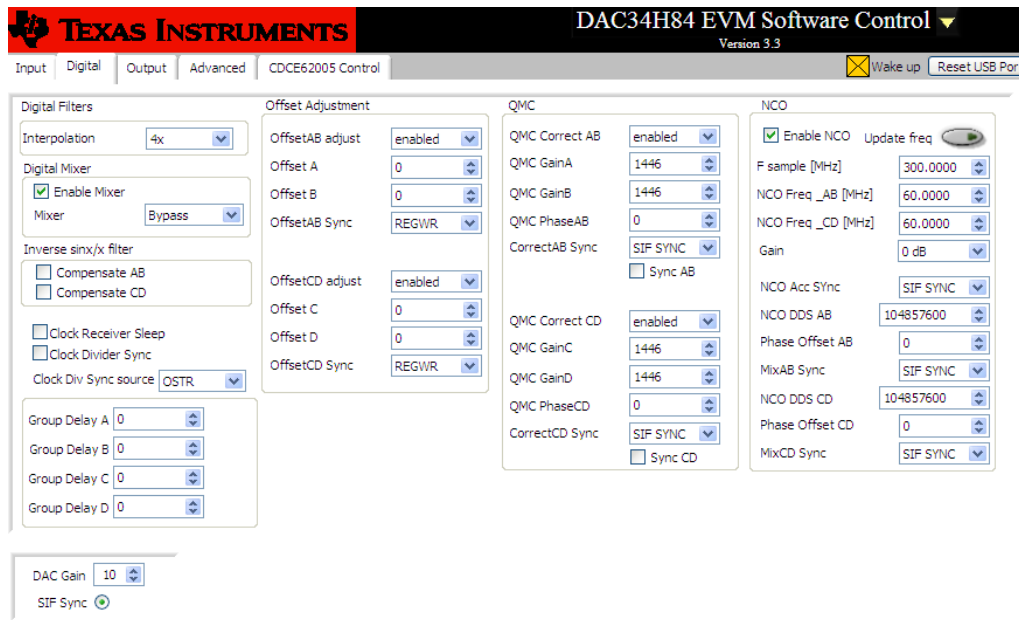


Figure 4. Digital Block Options

- Interpolation: allows control of the data rate versus DAC sampling rate ratio (i.e. data rate * interpolation = DAC sampling rate).
- Digital Mixer: allows control of the coarse mixer function.
Note: If fine mixer (NCO) is used, the “Enable Mixer” button must be checked, and the coarse mixer must be bypassed. See NCO section for detail.
- Inverse sinx/x filter: allows compensation of the sinx/x attenuation of the DAC output.
Note: If inverse sinx/x filter is used, the input data digital full-scale must be backed off accordingly to avoid digital saturation.
- Clock Receiver Sleep: allows the DAC clock receiver to be in sleep mode. The DAC has minimum power consumption in this mode.
- Clock Divider Sync: allows the sync of the internal divided-down clocks using either FRAME, SYNC, or OSTR signal. Enable the divider sync as part of the initialization procedure or resynchronization procedure.
- Group Delay: allows adjustment of group delay for each I/Q channel. This is useful for wideband sideband suppression.
- Offset Adjustment: allows adjustment of DC offset to minimize the LO feed-through of the modulator output. This section requires sync for proper operation. The sync options are listed below:
 - REGWR: auto-sync from SIF register write.
 - OSTR: sync from the external LVPECL OSTR signal. Clock divider sync must be enabled with OSTR set as sync source
 - SYNC: sync from the external LVDS SYNC signal.
 - SIF SYNC: sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.
- QMC Adjustment: allows adjustment of the gain and phase of the I/Q channel to minimize sideband power of the modulator output.
 - REGWR: auto-sync from SIF register write.
 - OSTR: sync from the external LVPECL OSTR signal. Clock divider sync must be enabled with OSTR set as sync source
 - SYNC: sync from the external LVDS SYNC signal.
 - SIF SYNC: sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.

- NCO: allows fine mixing of the I/Q signal. The procedure to adjust the NCO mixing frequency are listed below:
 1. Enter the DAC sampling frequency in *Fsample*.
 2. Enter the desired mixing frequency in both *NCO freq_AB* and *NCO freq_CD*.
 3. Press *Update freq*
 4. Sync the NCO block from the following options:
 - *REGWR*: auto-sync from SIF register write. Writing to either *Phase OffsetAB* or *Phase OffsetCD* can create a sync event.
 - *OSTR*: sync from the external LVPECL OSTR signal. Clock divider sync must be enabled with OSTR set as sync source. Refer to the datasheet for OSTR period requirement.
 - *SYNC*: sync from the external SYNC signal
 - *SIF SYNC*: sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.

2.2.3 Output Control Options

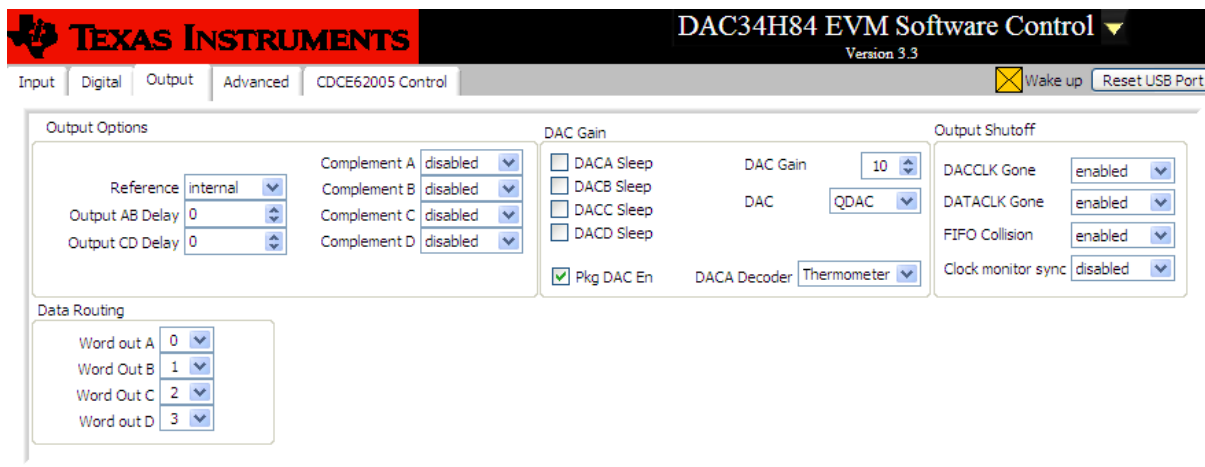


Figure 5. Output Control Options

- Output Options: allows the configuration of reference, output polarity, and output delay
- Data Routing: provides flexible routing of the A, B, C, and D digital path to the desired output channels.
- DAC Gain: configures the full-scale DAC current. With *Rbiaj* resistor set at 1.28kΩ:
 - DAC Gain = 15 for 30mA full-scale current.
 - DAC Gain = 10 for 20mA full-scale current (default).
- Output Shutoff On: allows outputs to shut-off when DACCLK GONE, DATACLK GONE, or FIFO COLLISION alarm event occurs.

2.2.4 CDCE62005

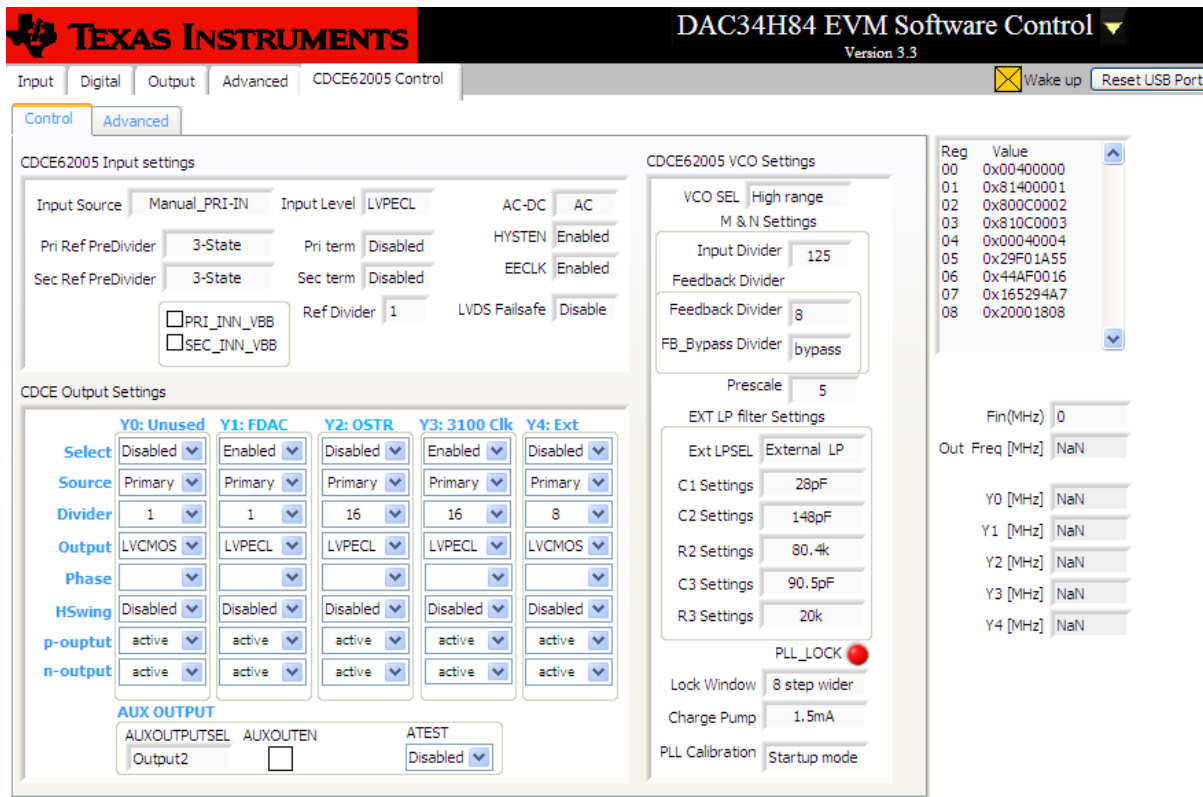


Figure 6. CDCE62005 Tab Configured for 4x Interpolation

Clock frequency control is determined by register values in the CDCE62005 Control tab. Refer to the CDCE62005 datasheet for detailed explanations of the register configuration to change the clock frequency.

The following CDCE62005 outputs are critical to proper operation of the DAC34H84:

- **Y1: DAC34H84 DAC sampling clock.** If the DAC34H84 is configured for internal PLL mode, this will be the reference clock input for the PLL block.
- **Y2: DAC34H84 FIFO OSTR clock.** The clock rate for this should be at most $F_{DAC}/\text{Interpolation}/8$.
 - The whole OSTR clock equation needs to take account of both the Y2 CDCE62005 clock divider ratio and the additional CDCP1803 divide-by-2 clock divider.
 - This OSTR signal can be a slower periodic signal or a pulse depending on the application.
 - **Note:** the FIFO OSTR clock should be disabled when the DAC34H84 is in PLL mode.
- **Y3: TSW3100 FPGA clock.** The clock rate for this should be $F_{DAC}/\text{interpolation}/4$.

2.2.5 Register Control

- Send All: Sends the register configuration to all devices
- Read All: Reads register configuration from DAC34H84 device
- Load Regs: Load a register file for all devices. Sample configuration files for common frequency plans are located in the install directory.
 - Select *Load Regs* button.
 - Double click on the *data* folder.
 - Double click on the desired register file.
 - Click on *Send All* to ensure all of the values are loaded properly.
- Save Regs: Saves the register configuration for all devices

2.2.6 Miscellaneous Settings

- Reset USB: Toggle this button if the USB port is not responding. This generates a new USB handle address
 - Note: It is recommended that the board be reset after every power cycle and the “reset usb” button on the GUI be clicked.
- Exit: Stops the program

3 Basic Test Procedure

This section outlines the basic test procedure for testing the EVM.

3.1 Test Block Diagram

The test set-up for general testing of the DAC34H84 with the TSW3100 pattern generation card is shown in [Figure 7](#).

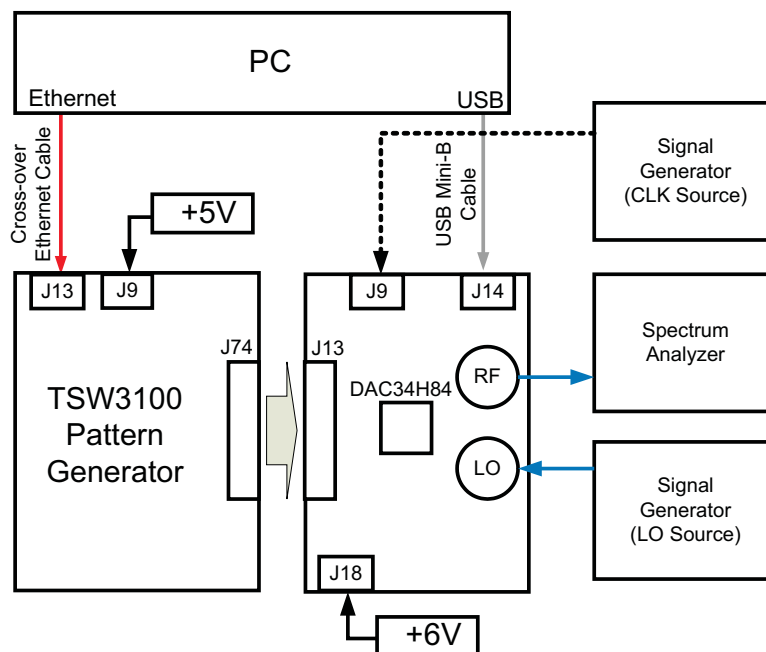


Figure 7. Test Set-up Block Diagram

3.2 Test Set-Up Connection

- TSW3100 Pattern Generator
 1. Connect 5V power supply to J9, *5V_IN* jack of the TSW3100 EVM.
 2. Connect the PC's Ethernet port to J13, *Ethernet* port of the TSW3100. The cable should be a standard cross-over Cat5e Ethernet cable.
- DAC34H84 EVM
 1. Connect J13 connector of DAC34H84 EVM to J74 connector of TSW3100 EVM
 2. Connect 6V to the J18, *Power In* jack of the DAC34H84 EVM.
 3. Connect PC's USB port to J14 USB port of the DAC34H84 EVM. The cable should be a standard A to mini-B connector cable.
 4. Provide a 1.5Vrms, 1.25GHz max Clock at J9, *CLKIN* SMA port of DAC34H84 EVM.
 5. Provide 12dBm max, 1500MHz to 2500GHz LO source at J19 or J22 port of the DAC34H84 EVM. This is to provide the LO source to the modulators.
 6. Connect the RF output port of J20 or J21 to the spectrum analyzer.
- DAC34H84 EVM jumpers: make sure the following jumpers are at their default setting
 - JP11 open.
 - JP10 on pin {1,2}
 - JP9 shorted.
 - JP8 shorted.
 - JP7 shorted. It can be open if the 19.2MHz TCXO is not used for CDCE62005 clock reference
 - JP6 on pin {1,2}
 - JP5 on pin {1,2}
 - JP4 on pin {2,3}
 - JP3 on pin {2,3}
 - JP2 on pin {1,2}

3.3 TSW3100 Quick Start Operation

Reference the TSW3100 User's Guide for more detailed explanations of the TSW3100 set-up and operation. This document assumes the TSW3100 software is installed and functioning properly. *The DAC348x needs TSW3100 operating software version 2.5 or higher with TSW3100 board Rev E (or higher).*

CommsSignalPattern Setup from Default Configuration (WCDMA)

- Change Interpolation value to DAC Clock Rate / Interpolation / 3.84 (**i.e. 1228.8 / 4 / 3.84 = 80**)
- Enter desired Offset Frequency (i.e. 30 MHz) for each desired carrier
- Select the **LVDS** output button
- Check the "LOAD and Run" box
- Press the green "Create" button

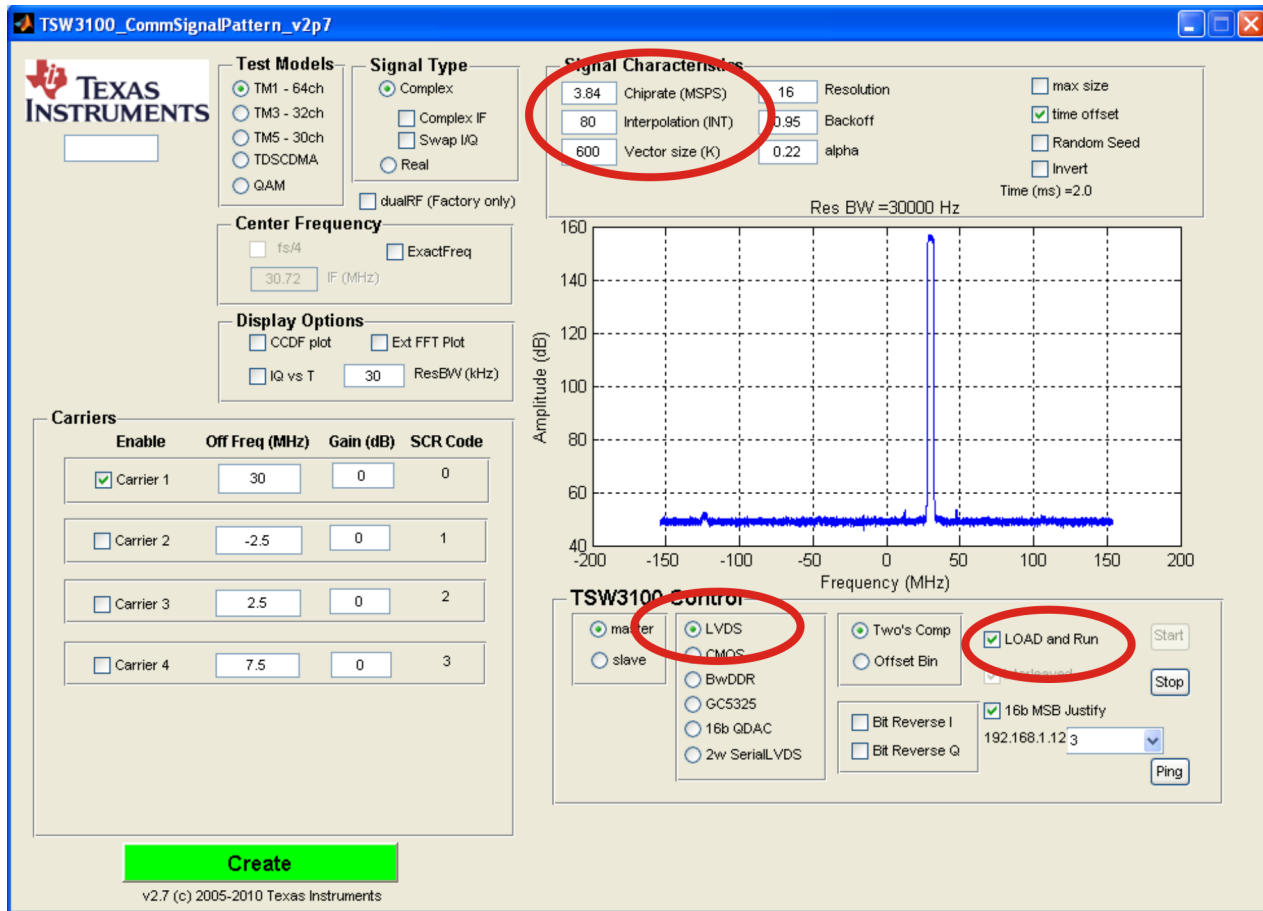
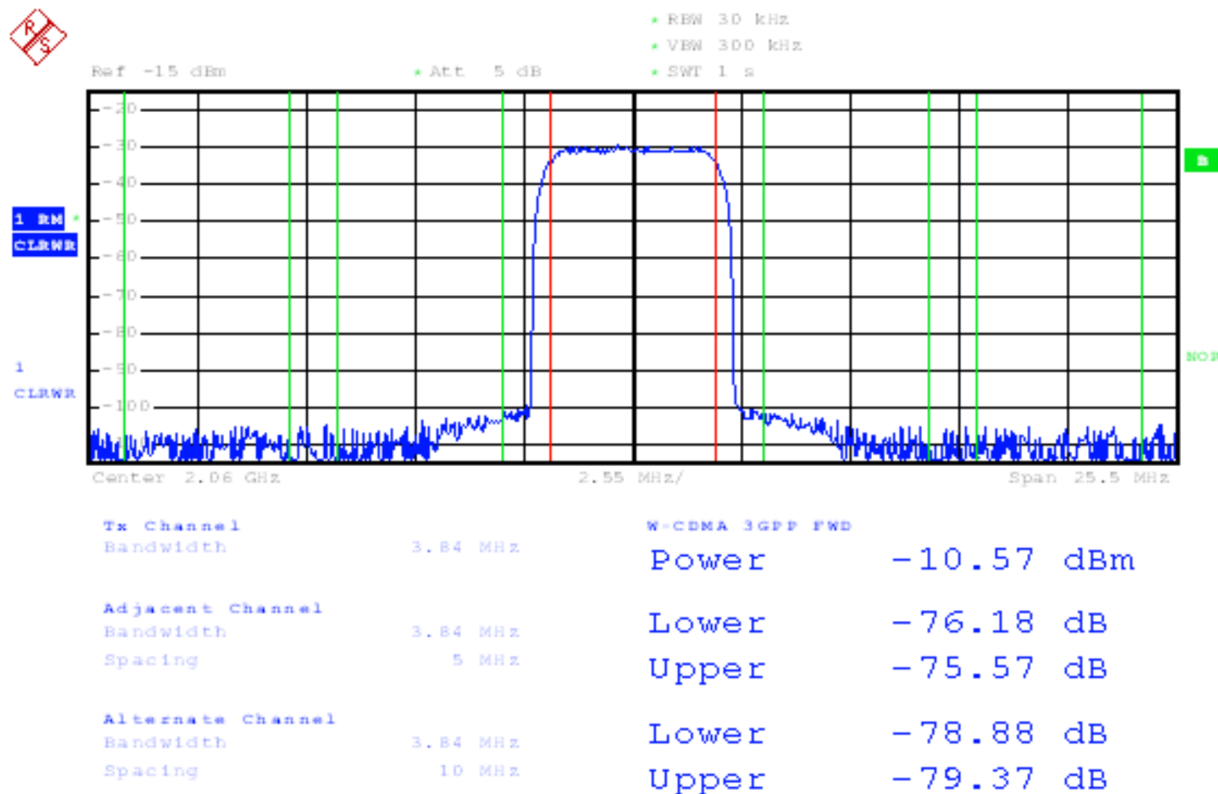


Figure 8. TSW3100 CommsSignalPattern (WCDMA) Programming GUI

3.4 DAC34H84 Software Quick Start Guide

- Provide the clock input **1228.8 MHz** at 1.5Vrms at J9 SMA connector of the DAC34H84 EVM.
- Provide the LO source of **2GHz (6dBm max)** at either J19 or J22 SMA connector of the DAC34H84 EVM.
- Turn on power to the board and press the reset button on the EVM
- Press the "Reset USB Port" button in GUI and verify USB communication.
- Switch to the INPUT tab of GUI
- Click "LOAD REGS", browse to the installation folder and load example file *DAC34H84_FDAC_1228p8MHz_4xint_NCO_30MHz_QMCon.txt*. This file contains settings for 4x interpolation with the DAC34H84 running at 1228.8MSPS. Load this file and wait a couple of seconds for the settings to go into effect.
- Verify the spectrum using the Spectrum Analyzer at the two RF outputs of the DAC EVM (J20 and J21).
- **(Toggle the SIF SYNC button to sync the appropriate digital blocks, if example file with NCO setting is used)**



(Baseband = 30MHz, NCO = 30MHz with NCO Gain disabled, QMC Gain = 1446, LO = 2000MHz)

Figure 9. DAC34H84 + Modulator WCDMA Output

4 Optional Configuration

4.1 Configuring and Testing the DAC34H84 Transformer Coupled Output

- Eight 0 Ohm resistors must be moved to configure the output of the DAC34H84 to be 4:1 transformer coupled
- Remove these resistors (Horizontal position): R19, R26, R27, R33, R35, R41, R93, R94.
- Install the following resistors (Vertical position): R1, R3, R8, R11, R17, R161, R162, R163. See [Figure 10](#) for detail.

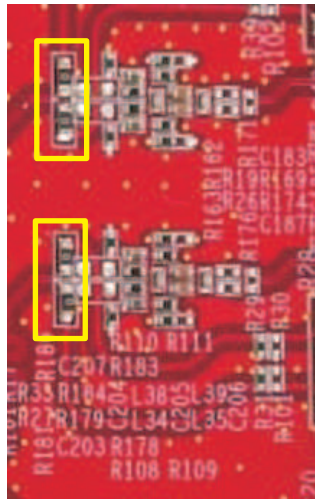
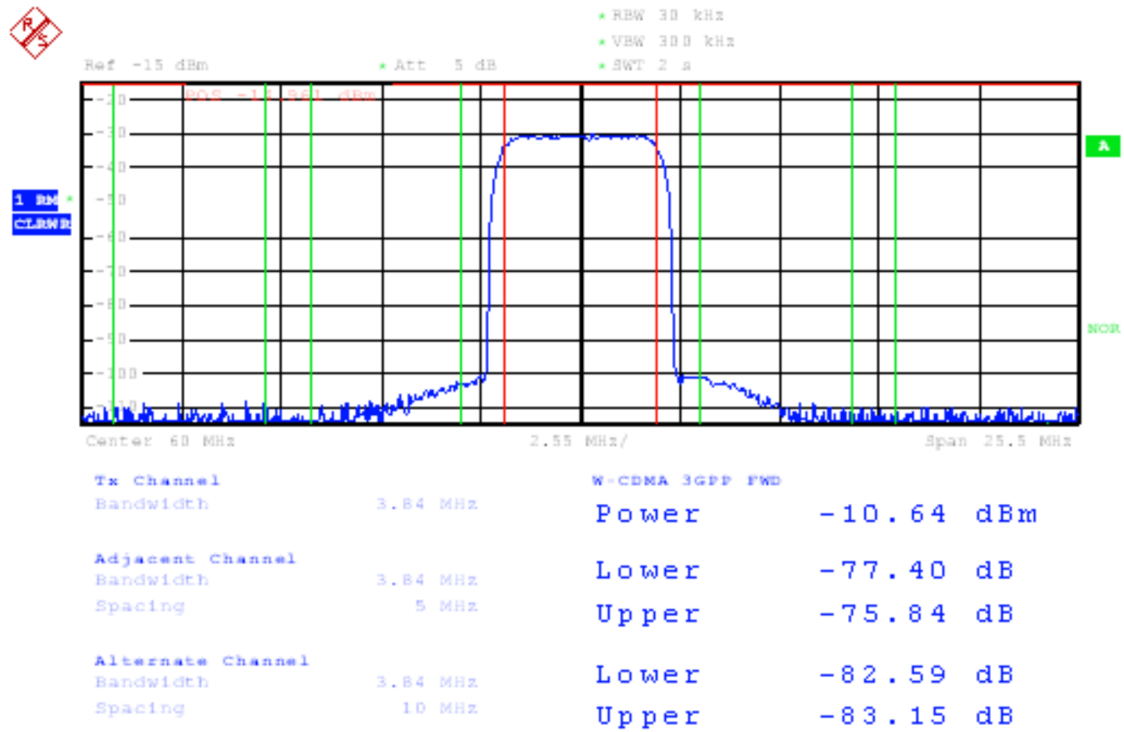


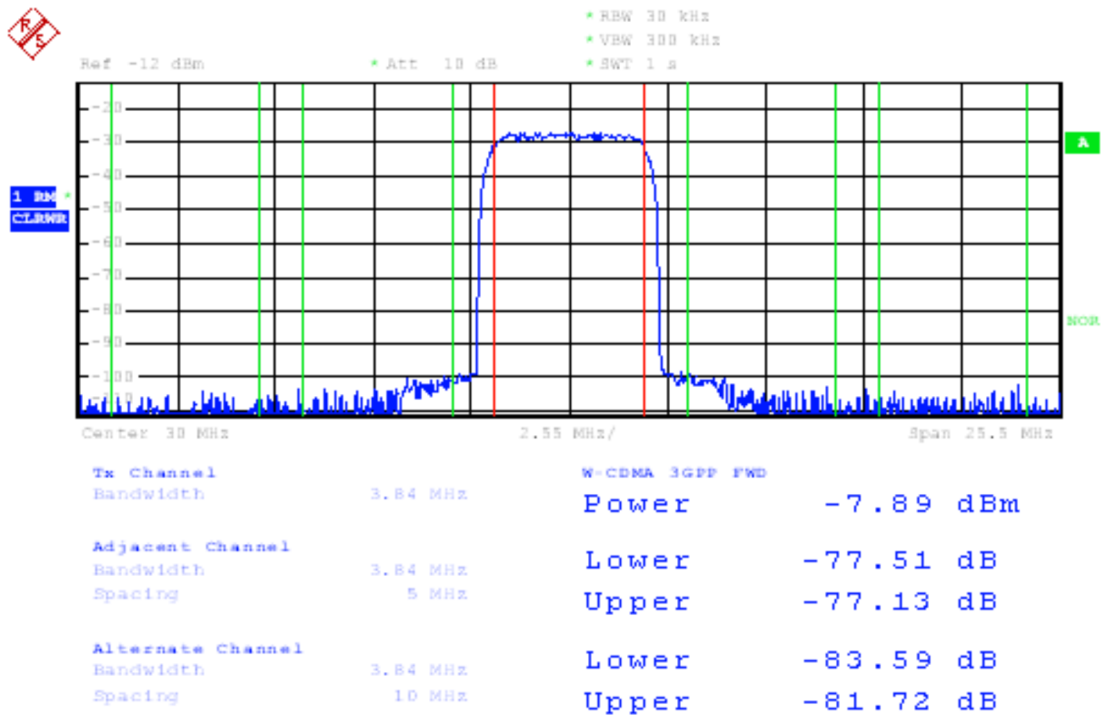
Figure 10. Locations of DAC34H84 to Transformer Output Jumper Locations

- Provide the clock input **1228.8** MHz at 1.5Vrms at J9 SMA connector of the DAC34H84 EVM
- Turn on power to the board and press the reset button on the EVM
- Press the “Reset USB Port” button in GUI and verify USB communication.
- Switch to the INPUT tab of GUI
- Click “LOAD REGS”, browse to the installation folder and load example file *DAC34H84_FDAC_1228p8MHz_4xint_NCO_30MHz_QMCon.txt*. This file contains settings for 4x interpolation with the DAC34H84 running at 1228.8MSPS. Load this file and wait a couple of seconds for the settings to go into effect.
- Verify the spectrum using the Spectrum Analyzer at the four DAC outputs of the DAC EVM (J7, J6, J3, and J2).
- **(Toggle the SIF SYNC button to sync the appropriate digital blocks, if example file with NCO setting is used)**



(baseband = 30MHz, NCO = 30MHz with NCO Gain disabled, QMC Gain = 1446)

Figure 11. DAC34H84 Transformer Coupled Output at 60MHz IF



(baseband = 30MHz, NCO disabled, QMC Gain = 1024)

Figure 12. DAC34H84 Transformer Coupled Output at 30MHz IF

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. **THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.**

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 5.5 V to 7.0 V and the output voltage range of 0 V to 3.3 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55° C. The EVM is designed to operate properly with certain components above 55° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video
Wireless	www.ti.com/wireless-apps

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated