

ADS58C28

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# Dual Channel IF Receiver with SNRBoost<sup>3G</sup>

Check for Samples: ADS58C28

# **FEATURES**

- Maximum Sample Rate: 200MSPS
- **High Dynamic Performance:** 
  - 83dBc SFDR at 140MHz
  - 72.5dBFS SNR with 60MHz BW Using SNRBoost<sup>3G</sup> Technology
- SNRBoost<sup>3G</sup> Highlights:
  - Supports Wide Bandwidth (up to 60MHz)
  - Programmable Bandwidths: 20MHz, 30MHz, and 40MHz
  - Flat Noise Floor within the Band
  - Independent SNRBoost<sup>3G</sup> Coefficients for **Both Channels**
- **Output Interface:** 
  - Double Data Rate (DDR) LVDS with **Programmable Swing and Strength:** 
    - Standard Swing: 350mV
    - Low Swing: 200mV
    - Default Strength: 100Ω termination
    - 2x Strength: 50Ω termination
  - Compatible with GC6016
  - 1.8V Parallel CMOS Interface Also Supported
  - Ultralow Power with Single 1.8V Supply:
  - 470mW Total Power
  - 710mW Total Power (200MSPS) with SNRBoost<sup>3G</sup> on Both Channels
- Programmable Gain up to 6dB for SNR/SFDR Trade-off
- **DC Offset Correction**
- **Supports Low Input Clock Amplitude**
- Package: QFN-64 (9mm × 9mm)

# DESCRIPTION

ADS58C28 The is а dual-channel, 11-bit analog-to-digital converter (ADC) with sampling rates up to 200MSPS. The device uses innovative design techniques to achieve high dynamic performance, while consuming extremely low power at 1.8V supply. This architecture makes it well-suited for multi-carrier. wide bandwidth communications applications.

The ADS58C28 uses third-generation SNRBoost<sup>3G</sup> technology to overcome SNR limitation as a result of quantization noise (for bandwidths less than Nyquist, f<sub>S</sub>/2). Enhancements in the SNRBoost<sup>3G</sup> technology allow support for SNR improvements over wide bandwidths (up to 60MHz). In addition, separate SNRBoost<sup>3G</sup> coefficients can also be programmed for each channel.

The device has a digital gain function that can be used to improve SFDR performance at lower full-scale input ranges. It includes a dc offset correction loop that can be used to cancel the ADC offset. The digital outputs of all channels are output as double data rate (DDR) low-voltage differential signaling (LVDS) together with an LVDS clock output. The low data rate of this interface (400MBPS at 200MSPS sample rate) makes it possible to use low-cost field-programmable gate array (FPGA)-based receivers. The strength of the LVDS output buffers can be increased to support 50Ω differential termination. This increase allows the output clock signal to be connected to two separate receiver chips with an effective  $50\Omega$  termination (such as the two clock ports of the GC5330). The same digital output pins can also be configured as a parallel 1.8V CMOS interface.

The device includes internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. The ADS58C28 is specified over the industrial temperature range (-40°C to +85°C).



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# ADS58C28



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT	PACKAGE- LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN <sup>(2)</sup>	LEAD/BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA			
40050000		BCC	40%C to 195%C	GREEN (RoHS, no		4750000	ADS58C28IRGC	Tape and reel			
AD556C26	QFIN-04	$RGC = -40^{\circ}C$ to $+85^{\circ}C$		Sb/Br)	Cu/NIPdAu	AZ56028	ADS58C28IRGC	Tape and reel			

# ORDERING INFORMATION<sup>(1)</sup>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

(2) Eco Plan is the planned eco-friendly classification. Green (RoHS, no Sb/Br): TI defines Green to mean Pb-Free (RoHS compatible) and free of Bromine- (Br) and Antimony- (Sb) based flame retardants. Refer to the Quality and Lead-Free (Pb-Free) Data web site for more information.

The ADS58C28 is pin-compatible with the previous generation ADS62C17 converter; this architecture enables easy migration. However, there are some important differences between the generations, summarized in Table 1.

## Table 1. Migrating from the ADS62C17

ADS62C17	ADS58C28						
PINS							
Pin 22 is NC (not connected)	Pin 22 is AVDD						
Pins 38 and 58 are DRVDD	Pins 38 and 58 are NC (do not connect pins)						
Pins 39 and 59 are DRGND	Pins 39 and 59 are NC (do not connect pins)						
SUPPLY							
AVDD is 3.3V	AVDD is 1.8V						
DRVDD is 1.8V	No change						
INPUT COMMON-MODE VOLTAGE							
CM is 1.5V	CM is 0.95V						
SERIAL INTERFACE							
Protocol: 8-bit register address and 8-bit register data	No change in protocol New serial register map						
PARALLEL CONFIGURATION							
SCLK pin controls internal and external reference mode	SCLK pin enables low-speed mode						
EXTERNAL REFERENCE							
Supported	Not supported						

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# ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

		ADS5	8C28	
		MIN	МАХ	UNIT
Supply voltage range, AVDD		-0.3	2.1	V
Supply voltage range, DRVDD		-0.3	2.1	V
Voltage between AGND and DRGND		-0.3	0.3	V
Voltage between AVDD to DRVDD (when	AVDD leads DRVDD)	-2.4	2.4	V
Voltage between DRVDD to AVDD (when	DRVDD leads AVDD)	-2.4	2.4	V
	INP, INM	-0.3	Minimum (1.9, AVDD + 0.3)	V
Voltage applied to input pins	CLKP, CLKM <sup>(2)</sup>	-0.3	AVDD + 0.3	V
	RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3	-0.3	+3.9	V
Operating free-air temperature range, $T_A$		-40	+85	°C
Operating junction temperature range, $T_J$		+125	°C	
Storage temperature range, T <sub>stg</sub>		-65	+150	°C
ESD, Human body model (HBM)			2	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is less than |0.3V|. This prevents the ESD protection diodes at the clock input pins from turning on.

# THERMAL INFORMATION

		ADS58C28	
	THERMAL METRIC <sup>(1)</sup>	RGC	UNITS
		64 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	23.9	
$\theta_{\text{JCtop}}$	Junction-to-case (top) thermal resistance	10.9	_
$\theta_{JB}$	Junction-to-board thermal resistance	4.3	°C/M
ΨJT	Junction-to-top characterization parameter	0.1	°C/vv
$\Psi_{JB}$	Junction-to-board characterization parameter	4.4	
$\theta_{\text{JCbot}}$	Junction-to-case (bottom) thermal resistance	0.6	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.



# **RECOMMENDED OPERATING CONDITIONS**

Over operating free-air temperature range, unless otherwise noted.

		MIN	NOM	MAX	UNIT
SUPPLIES					
Analog supply voltage, AVDD	1.75	1.8	1.9	V	
Digital supply voltage, DRVDD		1.7	1.8	1.9	V
ANALOG INPUTS					
Differential input valtage range	Default, SNRBoost <sup>3G</sup> disabled		2		V <sub>PP</sub>
Differential input voltage fange	SNRBoost <sup>3G</sup> enabled		1.6		V <sub>PP</sub>
Input common-mode voltage		VCM	$^{(1)} \pm 0.05$		V
Maximum analog input frequency with 2	V <sub>PP</sub> input amplitude <sup>(2)</sup>		400		MHz
Maximum analog input frequency with 1	V <sub>PP</sub> input amplitude <sup>(2)</sup>		600		MHz
CLOCK INPUT					
Insuit clock comple rote (3)	Default after reset LOW SPEED mode disabled	> 80		200	MODO
Input clock sample rate ~	LOW SPEED mode enabled	1		80	101222
	Sine wave, ac-coupled	0.2	1.5		V <sub>PP</sub>
Input clock amplitude differential	LVPECL, ac-coupled		1.6		V <sub>PP</sub>
(V <sub>CLKP</sub> – V <sub>CLKM</sub> )	LVDS, ac-coupled		0.7		V <sub>PP</sub>
	LVCMOS, single-ended, ac-coupled		1.8		V
Input clock duty cycle	Default after reset LOW SPEED mode disabled	35	50	65	%
	LOW SPEED mode enabled	40	50	60	%
DIGITAL OUTPUTS					
Maximum external load capacitance from	n each output pin to DRGND, C <sub>LOAD</sub>		10		pF
Differential load resistance between the	LVDS output pairs (LVDS mode), R <sub>LOAD</sub>		100		Ω
HIGH-PERFORMANCE MODES <sup>(4)(5)</sup>					
High-performance mode	igh-performance mode Set this register bit to get best performance across Register address = 03h, data = 03h				
High frequency mode	Set these register bits for high input signal	Register a data = 01h	ddress = 4/ 1	Ah,	
nigh-hequency mode	frequencies (> 200MHz)	Register a data = 01h	ddress = 58 1	Bh,	
Operating free-air temperature, T <sub>4</sub>	-40		+85	°C	

VCM, typically 0.95V, is the voltage measured on the VCM pin when the input clock is switched off.
 See the *Theory of Operation* section in the Application Information

See description for LOW SPEED mode in the Serial Interface Configuration section. (3)

(4)

It is recommended to use these modes to obtain best performance. See the Serial Interface Configuration section for details on register programming. (5)



# **ELECTRICAL CHARACTERISTICS**

Typical values are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, sampling frequency = 200MSPS, 50% clock duty cycle, -1dBFS differential analog input, and LVDS and CMOS interfaces, unless otherwise noted.

Minimum and maximum values are across the full temperature range:  $T_{MIN} = -40$  °C to  $T_{MAX} = +85$  °C, AVDD = 1.8V, and DRVDD = 1.8V.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTI	ION	· ·				
Resolution					11	Bits
ANALOG I	NPUTS					
	Differential input voltage range			2		V <sub>PP</sub>
	Differential input resistance (at 200MHz, see Figure 55)			0.75		kΩ
	Differential input capacitance (at 200MHz, see Figure 56)			3.7		pF
	Analog input bandwidth			550		MHz
	Analog input common-mode current (per input pin of each channel)			1.5		µA/MSPS
	VCM common-mode voltage output			0.95		V
	VCM output current capability			4		mA
POWER SI	UPPLY					
IAVDD	Analog supply current			141	163	mA
IDRVDD	Output buffer supply current LVDS interface	$350mV LVDS$ swing with $100\Omega$ external termination after reset		120	130	mA
	Analog power			254		mW
	Digital power LVDS interface			216		mW
	Global power-down				15	mW
DC ACCUP	RACY					
DNL	Differential nonlinearity	$f_{IN} = 170MHz$	-0.6		0.6	LSB
INL	Integral nonlinearity	$f_{IN} = 170MHz$	-1.5	0.3	1.5	LSB
	Offset error	Specified across devices and channels within a device	-15		15	mV
	There are two sources of gain error: ir	nternal reference inaccuracy and char	nnel gain e	error		
	Gain error as a result of internal reference inaccuracy alone	Specified across devices and channels within a device	-2		2	%FS
	Gain error of channel alone <sup>(1)</sup>	Specified across devices and channels within a device		±0.1	±1	%FS
	Channel gain error temperature coefficient			0.002		∆%/°C

(1) Specified by design and characterization; not tested in production.



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# **ELECTRICAL CHARACTERISTICS**

Typical values are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, sampling frequency = 200MSPS, 50% clock duty cycle, -1dBFS differential analog input, SNRBoost<sup>3G</sup> disabled, and LVDS and CMOS interfaces, unless otherwise noted. Minimum and maximum values are across the full temperature range:  $T_{MIN} = -40$ °C to  $T_{MAX} = +85$ °C, AVDD = 1.8V, and

DRVDD = 1.8V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SNR	f <sub>IN</sub> = 20MHz		66.8		
Signal-to-noise ratio,	f <sub>IN</sub> = 100MHz		66.4		dBFS
LVDS	f <sub>IN</sub> = 170MHz	65	66		
	f <sub>IN</sub> = 20MHz		66.7		
SINAD Signal-to-noise and distortion ratio	f <sub>IN</sub> = 100MHz		66.3		dBFS
	f <sub>IN</sub> = 170MHz	64.5	65.8		
	f <sub>IN</sub> = 20MHz		82		
SFDR Spurious-free dynamic range	f <sub>IN</sub> = 100MHz		84		dBc
opunous nee dynamic range	f <sub>IN</sub> = 170MHz	70.5	80		
	f <sub>IN</sub> = 20MHz		80		
THD Total harmonic distortion	f <sub>IN</sub> = 100MHz		81		dBc
	f <sub>IN</sub> = 170MHz	69.5	78		
	f <sub>IN</sub> = 20MHz		82		
HD2 Second-barmonic distortion	f <sub>IN</sub> = 100MHz		85		dBc
	f <sub>IN</sub> = 170MHz	70.5	79		
	f <sub>IN</sub> = 20MHz		86		dBc
HD3 Third-harmonic distortion	f <sub>IN</sub> = 100MHz		86		
	f <sub>IN</sub> = 170MHz	70.5	85		
Worst Spur	f <sub>IN</sub> = 20MHz		90		
Other than second and third	f <sub>IN</sub> = 100MHz		89		dBc
harmonics	f <sub>IN</sub> = 170MHz	74.5	88		
IMD Two-tone intermodulation distortion	F1 = 185MHz, F2 = 190MHz, each tone at -7dBFS		83		dBFS
Input overload recovery	Recovery to within 1% (of final value) for 6dB overload with sine wave input		1		Clock cycles
Crosstalk	With a full-scale 170MHz signal on aggressor and a full-scale 20MHz signal on victim		96		dB
PSRR AC power-supply rejection ratio	For 50mV <sub>PP</sub> signal on AVDD supply		20		dB



# **DIGITAL CHARACTERISTICS**

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at valid logic level 0 or 1. AVDD = 1.8V and DRVDD = 1.8V.

PAR	AMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS-F	RESET, SCLK, SDATA,	SEN, CTRL1, CTRL2, and CTRL3				
High-level input volta	ge	RESET, SCLK, SDATA and SEN support	1.3			V
Low-level input voltage	ge	1.8V and 3.3V CMOS logic levels.			0.4	V
High-level input	SDATA, SCLK <sup>(1)</sup>	V <sub>HIGH</sub> = 1.8V		10		μA
current	SEN <sup>(2)</sup>	V <sub>HIGH</sub> = 1.8V		0		μA
Low-level input	SDATA, SCLK	$V_{LOW} = 0V$		0		μA
current	SEN	$V_{LOW} = 0V$		-10		μA
DIGITAL OUTPUTS	-CMOS INTERFACE (	CHx_Dn, SDOUT)				
High-level output volt	tage		DRVDD - 0.1	DRVDD		V
Low-level output volt	age			0	0.1	V
DIGITAL OUTPUTS	-LVDS INTERFACE (C	HxP/M, CLKOUTP/M)				
V <sub>ODH</sub> , High-level outp	out voltage <sup>(3)</sup>	Standard swing LVDS	270	350	430	mV
V <sub>ODL</sub> , Low-level output voltage <sup>(3)</sup>		Standard swing LVDS -430		-350	-270	mV
V <sub>ODH</sub> , High-level output voltage <sup>(3)</sup>		Low swing LVDS <sup>(4)</sup>		200		mV
V <sub>ODL</sub> , Low-level output voltage <sup>(3)</sup>		Low swing LVDS <sup>(4)</sup> –20		-200		mV
V <sub>OCM</sub> , Output commo	on-mode voltage		0.9	1.05	1.25	V

SDATA and SCLK have an internal 150k $\Omega$  pull-down resistor. (1)

SEN has an internal  $150k\Omega$  pull-up resistor to AVDD.

(2) (3) With external  $100\Omega$  termination.

(4) See the LVDS Output Data and Clock Buffers section.

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		SNR WITHIN SPECIFIED BANDWIDTH (dBFS)						
	BANDWIDTH (MHz)	IN DEFAULT MODE (SNRBoost <sup>3G</sup> Disabled)			WITH SNRBoost <sup>3G</sup> ENABLED <sup>(2)(3)</sup>			
		MIN	ТҮР	MAX	MIN	ТҮР	MAX	
	60		68.3		69.7	72.5		
	40		70		71.8	74		
	30		71.1		72.8	74.7		
	20		72.5		74.4	76		
-	<b>1</b>	X	Logic 0 $V_{ODL} = -350 \text{mV}^{(1)}$	)	X	Logic 1 V <sub>ODH</sub> = +350mV	,(1)	
HAn_M	/		*	/	`\ <u>!</u>	!	/	
	V <sub>OCM</sub>							
GND -	₩							

Table 2. SNR Enhancement with SNRBoost<sup>3G</sup> Enabled<sup>(1)</sup>



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(2) The PowerPAD<sup>™</sup> is connected to DRGND.

AVDD 16

10 18

17

AGND

(3) NC = no connection.

# Figure 2. ADS58C28 LVDS Pinout

50 58

30

NA\_M

27

AGND

25 23 23 23

20

INB\_M AGND AVDD CM AGND CLKP CLKM

INB\_P

5

## Pin Assignments (LVDS Mode)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
AVDD	16, 22, 33, 34	4	Input	Analog power supply
AGND	17, 18, 21, 24, 27, 28, 31, 32	8	Input	Analog ground
CLK_P	25	1	Input	Differential clock positive input
CLK_M	26	1	Input	Differential clock negative input
INA_P	29	1	Input	Differential analog positive input, channel A
INA_M	30	1	Input	Differential analog negative input, channel A
INB_P	19	1	Input	Differential analog positive input, channel B
INB_M	20	1	Input	Differential analog negative input, channel B
СМ	23	1	Output	This pin outputs the common-mode voltage (0.95V) that can be used externally to bias the analog input pins

AVDD

33

32

31

AGND

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# Pin Assignments (LVDS Mode) (continued)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
RESET	12	1	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the <i>Serial Interface Configuration</i> section. In parallel interface mode, the RESET pin must be permanently tied high. SCLK and SEN are used as parallel control pins in this mode. This pin has an internal 100k $\Omega$ pull-down resistor.
SCLK	13	1	Input	This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode selection when RESET is tied high; see Table 6 for detailed information. This pin has an internal $100k\Omega$ pull-down resistor.
SDATA	14	1	Input	Serial interface data input; this pin has an internal $100k\Omega$ pull-down resistor.
SEN	15	1	Input	This pin functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see Table 7 for detailed information. This pin has an internal $150k\Omega$ pull-up resistor to AVDD.
SDOUT	64	1	Output	This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin forces a logic low and is not put in 3-state.
CTRL1	35	1	Input	Digital control input pins. Together, they control the SNRBoost <sup>3G</sup> , power-down, and multiplexed modes.
CTRL2	36	1	Input	Digital control input pins. Together, they control the SNRBoost <sup>3G</sup> , power-down, and multiplexed modes.
CTRL3	37	1	Input	Digital control input pins. Together, they control the SNRBoost <sup>3G</sup> , power-down, and multiplexed modes.
CLKOUT_P	57	1	Output	Differential output clock, true
CLKOUT_M	56	1	Output	Differential output clock, complement
CHA0_P, CHA0_M	Refer to Figure 2	2	Output	Channel A differential output data pair, 0 and D0 multiplexed
CHA2_P, CHA2_M	Refer to Figure 2	2	Output	Channel A differential output data D1 and D2 (multiplexed and true)
CHA4_P, CHA4_M	Refer to Figure 2	2	Output	Channel A differential output data D3 and D4 (multiplexed and true)
CHA6_P, CHA6_M	Refer to Figure 2	2	Output	Channel A differential output data D5 and D6 (multiplexed and true)
CHA8_P, CHA8_M	Refer to Figure 2	2	Output	Channel A differential output data D7 and D8 (multiplexed and true)
CHA10_P, CHA10_M	Refer to Figure 2	2	Output	Channel A differential output data D9 and D10 (multiplexed and true)
CHB0_P, CHB0_M	Refer to Figure 2	2	Output	Channel B differential output data pair, 0 and D0 multiplexed
CHB2_P, CHB2_M	Refer to Figure 2	2	Output	Channel B differential output data D1 and D2 (multiplexed and true)
CHB4_P, CHB4_M	Refer to Figure 2	2	Output	Channel B differential output data D3 and D4 (multiplexed and true)
CHB6_P, CHB6_M	Refer to Figure 2	2	Output	Channel B differential output data D5 and D6 (multiplexed and true)
CHB8_P, CHB8_M	Refer to Figure 2	2	Output	Channel B differential output data D7 and D8 (multiplexed and true)
CHB10_P, CHB10_M	Refer to Figure 2	2	Output	Channel B differential output data D9 and D10 (multiplexed and true)
DRVDD	1, 48	2	Input	Output buffer supply
DRGND	49, PAD	2	Input	Output buffer ground
NC	Refer to Figure 2	1		Do not connect

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(4) The PowerPAD is connected to DRGND.

(5) NC = no connection.

# Figure 3. ADS58C28 CMOS Pinout

### Pin Assignments (CMOS Mode)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
AVDD	16, 22, 33, 34	4	Input	Analog power supply
AGND	17, 18, 21, 24, 27, 28, 31, 32	8	Input	Analog ground
CLK_P	25	1	Input	Differential clock positive input
CLK_M	26	1	Input	Differential clock negative input
INA_P	29	1	Input	Differential analog positive input, channel A
INA_M	30	1	Input	Differential analog negative input, channel A
INB_P	19	1	Input	Differential analog positive input, channel B
INB_M	20	1	Input	Differential analog negative input, channel B
СМ	23	1	Output	This pin outputs the common-mode voltage (0.95V) that can be used externally to bias the analog input pins

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# Pin Assignments (CMOS Mode) (continued)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
RESET	12	1	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the <i>Serial Interface Configuration</i> section. In parallel interface mode, the RESET pin must be permanently tied high. SDATA and SEN are used as parallel control pins in this mode. This pin has an internal 100k $\Omega$ pull-down resistor.
SCLK	13	1	Input	This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode when RESET is tied high; see Table 6 for detailed information. This pin has an internal $100k\Omega$ pull-down resistor.
SDATA	14	1	Input	Serial interface data input; this pin has an internal $100k\Omega$ pull-down resistor.
SEN	15	1	Input	This pin functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see Table 7 for detailed information. This pin has an internal $150k\Omega$ pull-up resistor to AVDD.
SDOUT	64	1	Output	This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin forces a logic low and is not put in 3-state.
CTRL1	35	1	Input	Digital control input pins. Together, they control various power-down modes.
CTRL2	36	1	Input	Digital control input pins. Together, they control various power-down modes.
CTRL3	37	1	Input	Digital control input pins. Together, they control various power-down modes.
CLKOUT	57	1	Output	CMOS output clock
CHA_D0 to CHA_D10	Refer to Figure 3	11	Output	Channel A ADC output data bits, CMOS levels
CHB_D0 to CHB_D10	Refer to Figure 3	11	Output	Channel B ADC output data bits, CMOS levels
DRVDD	1, 48	2	Input	Output buffer supply
DRGND	49, PAD	2	Input	Output buffer ground
NC	Refer to Figure 3	1	—	Do not connect
UNUSED	56	1		This pin is not used in the CMOS interface



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# FUNCTIONAL BLOCK DIAGRAM





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# TIMING CHARACTERISTICS: LVDS AND CMOS MODES<sup>(1)</sup>

Typical values are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 200MSPS, sine wave input clock,  $C_{LOAD} = 5pF^{(2)}$ , and  $R_{LOAD} = 100\Omega^{(3)}$ , unless otherwise noted.

Minimum and maximum values are across the full temperature range:  $T_{MIN} = -40$ °C to  $T_{MAX} = +85$ °C, AVDD = 1.8V, and DRVDD = 1.7V to 1.9V.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>A</sub>	Aperture delay		0.5	0.8	1.1	ns
	Aperture delay matching	Between the two channels of the same device		±70		ps
	Variation of aperture delay	Between two devices at the same temperature and DRVDD supply		±150		ps
tj	Aperture jitter			140		f <sub>S</sub> rms
	Mini and the s	Time to valid data after coming out of STANDBY mode		50	100	μs
	wakeup time	Time to valid data after coming out of GLOBAL power-down mode	0.50.81.1en the two channels of the same device $\pm 70$ en two devices at the same temperature and D supply $\pm 150$ 140140o valid data after coming out of STANDBY5010050o valid data after coming out of GLOBAL -down mode100500100o valid data after coming out of GLOBAL -down mode100100500that after reset, DIGITAL MODE1 = 0, AL MODE2 = 016AL MODE2 = 117cost <sup>3G</sup> , gain and offset corr enabled, DIGITAL :1 = 1, DIGITAL MODE2 = 0 or 124ralid <sup>(6)</sup> to zero-crossing of CLKOUTP1.051.5rrossing of CLKOUTP1.05clock rising edge cross-over to output clock edge cross-overS < Sampling frequency ≤ 200MSPS	μs		
		Default latency after reset, DIGITAL MODE1 = 0, DIGITAL MODE2 = 0		16		Clock cycles
	ADC latency <sup>(4)</sup>	SNRBoost <sup>3G</sup> only enabled, DIGITAL MODE1 = 0, DIGITAL MODE2 = 1		17		Clock cycles
		SNRBoost <sup>3G</sup> , gain and offset corr enabled, DIGITAL MODE1 = 1, DIGITAL MODE2 = 0 or 1		24		Clock cycles
DDR LVD	OS MODE <sup>(5)</sup>					
t <sub>SU</sub>	Data setup time <sup>(6)</sup>	Data valid <sup>(6)</sup> to zero-crossing of CLKOUTP	1.05	1.5		ns
t <sub>H</sub>	Data hold time <sup>(6)</sup>	Zero-crossing of CLKOUTP to data becoming invalid <sup>(6)</sup>	0.35	0.6		ns
t <sub>PDI</sub>	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over 1MSPS ≤ Sampling frequency ≤ 200MSPS	5.1	6.4	7.7	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP-CLKOUTM) 1MSPS ≤ Sampling frequency ≤ 200MSPS		50%		
t <sub>RISE</sub> , t <sub>FALL</sub>	Data rise time, Data fall time	Rise time measured from -100mV to +100mV Fall time measured from +100mV to -100mV 1MSPS ≤ Sampling frequency ≤ 200MSPS		0.13		ns
t <sub>CLKRISE</sub> , t <sub>CLKFALL</sub>	Output clock rise time, Output clock fall time	Rise time measured from -100mV to +100mV Fall time measured from +100mV to -100mV 1MSPS ≤ Sampling frequency ≤ 200MSPS		0.13		ns
PARALLI	EL CMOS MODE					
t <sub>START</sub>	Input clock to data delay	Input clock rising edge crossover to start of data valid		0.06	1.5	ns
t <sub>DV</sub>	Data valid time	Time interval of data valid	3.1	3.6		ns
	Output clock duty cycle	Duty cycle of output clock, CLKOUT 1MSPS $\leq$ Sampling frequency $\leq$ 150MSPS <sup>(7)</sup>		44		%
t <sub>RISE</sub> , t <sub>FALL</sub>	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD $1 \leq Sampling frequency \leq 200MSPS$		1		ns
t <sub>CLKRISE</sub> , t <sub>CLKFALL</sub>	Output clock rise time Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD $1 \leq Sampling frequency \leq 150MSPS$		1		ns

(1) Timing parameters are ensured by design and characterization and not tested in production.

(2) C<sub>LOAD</sub> is the effective external single-ended load capacitance between each output pin and ground

(3) R<sub>LOAD</sub> is the differential load resistance between the LVDS output pair.

(4) At higher frequencies,  $t_{PDI}$  is greater than one clock period and overall latency = ADC latency + 1.

(5) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.

(6) Data valid refers to a logic high of +100mV and a logic low of -100mV.

(7) In CMOS mode, the output clock should be used only up to 150MSPS. See Figure 69 for a simple capture scheme above 150MSPS.

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SAMPLING FREQUENCY	SETUP TIME (ns)			HOLD TIME (ns)			t <sub>PDI</sub> , CLOCK PROPAGATION DELAY (ns) <sup>(1)</sup>		
(MSPS)	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
185	1.1	1.7		0.35	0.6		5.1	6.4	7.7
170	1.3	1.9		0.35	0.6		5.1	6.4	7.7
150	1.7	2.3		0.35	0.6		5.1	6.4	7.7
125	2.3	3		0.35	0.6		5.1	6.4	7.7

# Table 3. LVDS Timings at Lower Sampling Frequencies

(1) At higher frequencies,  $t_{PDI}$  is greater than one clock period and overall latency = ADC latency + 1.

Table 4. (	CMOS	Timings at	Lower	Sampling	Freque	ncies
------------	------	------------	-------	----------	--------	-------

SAMPLING FREQUENCY (MSPS)	TIMINGS SPECIFIED WITH RESPECT TO CLKOUT									
	SETUP TIME (ns)		HOLD TIME (ns)			t <sub>PDI</sub> , CLOCK PROPAGATION DELAY (ns) <sup>(1)</sup>				
	MIN	ТҮР	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
150	1.2	2.6		2.1	2.8		5.5	7	8.5	
125	2	3.2		2.8	3.5		5.5	7	8.5	
105	2.8	4		3.5	4.2		5.5	7	8.5	
80	4.3	5.5		5	5.7		5.5	7	8.5	

(1) At higher frequencies,  $t_{PDI}$  is greater than one clock period and overall latency = ADC latency + 1.



- (1) ADC latency after reset; at higher frequencies, t<sub>PDI</sub> is greater than one clock period and overall latency = ADC latency + 1.
- (2) E = even bits (D0, D2, D4, etc.); O = odd bits (D1, D3, D5, etc.).



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(1) Dn = bits D0, D2, D4, etc.

(2) Dn + 1 = bits D1, D3, D5, etc.





(1) Dn = bits D0, D1, D2, etc. of channels A and B.

Figure 7. CMOS Mode Timing



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# **DEVICE CONFIGURATION**

The ADS58C28 can be configured independently using either parallel interface control or serial interface programming.

# PARALLEL CONFIGURATION ONLY

To put the device into parallel configuration mode, keep RESET tied high (AVDD). Then, use the SEN, SCLK, CTRL1, CTRL2, and CTRL3 pins to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in Table 5 to Table 8). There is no need to apply a reset and SDATA can be connected to ground.

In this mode, SEN and SCLK function as parallel interface control pins. Some frequently-used functions can be controlled using these pins. Table 5 describes the modes controlled by the parallel pins.

PIN	CONTROL MODE
SCLK	Low-speed mode selection
SEN	Output data format and output interface selection
CTRL1	
CTRL2	Together, these pins control the SNRBoost <sup>3G</sup> and power-down modes.
CTRL3	

# Table 5. Parallel Pin Definition

# SERIAL INTERFACE CONFIGURATION ONLY

To exercise this mode, the serial registers must first be reset to the default values and the RESET pin must be kept low. SEN, SDATA, and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC. The registers can be reset either by applying a pulse on the RESET pin or by setting the RESET bit high. The *Serial Register Map* section describes the register programming and the register reset process in more detail.

# **USING BOTH SERIAL INTERFACE AND PARALLEL CONTROLS**

For increased flexibility, a combination of serial interface registers and parallel pin controls (CTRL1 to CTRL3) can also be used to configure the device. To enable this flexibility, keep RESET low. The parallel interface control pins CTRL1 to CTRL3 are available. After power-up, the device is automatically configured according to the voltage settings on these pins (see Table 8). SEN, SDATA, and SCLK function as serial interface digital pins and are used to access the internal registers of the ADC. The registers must first be reset to the default values either by applying a pulse on the RESET pin or by setting the RESET bit to '1'. After reset, the RESET pin must be kept low. The *Serial Register Map* section describes register programming and the register reset process in more detail.

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# DETAILS OF PARALLEL CONFIGURATION ONLY

The functions controlled by each parallel pin are described in Table 6, Table 7, and Table 8. A simple way of configuring the parallel pins is shown in Figure 8.

## Table 6. SCLK Control Pin

VOLTAGE APPLIED ON SCLK	DESCRIPTION
0V to 0.9V	Low-speed mode is disabled
0.9V to AVDD	Low-speed mode is enabled

## Table 7. SEN Control Pin

VOLTAGE APPLIED ON SEN	DESCRIPTION
0 (+50mV/–0mV)	Twos complement and parallel CMOS output
(3/8) AVDD (±50mV)	Offset binary and parallel CMOS output
(5/8) 2AVDD (±50mV)	Offset binary and DDR LVDS output
AVDD (+0mV/–50mV)	Twos complement and DDR LVDS output

# Table 8. CTRL1, CTRL2, and CTRL3 Pins

CTRL1	CTRL2	CTRL3	DESCRIPTION
Low	Low	Low	Normal operation; SNRBoost <sup>3G</sup> disabled for both channels
Low	Low	High	SNRBoost <sup>3G</sup> enabled for channel B
Low	High	Low	SNRBoost <sup>3G</sup> enabled for channel A
Low	High	High	SNRBoost <sup>3G</sup> enabled for channel A and B
High	Low	Low	Global power-down
High	Low	High	Channel A powered down, channel B is active
High	High	Low	Do not use
High	High	High	MUX mode of operation, channel A and B data are multiplexed and output on the CHB_D[10:0] pins.







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# DETAILS OF SERIAL INTERFACE

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequencies from 20MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

## **Register Initialization**

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

- 1. Either through hardware reset by applying a high pulse on the RESET pin (of width greater than 10ns), as shown in Figure 9; or
- By applying a software reset. When using the serial interface, set the RESET bit (D7 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.



Figure 9. Serial Interface Timing

	PARAMETER	MIN	TYP	MAX	UNIT
f <sub>SCLK</sub>	SCLK frequency (equal to 1/t <sub>SCLK</sub> )	> DC		20	MHz
t <sub>SLOADS</sub>	SEN to SCLK setup time	25			ns
t <sub>SLOADH</sub>	SCLK to SEN hold time	25			ns
t <sub>DSU</sub>	SDATA setup time	25			ns
t <sub>DH</sub>	SDATA hold time	25			ns

	Table 9.	Serial	Interface	Timing	Characteristics <sup>(</sup>	1)
--	----------	--------	-----------	--------	------------------------------	----

(1) Typical values at +25°C; minimum and maximum values across the full temperature range:  $T_{MIN} = -40$ °C to  $T_{MAX} = +85$ °C, AVDD = 1.8V, and DRVDD = 1.8V, unless otherwise noted.

### Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

- 1. Set the READOUT register bit to '1'. This setting disables any further writes to the registers.
- 2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
- 3. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin (pin 64).
- 4. The external controller can latch the contents at the SCLK falling edge.
- 5. To enable register writes, reset the READOUT register bit to '0'.

The serial register readout works with both CMOS and LVDS interfaces on pin 64.

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When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float.



b) Read contents of Register 45h. This register has been initialized with 04h (device is put into global power-down mode.)

(1) The SDOUT pin functions as a serial readout (READOUT = 1).

# Figure 10. Serial Readout Timing Diagram

Table 10. Reset Timing (Only when Serial Interface is Used) <sup>(1)</sup>							
ARAMETER	CONDITIONS	MIN	TY				

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>1</sub>	Power-on delay	Delay from AVDD and DRVDD power-up to active RESET pulse	1			ms
			10			ns
t <sub>2</sub> Rese	Reset pulse width	Active RESET signal pulse width			1	μs
t <sub>3</sub>	Register write delay	Delay from RESET disable to SEN active	100			ns

Typical values at +25°C; minimum and maximum values across the full temperature range: T<sub>MIN</sub> = -40°C to T<sub>MAX</sub> = +85°C, unless (1)otherwise noted.







NOTE: A high pulse on the RESET pin is required in the serial interface mode when initialized through a hardware reset. For parallel interface operation, RESET must be permanently tied high.

# Figure 11. Reset Timing Diagram

# SERIAL REGISTER MAP

Table 11 summarizes the functions supported by the serial interface.

Table 11. Serial Interface Register Map <sup>(1)</sup>	
--	--

REGISTER ADDRESS		REGISTER DATA									
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0			
00	0	0	0	0	0	0	RESET	READOUT			
01			LVDS	SWING			0	0			
03	0	0	0	0	0	0	HIGH PE	RF MODE			
25		CH A	GAIN		0	CH	A TEST PATTER	RNS			
26	0			CH A SNF	RBoost <sup>3G</sup> FILTER	NUMBER					
28	0	CH A SNRBoost <sup>3G</sup> ON	0	0	0	0	0	0			
29	0	0	0	DATA F	ORMAT	0	0	0			
2B		CH B	GAIN		0	СН	B TEST PATTER	RNS			
2D	0			CH B SNF	RBoost <sup>3G</sup> FILTER	NUMBER					
2E	0	CH B SNRBoost <sup>3G</sup> ON	0	0	0	0	0	0			
3D	0	0	ENABLE OFFSET CORR	0	0	0	0	0			
3F	0	0		TTERN D[10:5]		•					
40		CUS	TOM PATTERN	D[4:0]	0	0	0				
41	LVDS	CMOS	CMOS CLKO	JT STRENGTH	0	0	0	0			
42	0	0	0	0	DIGITAL MODE 1	0	0	0			
44	0	0	0	0	0	0	0	DIGITAL MODE 2			
45	STBY	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH	0	0	PDN GLOBAL	0	0			
4A	0	0	0	0	0	0	0	HIGH FREQ MODE CH B			
58	0	0	0	0	0	0	0	HIGH FREQ MODE CH A			
BF	CH A	OFFSET PEDE	STAL	0	0	0	0	0			
C1	CH E	B OFFSET PEDE	STAL	0	0	0	0	0			
CF	FREEZE OFFSET CORR	0		OFFSET CORR	TIME CONSTAN	г	0	0			
DB	0	0	0	0	0	0	0	LOW SPEED MODE CH B			
EA	OVERRIDE SNRBoost <sup>3G</sup> PINS	0	0	0	0	0	0	0			
EF	0	0	0	EN LOW SPEED MODE	0	0	0	0			
F1	0	0	0	0	0	0	EN LVD	S SWING			
F2	0	0	0	0	LOW SPEED	0	0	0			

(1) All registers default to '0' after reset.



# **DESCRIPTION OF SERIAL REGISTERS**

		Regis	ster Address (	0h (Default	= 00h)		
7	6	5	4	3	2	1	0
0	0	0	0	0	0	RESET	READOUT
Bits[7:2]	Always write '0	)'					
Bit 1	RESET: Softwa	are reset app	lied				
	This bit resets a	all internal regi	isters to the de	fault values a	and self-clears to	o 0 (default =	- 1).
Bit O	READOUT: Se	rial readout					
	This bit sets the 0 = Serial reado 1 = Serial reado levels running fi	e serial readou out of registers out enabled; th rom the DRVE	it of the registe s disabled; the ne SDOUT pin DD supply. See	rs. SDOUT pin is functions as the <i>Serial R</i> a	s placed in a hig a serial data rea egister Readour	gh-impedanc adout with CN t section.	e state. ∕IOS logic
		Regis	ster Address (	)1h (Default	= 00h)		
7	6	5	4	3	2	1	0
	These bits prog swing. 000000 = Defau 011011 = LVDS 110010 = LVDS 010100 = LVDS 111110 = LVDS 001111 = LVDS	ram the LVDS ult LVDS swing S swing increa S swing increa S swing increa S swing increa S swing increa	S swing. Set the g; $\pm 350$ with ses to $\pm 410$ mV ses to $\pm 465$ mV ses to $\pm 570$ mV ses to $\pm 200$ mV ses to $\pm 125$ mV	e EN LVDS S n external 100 / / / /	WING bit to '1' 0Ω termination	before progra	amming
Bits[1:0]	Always write '(	)'					
		Regis	ster Address (	)3h (Default	= 00h)		
7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH PE	ERF MODE
Bits[7:2] Bits[1:0]	Always write '( HIGH PERF M(	)' DDE: High-pe	erformance mo	ode			
	These bits enab 00 = Default pe	ole LVDS swin	ng control using	the LVDS S	WING register I	oits.	

01 = Do not use

10 = Do not use

11 = Obtain best performance across sample clock and input signal frequencies

7	6	5	4	3	2	1	0
	CH A	GAIN		0	(	CH A TEST PATTERN	٧S
Bits[7:4]	CH A GAIN: CI	hannel A gain	programma	bility			
	These bits set t	he gain progra	ammability in (	0.5dB steps fo	r channel A.		
	0000 = 0dB gai	n (default afte	r reset)				
	0001 = 0.5dB g	ain					
	0010 = 10B  gai	n Jain					
	0100 = 2dB gai	n					
	0101 = 2.5dB g	ain					
	0110 = 3dB gai	n					
	0111 = 3.5 dB g 1000 = 4 dB gai	ain n					
	1000 = 400 gal 1001 = 4.5dB g	lain					
	1010 = 5dB gai	n					
	1011 = 5.5 dB g	ain					
D:4 0							
Bit 3	Always write '	U <sup>.</sup>					
Bits[2:0]	CH A TEST PA	TTERNS: Ch	annel A data	capture			
	These bits verif	y data capture	for channel A	A; see Table 1	2.		
	000 = Normal o 001 = Outputs a	peration					
	010 = Outputs a	all 1s					
	011 = Outputs t	toggle pattern;	D[10:0] outpu	ut data are an	alternating s	equence of 1010	1010101 and
	100 = Outputs d	digital ramp: o	utput data inc	rements by 1L	SB (11 bits)	everv eighth cloc	k cvcle from
	code 0 to code	2047			- ( )	, , , , , , , , , , , , , , , , , , , ,	- <b>)</b>
	101 = Outputs of 101	custom patterr	n; use register	s 3Fh and 40h	n to set the c	ustom pattern	
	110 = Unused						
		Regis	ter Address	26h (Default =	= 00h)		
7	e	F	4	2	2	1	0

Register Address 25h (Default = 00h)

#### 6 0 5 3 CH A SNRBoost<sup>3G</sup> FILTER NUMBER 0

#### Always write '0' Bit 7

#### CH A SNRBoost<sup>3G</sup> FILTER NUMBER: Channel A SNRBoost<sup>3G</sup> filter selection Bits[6:0]

These bits select any one of 55 SNRBoost<sup>3G</sup> filters for channel A **only** after selecting the appropriate mode from Table 12; refer to the SNR Enhancement Using SNRBoost section.

# Register Address 28h (Default = 00h)

7	6	5	4	3	2	1	0
0	CH A SNRBoost <sup>3G</sup> ON	0	0	0	0	0	0

#### Always write '0' Bit 7

#### CH A SNRBoost<sup>3G</sup> ON: Channel A SNRBoost<sup>3G</sup> setting Bit 6

This bit sets the SNRBoost<sup>3G</sup> for channel A  $0 = SNRBoost^{3G}$  for channel A is off

 $1 = SNRBoost^{3G}$  for channel A is on

#### Always write '0' Bits[5:0]

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		Rec	nister Addre	ss 29h (Defaul	t = 00h		
7	6	5	4	33 2011 (Delidul	2 2	1	0
0	0	0	DA1		0	0	0
Bits[7:5]	Always write '0'	,					
Bits[4:3]	DATA FORMAT	: Data form	nat selection	n			
	00 = Twos comp 01 = Twos comp 10 = Twos comp 11 = Offset binar	olement olement olement ry					
Bits[2:0]	Always write '0'	ı					
		Reg	gister Addres	ss 2Bh (Defau	lt = 00h)		
7	6	5	4	3	2	1	0
	CH B G	AIN		0		CH B TEST PATTE	RNS
Bits[7:4]	CH B GAIN: Ch	annel B ga	ain programi	mability			
	0000 = 0dB gain 0001 = 0.5dB gain 0010 = 1dB gain 0011 = 1.5dB gain 0100 = 2dB gain 0101 = 2.5dB gain 0101 = 3dB gain 0111 = 3.5dB gain 1000 = 4dB gain 1001 = 4.5dB gain 1010 = 5dB gain 1011 = 5.5dB gain 1001 = 6dB gain	(default af in in in in in in	ter reset)				
Bit 3	Always write '0'	I					
Bits[2:0]	CH B TEST PAT	TTERNS: C	Channel B da	ata capture			
	These bits verify 000 = Normal op 001 = Outputs al 010 = Outputs al 011 = Outputs to 01010101010 100 = Outputs di code 0 to code 2 101 = Outputs cu 110 = Unused	data captu peration II 0s II 1s pggle patter igital ramp; 2047 ustom patter	ure for chann rn; D[10:0] ou output data ern; use regis	el B; see Table utput data are a increments by sters 3Fh and 4	12. In alternating 1LSB (11 bit Oh to set the	g sequence of <i>101</i> s) every eighth clo e custom pattern	<i>01010101</i> and ock cycle from

111 = Unused

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Register Address 2Dh (Default = 00h)											
7	6	5	4	3	2	1	0				
0	CH B SNRBoost <sup>3G</sup> FILTER NUMBER										

# Bit 7 Always write '0'

# Bits[6:0] CH B SNRBoost<sup>3G</sup> FILTER NUMBER: Channel B SNRBoost<sup>3G</sup> filter selection

These bits select any one of 55 SNRBoost<sup>3G</sup> filters for channel B **only** after selecting the appropriate mode from Table 12; refer to the *SNR Enhancement Using SNRBoost* section.

# Register Address 2Eh (Default = 00h)

7	6	5	4	3	2	1	0
0	CH B SNRBoost <sup>3G</sup> ON	0	0	0	0	0	0

# Bit 7 Always write '0'

# Bit 6 CH B SNRBoost<sup>3G</sup> ON: Channel B SNRBoost<sup>3G</sup> setting

This bit sets the SNRBoost<sup>3G</sup> for channel B

 $0 = SNRBoost^{3G}$  for channel B is off

1 = SNRBoost<sup>3G</sup> for channel B is on

# Bits[5:0] Always write '0'

# Register Address 3Dh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	ENABLE OFFSET CORR	0	0	0	0	0

# Bits[7:6] Always write '0'

# Bit 5 ENABLE OFFSET CORR: Offset correction setting

This bit sets the offset correction; see Table 12.

0 = Offset correction disabled

1 = Offset correction enabled

# Bits[4:0] Always write '0'

# Register Address 3Fh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8	CUSTOM PATTERN D7	CUSTOM PATTERN D6	CUSTOM PATTERN D5

# Bits[7:6] Always write '0'

# Bits[7:0] CUSTOM PATTERN D[10:5]

These are the six custom pattern upper bits available at output instead of ADC data.

# Register Address 40h (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D4	CUSTOM PATTERN D3	CUSTOM PATTERN D2	CUSTOM PATTERN D1	CUSTOM PATTERN D0	0	0	0

# Bits[7:3] CUSTOM PATTERN D[4:0]

These are the five lower custom pattern bits available at output instead of ADC data.

# Bits[2:0] Always write '0'

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		Re	egister Address	41h (Defaul	t = 00h)								
7	6	5	4	3	2	2	1		0				
LVI	DS CMOS	CMOS CL	KOUT STRENGTH	0	C	)	0		0				
Bits[7:6]	LVDS CMOS:	Interface s	election										
	These bits sele 00 = DDR LVD 01 = Parallel C 10 = Parallel C 11 = Parallel C	<ul> <li>I hese bits select the interface.</li> <li>00 = DDR LVDS interface</li> <li>01 = Parallel CMOS interface</li> <li>10 = Parallel CMOS interface</li> <li>11 = Parallel CMOS interface</li> </ul>											
Bits[5:4]	CMOS CLKOU	JT STRENG	GTH										
	These bits con 00 = Maximum 01 = Medium s 10 = Low stren 11 = Very low s	These bits control the strength of the CMOS output clock. 00 = Maximum strength (recommended) 01 = Medium strength 10 = Low strength 11 = Very low strength											
Bits[3:0]	Always write '	0'											
	-	D	aiotor Addrooo	12h (Defaul	4 - 00h)								
7	6	κŧ			t = 00n)		2	1	0				
0	0		0	0	DIGITAL N	MODE 1	0	0	0				
Bits[7·4]	Always write '	0'	L		1	L		1	4				
Bit 3	DIGITAL MOD	е Е 1											
	See Table 12.												
Bits[2:0]	Always write '	0'											
	· · · · · <b>,</b> · · · · · ·	-											
		Re	egister Address	44h (Defaul	t = 00h)								
7	6	5	4	3	2	1							
0	0	0	0	0	0	0			DDE 2				
Bits[7:1]	Always write '	0'											
Bit 0	DIGITAL MOD	E 2											
	Refer to the Di	igital Functi	ons section.										

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## Register Address 45h (Default = 00h)

7	6	5	4	3	2	1	0
STBY	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH	0	0	PDN GLOBAL	0	0

# Bit 7 STBY: Standby setting

0 = Normal operation

1 = Both channels are put in standby; wakeup time from this mode is fast (typically 50µs).

# Bit 6 LVDS CLKOUT STRENGTH: LVDS output clock buffer strength setting

0 = LVDS output clock buffer at default strength to be used with  $100\Omega$  external termination 1 = LVDS output clock buffer has double strength to be used with  $50\Omega$  external termination

# Bit 5 LVDS DATA STRENGTH

0 = AII LVDS data buffers at default strength to be used with  $100\Omega$  external termination 1 = AII LVDS data buffers have double strength to be used with  $50\Omega$  external termination

# Bits[4:3] Always write '0'

# Bit 2 PDN GLOBAL

0 = Normal operation

1 = Total power down; all ADC channels, internal references, and output buffers are powered down. Wakeup time from this mode is slow (typically 100µs).

# Bits[1:0] Always write '0'

# Register Address 4Ah (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HIGH FREQ MODE CH B

# Bits[7:1] Always write '0'

# Bit 0 HIGH FREQ MODE CH B: Channel B high-frequency mode selection

This bit configures the high-frequency mode for channel B. This bit is recommended for high input signal frequencies greater than 200MHz.

0 = Default performance after reset

1 = Set this bit for each channel for high input frequencies

# Register Address 58h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HIGH FREQ MODE CH A

# Bits[7:1] Always write '0'

# Bit 0 HIGH FREQ MODE CH A: Channel A high-frequency mode selection

This bit configures the high-frequency mode for channel A. This bit is recommended for high input signal frequencies greater than 200MHz.

0 = Default performance after reset

1 = Set this bit for each channel for high input frequencies



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	Register Address BFh (Default = 00h)											
7	6	5	4	3	2	1	0					
СН	A OFFSET PEDES	STAL	0	0	0	0	0					

# Bits[7:5] CH A OFFSET PEDESTAL: Channel A offset pedestal selection

When the offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits. See the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.

100 = Pedestal is 4LSB

011 = Pedestal is 3LSB 010 = Pedestal is 2LSB 001 = Pedestal is 1LSB 000 = Pedestal is 0LSB 111 = Pedestal is -1LSB 110 = Pedestal is -2LSB 101 = Pedestal is -3LSB

# Bits[4:0] Always write '0'

# Register Address C1h (Default = 00h)

7	6	5	4	3	2	1	0
CH E	B OFFSET PEDES	STAL	0	0	0	0	0

# Bits[7:5] CH B OFFSET PEDESTAL: Channel B offset pedestal selection

When the offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits. See the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.

100 = Pedestal is 4LSB 011 = Pedestal is 3LSB 010 = Pedestal is 2LSB 001 = Pedestal is 1LSB 000 = Pedestal is 0LSB 111 = Pedestal is -1LSB 110 = Pedestal is -2LSB 101 = Pedestal is -3LSB

# Bits[4:0] Always write '0'

			Register A	ddress CFh (De	fault = 00h)						
	7	6	5	4	3	2	1	0			
FREEZE OF	FSET CORR	0		OFFSET CORR	TIME CONSTANT		0	0			
Bit 7	Bit 7 FREEZE OFFSET CORR: Freeze offset correction setting										
	This bit set 0 = Estima 1 = Estima the last est section.	tion of offs tion of offs tion of offs timated va	ze offset corre set correction set correction lue is used fo	ection estimation. is not frozen (the is frozen (the EN r offset correctior	EN OFFSET CO OFFSET CORR of every clock c	ORR bit must be bit must be set ycle. See the O	set) ); when ffset Co	frozen, <i>rrection</i>			
Bit 6	Always wr	'ite '0'									
Bits[5:2]	OFFSET C	ORR TIM	E CONSTAN	т							
	The offset	correction	loop time cor	stant in number	of clock cycles. R	efer to the Offs	et Corre	ection			

# section.

#### Always write '0' Bits[1:0]

# Register Address DBh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	LOW SPEED MODE CH B

#### Always write '0' Bits[7:1]

#### Bit 0 LOW SPEED MODE CH B: Channel B low-speed mode enable

This bit enables the low-speed mode for channel B. Set the EN LOW SPEED MODE bit to '1' before using this bit.

0 = Low-speed mode is disabled for channel B

1 = Low-speed mode is enabled for channel B

# Register Address EAh (Default = 00h)

7	6	5	4	3	2	1	0
OVERRIDE SNRBoost <sup>3G</sup> PINS	0	0	0	0	0	0	0

#### **OVERRIDE SNRBoost<sup>3G</sup> PINS** Bit 7

Refer to the SNR Enhancement Using SNRBoost section.

#### Bits[6:0] Always write '0'

# Register Address EFh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	EN LOW SPEED MODE	0	0	0	0

#### Bits[7:5] Always write '0'

#### Bit 4 EN LOW SPEED MODE: Enable control of low-speed mode through serial register bits

This bit enables the control of the low-speed mode using the ENABLE LOW SPEED MODE CH B and ENABLE LOW SPEED MODE CH A register bits.

0 = Low-speed mode is controlled by dc voltage on the SCLK pin

1 = Low-speed mode is controlled by serial register bits

#### Always write '0' Bits[3:0]



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		Regi	ister Address	F1h (Default	= 00h)		
7	6	5	4	3	2	1	0
0	0	0	0	0	0	EN LVD	S SWING
Bits[7:2]	Always write '	'0'					
Bits[1:0]	EN LVDS SWI	NG: LVDS sv	ving enable				
	These bits ena 00 = LVDS swi 01 = Do not us 10 = Do not us	ble LVDS swi ing control usi e e	ng control usin ing the LVDS S	g the LVDS S WING registe	SWING register er bits is disable	bits. ed	

11 = LVDS swing control using the LVDS SWING register bits is enabled

# Register Address F2h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	LOW SPEED MODE CH A	0	0	0

# Bits[7:4] Always write '0'

# Bit 3 LOW SPEED MODE CH A: Channel A low-speed mode enable

This bit enables the low-speed mode for channel A. Set the EN LOW SPEED MODE bit to '1' before using this bit.

0 = Low-speed mode is disabled for channel A

1 = Low-speed mode is enabled for channel A

# Bits[2:0] Always write '0'



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# **TYPICAL CHARACTERISTICS**

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.





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# **TYPICAL CHARACTERISTICS (continued)**

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock.  $1.5V_{PP}$  differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.



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# **TYPICAL CHARACTERISTICS (continued)**

LVDS output interface, and 32k point FFT, unless otherwise noted.



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# **TYPICAL CHARACTERISTICS (continued)**

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock.  $1.5V_{PP}$  differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.





 TYPICAL CHARACTERISTICS (continued)

 All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V<sub>PP</sub>



Figure 30.



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## **TYPICAL CHARACTERISTICS (continued)**

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock.  $1.5V_{PP}$  differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.





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# **TYPICAL CHARACTERISTICS (continued)**

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.



65.2

64.9

64.6

64.3

64

-40

AVDD = 1.65

AVDD = 1.7

AVDD = 1.75

AVDD = 1.8

AVDD = 1.85

AVDD = 1.9

AVDD = 1.95

-15

10

Temperature (°C)

Figure 38.

SFDR (dBc)

80

78

76

74

72

70

-40

AVDD = 1.65

AVDD = 1.7 AVDD = 1.75

AVDD = 1.8

AVDD = 1.85

AVDD = 1.9

AVDD = 1.95

10

Temperature (°C)

Figure 37.

-15

Input Frequency = 150MHz

60

85

35

Input Frequency = 150MHz

60

85

35



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# **TYPICAL CHARACTERISTICS (continued)**

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock.  $1.5V_{PP}$  differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.



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AVDD = 1.8V

LVDS output interface, and 32k point FFT, unless otherwise noted. ANALOG POWER vs SAMPLING FREQUENCY



**TYPICAL CHARACTERISTICS (continued)** All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR

550

Default

Figure 45.

**DIGITAL POWER vs SAMPLING FREQUENCY** 

70 80 90 100

EXAS ISTRUMENTS

150

175

 $f_{IN} = 40 MHz$ 

 $f_{CM} = 10MHz, 50mV_{PP}$ 

SFDR = 79.36dBFS

200

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# **TYPICAL CHARACTERISTICS (continued)**

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock.  $1.5V_{PP}$  differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.







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# **TYPICAL CHARACTERISTICS: Contour**

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.



SPURIOUS-FREE DYNAMIC RANGE (0dB Gain)

SFDR (dBc) Figure 50.



Figure 51.



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# **TYPICAL CHARACTERISTICS: Contour (continued)**

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock.  $1.5V_{PP}$  differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.



SIGNAL-TO-NOISE RATIO (0dB Gain)

Figure 52.



SIGNAL-TO-NOISE RATIO (6dB Gain)



# **APPLICATION INFORMATION**

# THEORY OF OPERATION

The ADS58C28 is a dual-channel, 11-bit, analog-to-digital converter (ADC) with sampling rates up to 200MSPS. At every rising edge of the input clock, the analog input signal of each channel is simultaneously sampled. The sampled signal in each channel is converted by a pipeline of low-resolution stages. In each stage, the sampled and held signal is converted by a high-speed, low-resolution, flash sub-ADC. The difference (residue) between the stage input and the quantized equivalent is gained and propagates to the next stage. At every clock, each succeeding stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block and are processed digitally to create the final code, after a data latency of 16 clock cycles. The digital output is available as either DDR LVDS or parallel CMOS and coded in either straight offset binary or binary twos complement format.

# ANALOG INPUT

The analog input consists of a switched-capacitor based, differential sample-and-hold architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The IN\_P and IN\_M pins must be externally biased around a common-mode voltage of 0.95V, available on the VCM pin. For a full-scale differential input, each input pin (IN\_P and IN\_M) must swing symmetrically between VCM + 0.5V and VCM - 0.5V, resulting in a  $2V_{PP}$  differential input swing. The input sampling circuit has a high 3dB bandwidth that extends up to 550MHz (measured from the input pins to the sampled voltage).



Figure 54. Analog Input Equivalent Circuit



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### **Drive Circuit Requirements**

For optimum performance, the analog inputs must be driven differentially. This operation improves the common-mode noise immunity and even-order harmonic rejection. A  $5\Omega$  to  $15\Omega$  resistor in series with each input pin is recommended to damp out ringing caused by package parasitics.

SFDR performance can be limited as a result of several reasons, including the effects of sampling glitches; nonlinearity of the sampling circuit; and nonlinearity of the quantizer that follows the sampling circuit. Depending on the input frequency, sample rate, and input amplitude, one of these factors plays a dominant part in limiting performance. At very high input frequencies (greater than approximately 300MHz), SFDR is determined largely by the device sampling circuit nonlinearity. At low input amplitudes, the quantizer nonlinearity usually limits performance.

Glitches are caused by the opening and closing of the sampling switches. The driving circuit should present a low source impedance to absorb these glitches. Otherwise, glitches could limit performance, primarily at low input frequencies (up to approximately 200MHz). It is also necessary to present low impedance (less than  $50\Omega$ ) for the common-mode switching currents. This configuration can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The cutoff frequency of the R-C filter involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but it reduces the input bandwidth. On the other hand, with a higher cutoff frequency (smaller C), bandwidth support is maximized. However, the sampling glitches now must be supplied by the external drive circuit. This tradeoff has limitations as a result of the presence of the package bond-wire inductance.

In the ADS58C28, the R-C component values have been optimized while supporting high input bandwidth (up to 550MHz). However, in applications with input frequencies up to 200MHz to 300MHz, the filtering of the glitches can be improved further using an external R-C-R filter; see Figure 57 and Figure 58.

In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. Furthermore, the ADC input impedance must be considered. Figure 55 and Figure 56 show the impedance ( $Z_{IN} = R_{IN} || C_{IN}$ ) looking into the ADC input pins.







Figure 56. ADC Analog Input Capacitance (C<sub>IN</sub>) Across Frequency



# **Driving Circuit**

Two example driving circuit configurations are shown in Figure 57 and Figure 58—one optimized for low bandwidth (low input frequencies) and the other one for high bandwidth to support higher input frequencies. Note that both of the drive circuits have been terminated by  $50\Omega$  near the ADC side. The termination is accomplished by a  $25\Omega$  resistor from each input to the 0.95V common-mode (VCM) from the device. This allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch; good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 57, Figure 58, and Figure 59. The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective  $50\Omega$  (in the case of  $50\Omega$  source impedance).



Figure 57. Drive Circuit with Low Bandwidth (for Low Input Frequencies)



Figure 58. Drive Circuit with High Bandwidth (for High Input Frequencies)



Figure 59. Drive Circuit with Very High Bandwidth (Greater than 300MHz)



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All of these examples show 1:1 transformers being used with a  $50\Omega$  source. As explained in the *Drive Circuit Requirements* section, this configuration helps to present a low source impedance to absorb the sampling glitches. With a 1:4 transformer, the source impedance is  $200\Omega$ . Higher impedance can lead to degradation in performance, compared to the case with 1:1 transformers. For applications where only a band of frequencies are used, the drive circuit can be tuned to present a low impedance for the sampling glitches. Figure 60 shows an example with a 1:4 transformer, tuned for a band of approximately 150MHz.



Figure 60. Drive Circuit with a 1:4 Transformer

# **CLOCK INPUT**

The ADS58C28 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal  $5k\Omega$  resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources. Figure 61 shows a circuit for the internal clock buffer.



NOTE:  $C_{EQ}$  is 1pF to 3pF and is the equivalent input capacitance of the clock buffer.

Figure 61. Internal Clock Buffer

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A single-ended CMOS clock can be ac-coupled to the CLK\_P input, with CLK\_M connected to ground with a 0.1µF capacitor, as shown in Figure 62. For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input. Figure 63 shows a differential circuit.







# **DIGITAL FUNCTIONS**

The device has several useful digital functions such as test patterns, gain, offset correction, and SNRBoost<sup>3G</sup>. All of these functions can be controlled using two control bits (DIGITAL MODE 1 and DIGITAL MODE 2), as shown in Table 12.

DIGITAL MODE 1	DIGITAL MODE 2	DESCRIPTION				
0	0	Default				
0	1	SNRBoost <sup>3G</sup> enabled, test patterns, gain, and offset correction disabled				
1	0	SNRBoost <sup>3G</sup> , test patterns, gain, and offset correction enabled				
1	1	SNRBoost <sup>3G</sup> , test patterns, gain, and offset correction enabled				

## Table 12. Digital Functions Control Bits

# SNR ENHANCEMENT USING SNRBoost<sup>3G</sup>

SNRBoost<sup>3G</sup> technology makes it possible to overcome SNR limitations resulting from quantization noise. Using SNRBoost<sup>3G</sup>, enhanced SNR can be obtained for any bandwidth (less than Nyquist or  $f_S/2$ ; see Table 5). SNR improvement is achieved without affecting the default harmonic performance.

The ADS58C28 uses third-generation SNRBoost technology (SNRBoost<sup>3G</sup>) to achieve SNR enhancement over very wide bandwidths (up to 60MHz). When SNRBoost<sup>3G</sup> is enabled, the noise floor in the spectrum acquires a typical bathtub shape. The special feature of SNRBoost<sup>3G</sup> is the nearly flat noise floor within the entire band of the bathtub.

The position of the center of the bathtub and its bandwidth are programmable; the available bandwidths are 60MHz, 40MHz, 30MHz, and 20MHz. Several center frequency options are available for each bandwidth. The ADS58C28 includes 55 pre-programmed combinations of center frequency and bandwidth. Any one of these combinations can be selected by programming the Ch SNRBoost<sup>3G</sup> Filter Number register bits. Each channel can be programmed with independent center frequency and bandwidths.

One of the characteristics of SNRBoost<sup>3G</sup> is that the bandwidth scales with the sampling frequency. 60MHz and 40MHz bandwidths are achieved at a sampling rate of 184MHz; at higher sample rates, even higher bandwidths are possible. The lower 30MHz and 20MHz bandwidths are achieved at a sample rate of 200MHz; at lower sample rates, the achieved bandwidth is lower. Table 14 shows all combinations of center frequency for each bandwidth, specified as fractions of the sample rate. By positioning the bathtub within the desired signal band, SNR improvement can be achieved. Note that as the bandwidth increases, the amount of SNR improvement reduces. After reset, the SNRBoost<sup>3G</sup> function is disabled.



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To use SNRBoost<sup>3G</sup> with control pins, follow this exact sequence:

# Select and Enable the SNRBoost<sup>3G</sup> Filter

- 1. First, disable the DIGITAL MODE 1 and DIGITAL MODE 2 bits (set to '0').
- 2. Next, select the appropriate SNRBoost<sup>3G</sup> filter, using the Ch SNRBoost<sup>3G</sup> Filter number register bits.
- 3. Finally, set the DIGITAL MODE 2 bit (set to '1').

# Turn On/Off SNRBoost<sup>3G</sup>

1. Use the CTRL1, CTRL2, and CTRL3 pins to dynamically turn on/off the SNRBoost<sup>3G</sup> for each pair of channels.

To use SNRBoost<sup>3G</sup> without using control pins follow this exact sequence:

# Select and Enable the SNRBoost<sup>3G</sup> Filter

- 1. First, disable the DIGITAL MODE 1 and DIGITAL MODE 2 bits (set to '0').
- 2. Next, select the appropriate SNRBoost<sup>3G</sup> filter using the Ch SNRBoost Filter number register bits.
- 3. Then set the DIGITAL MODE 2 bit (set to '1').
- 4. Finally, set the SNRBoost<sup>3G</sup> pin override bit (OVERRIDE SNRBoost PINS).

# Turn On/Off SNRBoost<sup>3G</sup>

1. Turn on and off the SNRBoost<sup>3G</sup> for each channel using the SNRBoost CH A ON and SNRBoost CH B ON register bits.

# NOTE

To use a different SNRBoost<sup>3G</sup> filter, it is required to follow all the above steps in the exact order specified. Not following this order can result in incorrect operation of the SNRBoost<sup>3G</sup> filter. To turn on and off the filter without changing the filter number, simply follow the steps under the Turn On/Off SNRBoost<sup>3G</sup> outline.

Table 13 describes the SNRBoost<sup>3G</sup> control when used with the CTRL pins.

CTRL1	CTRL2	CTRL3	DESCRIPTION
Low	Low	Low	Normal operation; SNRBoost <sup>3G</sup> disabled for both channels
Low Low		High	SNRBoost <sup>3G</sup> enabled for channel B
Low	High	Low	SNRBoost <sup>3G</sup> enabled for channel A
Low	High	High	SNRBoost <sup>3G</sup> enabled for channels A and B
High	Low	Low	Global power-down
High	Low	High	Channel A standby
High	High	Low	Do not use
High	High	High	MUX mode of operation, channels A and B data are multiplexed and output on pins CHB_D[10:0].

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SNRBoost <sup>3G</sup> FILTER NUMBER	BANDWIDTH OF THE BATHTUB (MHz)	CENTER FREQUENCY OF THE BATHTUB (MHz)
0	25 × (f <sub>s</sub> /200)	15 × (f <sub>s</sub> /200)
1	$20 \times (f_{S}/200)$	$30 \times (f_S/200)$
2	$20 \times (f_{S}/200)$	35 × (f <sub>S</sub> /200)
3	20 × (f <sub>S</sub> /200)	$42 \times (f_{\rm S}/200)$
4	$20 \times (f_{\rm S}/200)$	$50 \times (f_S/200)$
5	$20 \times (f_{\rm S}/200)$	$58 \times (f_{\rm S}/200)$
6	20 × (f <sub>S</sub> /200)	$65 \times (f_{\rm S}/200)$
7	20 × (f <sub>S</sub> /200)	75 × (f <sub>S</sub> /200)
8	20 × (f <sub>S</sub> /200)	85 × (f <sub>S</sub> /200)
9	25 × (f <sub>S</sub> /200)	87.5 × (f <sub>S</sub> /200)
10	25 × (f <sub>S</sub> /200)	15 × (f <sub>S</sub> /200)
11	20 × (f <sub>S</sub> /200)	25 × (f <sub>S</sub> /200)
12	20 × (f <sub>S</sub> /200)	35 × (f <sub>S</sub> /200)
13	20 × (f <sub>S</sub> /200)	42 × (f <sub>S</sub> /200)
14	20 × (f <sub>S</sub> /200)	50 × (f <sub>S</sub> /200)
15	20 × (f <sub>S</sub> /200)	58 × (f <sub>S</sub> /200)
16	20 × (f <sub>S</sub> /200)	65 × (f <sub>S</sub> /200)
17	20 × (f <sub>S</sub> /200)	75 × (f <sub>S</sub> /200)
18	25 × (f <sub>S</sub> /200)	82.5 × (f <sub>S</sub> /200)
19	25 × (f <sub>S</sub> /200)	87.5 × (f <sub>S</sub> /200)
20	25 × (f <sub>S</sub> /200)	15 × (f <sub>S</sub> /200)
21	30 × (f <sub>S</sub> /200)	30 × (f <sub>S</sub> /200)
22	30 × (f <sub>S</sub> /200)	35 × (f <sub>S</sub> /200)
23	30 × (f <sub>S</sub> /200)	45 × (f <sub>S</sub> /200)
24	30 × (f <sub>S</sub> /200)	55 × (f <sub>S</sub> /200)
25	30 × (f <sub>S</sub> /200)	65 × (f <sub>S</sub> /200)
26	30 × (f <sub>S</sub> /200)	70 × (f <sub>S</sub> /200)
27	30 × (f <sub>S</sub> /200)	80 × (f <sub>S</sub> /200)
28	30 × (f <sub>S</sub> /200)	85 × (f <sub>S</sub> /200)
29	25 × (f <sub>S</sub> /200)	87.5 × (f <sub>S</sub> /200)
30	40 × (f <sub>S</sub> /184)	46 × (f <sub>S</sub> /184)
31	40 × (f <sub>S</sub> /184)	72 × (f <sub>S</sub> /184)
32	40 × (f <sub>S</sub> /184)	20 × (f <sub>S</sub> /184)
33	40 × (f <sub>S</sub> /184)	40 × (f <sub>S</sub> /184)
34	40 × (f <sub>S</sub> /184)	39.5 × (f <sub>S</sub> /184)
35	40 × (f <sub>S</sub> /184)	33.5 × (f <sub>S</sub> /184)
36	40 × (f <sub>S</sub> /184)	27 × (f <sub>S</sub> /184)
37	40 × (f <sub>S</sub> /184)	53 × (f <sub>S</sub> /184)
38	40 × (f <sub>S</sub> /184)	59 × (f <sub>S</sub> /184)
39	40 × (f <sub>S</sub> /184)	65.5 × (f <sub>S</sub> /184)

# Table 14. Complete List of SNRBoost<sup>3G</sup> Modes ( $f_s$ = Sampling Frequency in MSPS)

### SBAS509B-JUNE 2010-REVISED OCTOBER 2010

SNRBoost <sup>3G</sup> FILTER NUMBER	BANDWIDTH OF THE BATHTUB (MHz)	CENTER FREQUENCY OF THE BATHTUB (MHz)
40	60 × (f <sub>S</sub> /184)	46 × (f <sub>S</sub> /184)
41	60 × (f <sub>S</sub> /184)	46 × (f <sub>S</sub> /184)
42	60 × (f <sub>S</sub> /184)	30 × (f <sub>S</sub> /184)
43	60 × (f <sub>S</sub> /184)	30 × (f <sub>S</sub> /184)
44	60 × (f <sub>S</sub> /184)	62 × (f <sub>S</sub> /184)
45	60 × (f <sub>S</sub> /184)	62 × (f <sub>S</sub> /184)
46	60 × (f <sub>S</sub> /184)	40.5 × (f <sub>S</sub> /184)
47	60 × (f <sub>S</sub> /184)	40.5 × (f <sub>S</sub> /184)
48	60 × (f <sub>S</sub> /184)	37 × (f <sub>S</sub> /184)
49	60 × (f <sub>S</sub> /184)	37 × (f <sub>S</sub> /184)
50	60 × (f <sub>S</sub> /184)	53 × (f <sub>S</sub> /184)
51	60 × (f <sub>S</sub> /184)	50 × (f <sub>S</sub> /184)
52	60 × (f <sub>S</sub> /184)	54 × (f <sub>S</sub> /184)
53	58 × (f <sub>S</sub> /184)	58 × (f <sub>S</sub> /184)
54	60 × (f <sub>S</sub> /184)	62 × (f <sub>S</sub> /184)

# Table 14. Complete List of SNRBoost<sup>3G</sup> Modes (f<sub>s</sub> = Sampling Frequency in MSPS) (continued)

# GAIN FOR SFDR/SNR TRADE-OFF

The ADS58C28 includes gain settings that can be used to get improved SFDR performance. The gain is programmable from 0dB to 6dB (in 0.5dB steps) using the GAIN register bits. For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 15.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5dB and 1dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used as a trade-off between SFDR and SNR.

After a reset, the gain function is disabled. To use gain:

- First, program the DIGITAL MODE 1 and DIGITAL MODE 2 bits (see Table 12) to enable the gain function.
- This setting enables the gain and puts the device in a 0dB gain mode.
- · For other gain settings, program the GAIN register bits.

GAIN (dB)	ТҮРЕ	FULL-SCALE (V <sub>PP</sub> )
0	Default after reset	2
1	Fine adjust, programmable	1.78
2	Fine adjust, programmable	1.59
3	Fine adjust, programmable	1.42
4	Fine adjust, programmable	1.26
5	Fine adjust, programmable	1.12
6	Fine adjust, programmable	1

# Table 15. Full-Scale Range Across Gains



# OFFSET CORRECTION

The ADS58C28 has an internal offset correction algorithm that estimates and corrects dc offset up to ±10mV. The correction can be enabled using the ENABLE OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in Table 16.

OFFSET CORR TIME CONSTANT	TIME CONSTANT, TC <sub>CLK</sub> (Number of Clock Cycles)	TIME CONSTANT, TC <sub>CLK</sub> × 1/f <sub>S</sub> (sec) <sup>(1)</sup>
0000	1M	5ms
0001	2M	10ms
0010	4M	21ms
0011	8M	42ms
0100	16M	84ms
0101	32M	168ms
0110	64M	336ms
0111	128M	671ms
1000	256M	1.3s
1001	512M	2.7s
1010	1024M	5.4s
1011	2048M	10.7s
1100	Reserved	—
1101	Reserved	—
1110	Reserved	_
1111	Reserved	_

# Table 16. Time Constant of Offset Correction Algorithm

(1) Sampling frequency,  $f_S = 200MSPS$ .

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 1. Once frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by default after reset.

After a reset, the offset correction is disabled. To use offset correction:

- First, program the DIGITAL MODE 1 and DIGITAL MODE 2 bits (see Table 12) to enable the correction.
- Then set ENABLE OFFSET CORR to '1' and program the required time constant.

# DIGITAL OUTPUT INFORMATION

The ADS58C28 provides 11-bit digital data for each channel and a common output clock synchronized with the data.

# **Output Interface**

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. They can be selected using the LVDS CMOS serial interface register bit .

# **DDR LVDS Outputs**

In this mode, the data bits and clock are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair.





NOTE: X = channels A and B.





Figure 65. DDR LVDS Interface Timing Diagram



# LVDS Output Data and Clock Buffers

The equivalent circuit of each LVDS output buffer is shown in Figure 66. After reset, the buffer presents an output impedance of  $100\Omega$  to match with the external  $100\Omega$  termination.

The V<sub>DIFF</sub> voltage is nominally 350mV, resulting in an output swing of  $\pm$ 350mV with 100 $\Omega$  external termination. The V<sub>DIFF</sub> voltage is programmable using the LVDS SWING register bits from  $\pm$ 125mV to  $\pm$ 570mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support  $50\Omega$  differential termination. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a  $100\Omega$  termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.



Figure 66. LVDS Buffer Equivalent Circuit



Figure 67. LVDS Strength Doubling (Example Application)



### **Parallel CMOS Interface**

In the CMOS mode, each data bit is output on separate pins as CMOS voltage level, every clock cycle. The rising edge of the output clock CLKOUT can be used to latch data in the receiver.

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs and degrade the SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this effect, the CMOS output buffers are designed with controlled drive strength. The default drive strength ensures wide data stable window provided the data outputs have minimal load capacitance. It is recommended to use short traces (1 to 2 inches or 25,4mm to 50,8mm) terminated with not more than 5pF load capacitance.

For sampling frequencies greater than 150MSPS, it is recommended to use an external clock to capture data. The delay from input clock to output data and the data valid times are specified for the higher sampling frequencies. These timings can be used to delay the input clock appropriately and use it to capture the data.





Figure 68. CMOS Interface

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ADC output and receiver pins (1 to 2 inches).



# **CMOS** Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital current as a result of CMOS output switching =  $C_L \times DRVDD \times (N \times F_{AVG})$ ,

where  $C_L$  = load capacitance, N ×  $F_{AVG}$  = average number of output bits switching.



## **Multiplexed Mode of Operation**

In this mode, the digital outputs of both channels are multiplexed and output on a single bus (CHB\_D[10:0] pins), as shown in Figure 70. Any unused channel output pins (CHA\_Dn) are forced low and are not put in a high-impedance state. Because the output data rate on the channel B bus is effectively doubled, this mode is recommended only for low sampling frequencies (< 75MSPS). This mode can be enabled using the POWER-DOWN MODE register bits or using the CTRL[3:1] parallel pins. Note that setup and hold timings in this mode are different compared to the default CMOS mode.



(1) Dn = Bits D0, D1, D2, etc.

(2) In multiplexed mode, both channel outputs come on channel B output pins.



# **Output Data Format**

Two output data formats are supported: twos complement and offset binary. They can be selected using the DATA FORMAT CHx serial interface register bit.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 7FFh in offset binary output format, and 3FFh in twos complement output format. For a negative input overdrive, the output code is 0000h in offset binary output format and 400h in twos complement output format.

# **BOARD DESIGN CONSIDERATIONS**

# Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the *EVM User Guide* for details on layout and grounding.

# Exposed Pad

In addition to providing a path for heat dissipation, the PowerPAD is also electrically internally connected to the digital ground. Therefore, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes.

# **DEFINITION OF SPECIFICATIONS**

**Analog Bandwidth** – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

**Aperture Delay** – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

**Clock Pulse Width/Duty Cycle** – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

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**Maximum Conversion Rate** – The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

**Differential Nonlinearity (DNL)** – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

**Integral Nonlinearity (INL)** – The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

**Gain Error** – Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as  $E_{GREF}$  and  $E_{GCHAN}$ .

To a first-order approximation, the total gain error is  $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$ .

For example, if  $E_{TOTAL} = \pm 0.5\%$ , the full-scale input varies from  $(1 - 0.5/100) \times FS_{ideal}$  to  $(1 + 0.5/100) \times FS_{ideal}$ .

**Offset Error** – The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

**Temperature Drift** – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from  $T_{MIN}$  to  $T_{MAX}$ . It is calculated by dividing the maximum deviation of the parameter across the  $T_{MIN}$  to  $T_{MAX}$  range by the difference  $T_{MAX} - T_{MIN}$ .

**Signal-to-Noise Ratio** – SNR is the ratio of the power of the fundamental ( $P_S$ ) to the noise floor power ( $P_N$ ), excluding the power at dc and the first nine harmonics.

SNR = 
$$10 \text{Log}^{10} \frac{\text{P}_{\text{S}}}{\text{P}_{\text{N}}}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

**Signal-to-Noise and Distortion (SINAD)** – SINAD is the ratio of the power of the fundamental ( $P_S$ ) to the power of all the other spectral components including noise ( $P_N$ ) and distortion ( $P_D$ ), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D}$$
(2)

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

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(1)



**Effective Number of Bits (ENOB)** – ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\mathsf{ENOB} = \frac{\mathsf{SINAD} - 1.76}{6.02}$$

**Total Harmonic Distortion (THD)** – THD is the ratio of the power of the fundamental ( $P_S$ ) to the power of the first nine harmonics ( $P_D$ ).

THD = 
$$10 \text{Log}^{10} \frac{\text{P}_{\text{S}}}{\text{P}_{\text{N}}}$$

THD is typically given in units of dBc (dB to carrier).

**Spurious-Free Dynamic Range (SFDR)** – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

**Two-Tone Intermodulation Distortion** – IMD3 is the ratio of the power of the fundamental (at frequencies  $f_1$  and  $f_2$ ) to the power of the worst spectral component at either frequency  $2f_1 - f_2$  or  $2f_2 - f_1$ . IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

**DC Power-Supply Rejection Ratio (DC PSRR)** – DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

**AC Power-Supply Rejection Ratio (AC PSRR)** – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If  $\Delta V_{SUP}$  is the change in supply voltage and  $\Delta V_{OUT}$  is the resultant change of the ADC output code (referred to the input), then:

PSRR = 20Log<sup>10</sup> 
$$\frac{\Delta V_{OUT}}{\Delta V_{SUP}}$$
 (Expressed in dBc)

**Voltage Overload Recovery** – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6 dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

**Common-Mode Rejection Ratio (CMRR)** – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If  $\Delta V_{CM_{IN}}$  is the change in the common-mode voltage of the input pins and  $\Delta V_{OUT}$  is the resulting change of the ADC output code (referred to the input), then:

CMRR = 20Log<sup>10</sup> 
$$\frac{\Delta V_{OUT}}{\Delta V_{CM}}$$
 (Expressed in dBc)

**Crosstalk (only for multi-channel ADCs)** – This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

(3)

(4)

(5)

(6)



# **REVISION HISTORY**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Cł	hanges from Revision A (October 2010) to Revision B	Page
•	Updated Figure 44	40



# **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
ADS58C28IRGC25	ACTIVE	VQFN	RGC	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS58C28IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS58C28IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# PACKAGE MATERIALS INFORMATION

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# TAPE AND REEL INFORMATION

# REEL DIMENSIONS

TEXAS INSTRUMENTS





TAPE AND REEL INFORMATION

### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal												
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS58C28IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS58C28IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

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# PACKAGE MATERIALS INFORMATION

16-Feb-2012



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS58C28IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
ADS58C28IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6

# **MECHANICAL DATA**



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.

- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.





NOTE: A. All linear dimensions are in millimeters



RGC (S-PVQFN-N64)

# PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.



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