CRD5378

Single-Channel Seismic Reference Design

Features

- Single-channel Seismic Acquisition Node
  - – CS3302A hydrophone amplifier
  - – CS5373A ΔΣ modulator + test DAC
  - – CS5378 digital filter + PLL
  - – Precision voltage reference
- On-board Microcontroller
  - – SPI™ interface to digital filter
  - – USB communication with PC
- Board Design
  - – Compact board size: 5” x 1.25” x 0.5”
  - – Detachable acquisition and telemetry nodes
- PC Evaluation Software
  - – Register setup & control
  - – FFT frequency analysis
  - – Time domain analysis
  - – Noise histogram analysis

General Description

The CRD5378 board is a compact reference design for the Cirrus Logic single-channel seismic chip set. Data sheets for the CS3302A, CS5373A, and CS5378 devices should be consulted when using the CRD5378 reference design.

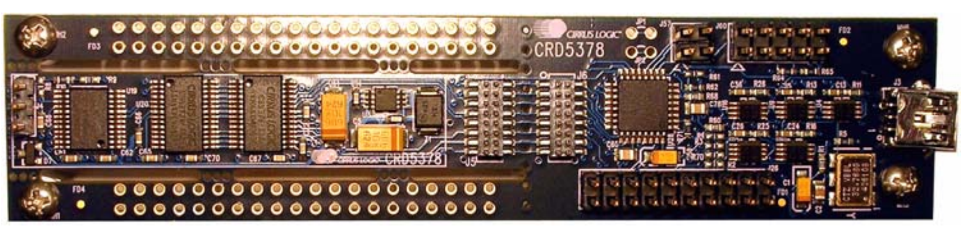
Pin headers connect an external differential sensor to the analog inputs of the measurement channel. An on-board test DAC creates precision differential analog signals for in-circuit performance testing without an external signal source.

The reference design includes an 8051-type microcontroller with hardware SPI™ and USB serial interfaces. The microcontroller communicates with the digital filter via SPI and with the PC evaluation software via USB. The PC evaluation software controls register and coefficient initialization and performs time domain, histogram, and FFT frequency analysis on captured data.

The CRD5378 board features a special breakout connector used to detach the acquisition and telemetry sections for remote sensor applications.

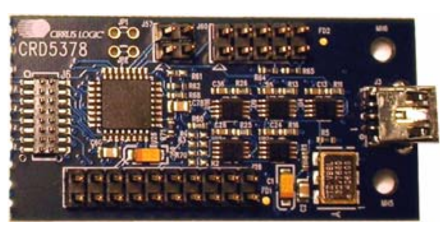
ORDERING INFORMATION

CRD5378 Reference Design



Reference Design Panel (Actual Size)

Data Aquisition Board (Actual Size)



Control Board (Actual Size)

REVISION HISTORY

Revision	Date	Changes
RD1	JAN 2007	Initial release.
RD2	JAN 2008	Upgrade from CS3302 to CS3302A-ISZ/G (U19). Change (R27,R28,R29,R30) from 0ohms to 680ohms.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com

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1. INITIAL SETUP

1.1 Kit Contents

The CRD5378 reference design kit includes:

- CRD5378 reference design board
- USB cable (A to mini-B)
- Software download information card

The following are required to operate CRD5378, and are not included:

- Bipolar power supply with clip lead outputs (+/- 3.3 V @ 100 mA)
- PC running Windows 2000™ or Windows XP® with an available USB port
- Internet access to download the evaluation software

1.2 Hardware Setup

To set up the CRD5378 reference design hardware:

- Verify all jumpers are in the default settings (see next section).
- With power off, connect the CRD5378 power inputs to the power supply outputs.

  J26 pin 17 = -3.3 V

  J26 pin 19 = +3.3 V

  J26 pin 20 = 0 V
- Connect the USB cable between the CRD5378 USB connector and the PC USB port.
- Proceed to the Software Setup section to install the evaluation software and USB driver.

1.2.1 Default Jumper Settings

* indicates the default 0 Ω jumper installations for CRD5378.

Amplifier		CS3301A	CS3302A
CH1	U19	R8 + R9	*R10

Table 1. Amplifier Pin 13 Jumper Setting

Input Clock	Resistor
EXTERNAL CLOCK	R2
1.024 MHz	R70
2.048 MHz	R4
4.096 MHz	R3
32.768 MHz	*R60

Table 2. System Clock Input Setting

Digital Filter Clock	Resistor
4.096 MHz Manchester	R15 + R41 + R42
2.048 MHz Manchester	R42
1.024 MHz Manchester	R41
32.768 MHz	R41+R42
4.096 MHz	R15
2.048 MHz	R15+R42
1.024 MHz	R15+R41
32.768 MHz	*Not Populated

Table 3. CS5378 PLL Mode Select Setting (R15, R41, R42)

Sync Source	Jumper
RS-485	*R47 + *R48
Direct Output	R49 + R50 + R45

Table 4. Input SYNC Source Selection Setting

Sync Source	Jumper
SYNC	*R71 (Not Populated)
SYNC_IO	R71

Table 5. CS5378 SYNC Source Selection Setting

1.3 Software Setup

1.3.1 PC Requirements

The PC hardware requirements for the Cirrus Seismic Evaluation system are:

- *Windows XP®, Windows 2000™, Windows NT®*
- *Intel Pentium 600 MHz or higher microprocessor*
- *VGA resolution or higher video card*
- *Minimum 64MB RAM*
- *Minimum 40MB free hard drive space*

1.3.2 Seismic Evaluation Software Installation

Important: For reliable USB communication, the USBXpress® driver must be installed after the Seismic Evaluation Software installation but ***before*** launching the application. The USBXpress driver files are included in a sub-folder as part of the installation.

To install the Cirrus Logic Seismic Evaluation Software:

- Go to the Cirrus Logic Industrial Software web page (http://www.cirrus.com/industrialsoftware). Click the link for *"Cirrus Seismic Evaluation GUI"* to get to the download page and then click the link for *"Cirrus Seismic Evaluation GUI Release Vxx"* (*xx* indicates the version number).
- Read the software license terms and click *"Accept"* to download the *"SeismicEvalGUI_vxx.zip"* file to any directory on the PC.
- Unzip the downloaded file to any directory and a *"Distribution\Volume1"* sub-folder containing the installation application will automatically be created.
- Open the *"Volume1"* sub-folder and run *"setup.exe"*. If the Seismic Evaluation Software has been previously installed, the uninstall wizard will automatically remove the previous version during install.
- Follow the instructions presented by the Cirrus Seismic Evaluation Installation Wizard. The default installation location is *"C:\Program Files\Cirrus Seismic Evaluation"*.

An application note, AN271 - *Cirrus Seismic Evaluation GUI Installation Guide*, is available from the Cirrus Logic web site with step-by-step instructions on installing the Seismic Evaluation Software.

1.3.3 USBXpress® Driver Installation

Important: For reliable USB communication, the USBXpress® driver must be installed after the Seismic Evaluation Software installation but ***before*** launching the application. The USBXpress driver files are included in a sub-folder as part of the installation.

The Cirrus Logic Seismic Evaluation Software communicates with CRD5378 via USB using the USBXpress driver from Silicon Laboratories (http://www.silabs.com). For convenience, the USBXpress driver files are included as part of the installation package.

To install the USBXpress driver (after installing the Seismic Evaluation Software):

- Connect CRD5378 to the PC through an available USB port and apply power. The PC will detect CRD5378 as an unknown USB device.

- If prompted for a USB driver, skip to the next step. If not, using Windows Hardware Device Manager go to the properties of the unknown USB API device and select *"Update Driver"*.
- Select *"Install from a list or specific location"*, then select *"Include this location in the search"* and then browse to *"C:\Program Files\Cirrus Seismic Evaluation\Driver\"*. The PC will recognize and install the USBXpress device driver.
- After driver installation, cycle power to CRD5378. The PC will automatically detect it and add it as a USBXpress device in the Windows Hardware Device Manager.

An application note, AN271 - *Cirrus Seismic Evaluation GUI Installation Guide*, is available from the Cirrus Logic web site with step-by-step instructions on installing the USBXpress driver.

1.3.4 Launching the Seismic Evaluation Software

Important: For reliable USB communication, the USBXpress driver must be installed after the Seismic Evaluation Software installation but ***before*** launching the application. The USBXpress driver files are included in a sub-folder as part of the installation.

To launch the Cirrus Seismic Evaluation Software, go to:

- *Start ⇨ Programs ⇨ Cirrus Seismic Evaluation ⇨ Cirrus Seismic Evaluation*

or:

- *C:\Program Files\Cirrus Seismic Evaluation\SeismicGUI.exe*

For the most up-to-date information about the software, please refer to it's help file:

- Within the software: *Help ⇨ Contents*

or:

- *C:\Program Files\Cirrus Seismic Evaluation\SEISMICGUI.HLP*

1.4 Self-Testing CRD5378

Noise and distortion self-tests can be performed once hardware and software setup is complete.

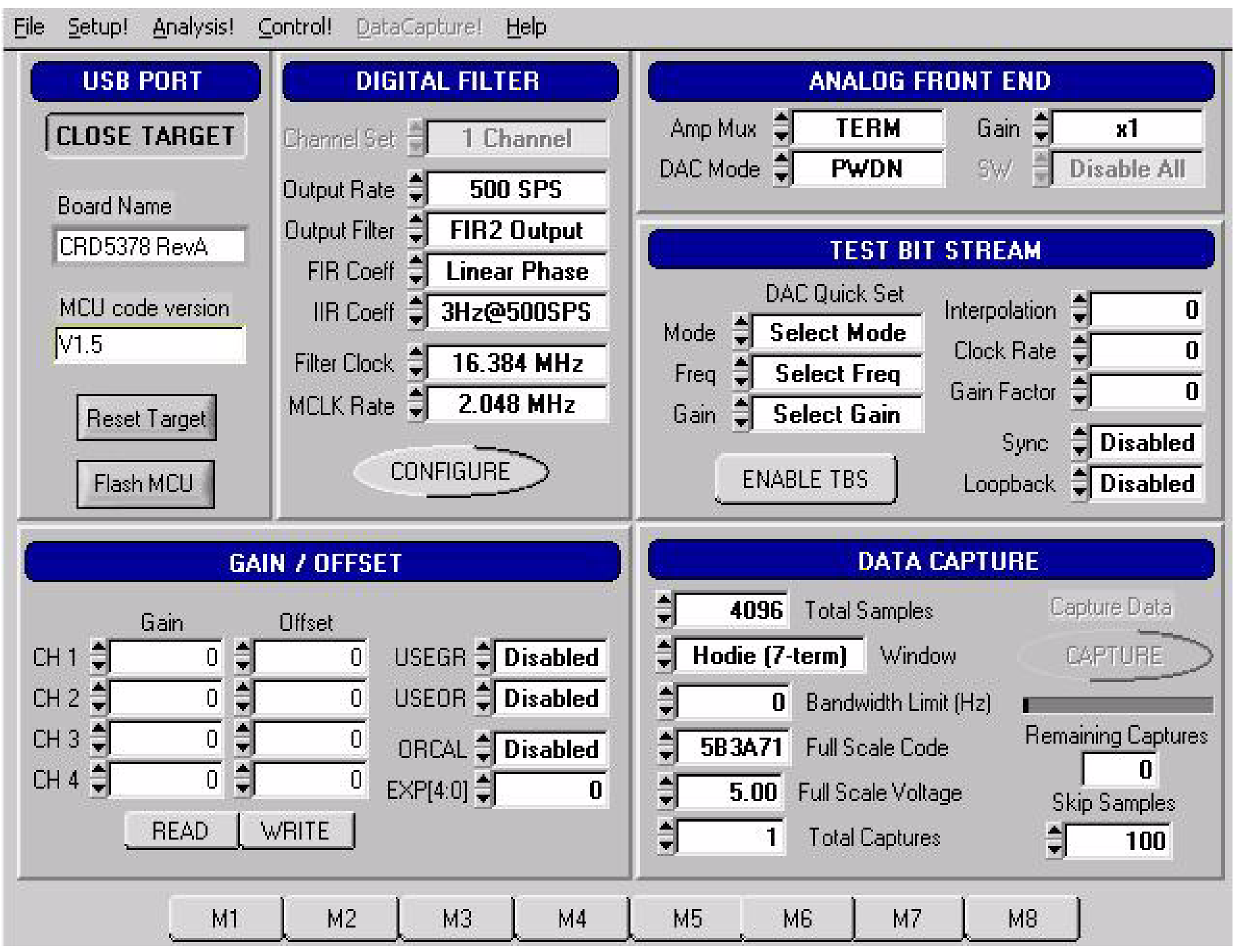
First, initialize the CRD5378 reference design:

- Launch the evaluation software and apply power to CRD5378.
- Click ‘OK’ on the **About** panel to get to the **Setup** panel.
- On the **Setup** panel, select *Open Target* on the **USB Port** sub-panel.
- When connected, the *Board Name* and *MCU code version* will be displayed.

1.4.1 Noise Test

Noise performance of the measurement channel can be tested as follows:

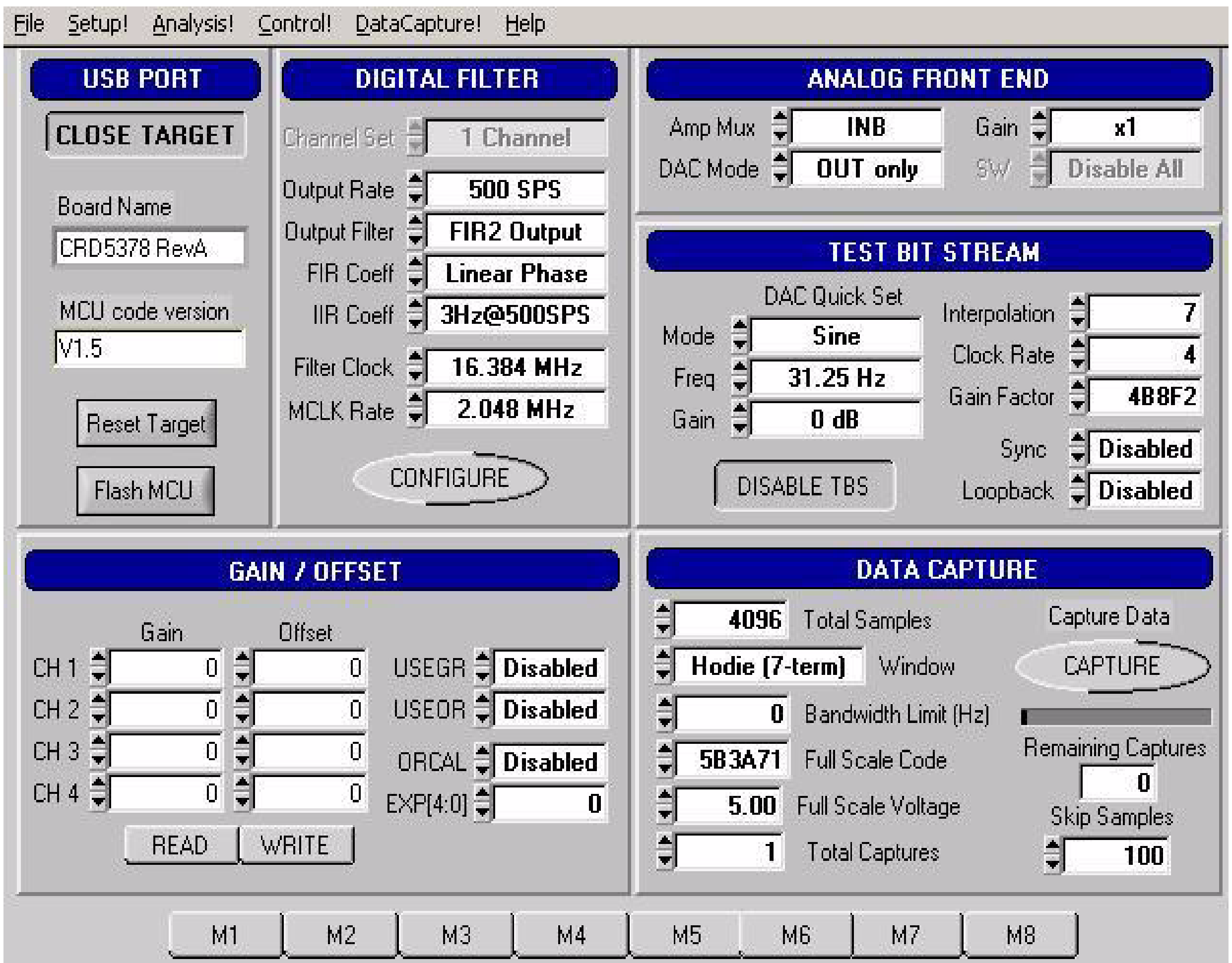
- Set the controls on the **Setup** panel to match the picture:



- Once the **Setup** panel is set, select *Configure* on the **Digital Filter** sub-panel.
- After digital filter configuration is complete, click *Capture* on the **Data Capture** sub-panel.
- Once the data record is collected, the **Analysis** panel is automatically displayed.
- Select *Noise FFT* from the *Test Select* control to display the calculated noise statistics.
- Verify the noise performance (S/N) is 124 dB or better.

1.4.2 Distortion Test

- Set the controls on the **Setup** panel to match the picture:



- Once the **Setup** panel is set, select *Configure* on the **Digital Filter** sub-panel.
- After digital filter configuration is complete, click *Capture* on the **Data Capture** sub-panel.
- Once the data record is collected, the **Analysis** panel is automatically displayed.
- Select *Signal FFT* from the *Test Select* control to display the calculated noise statistics.
- Verify the distortion performance (S/D) is 109 dB or better.

2. HARDWARE DESCRIPTION

2.1 Block Diagram

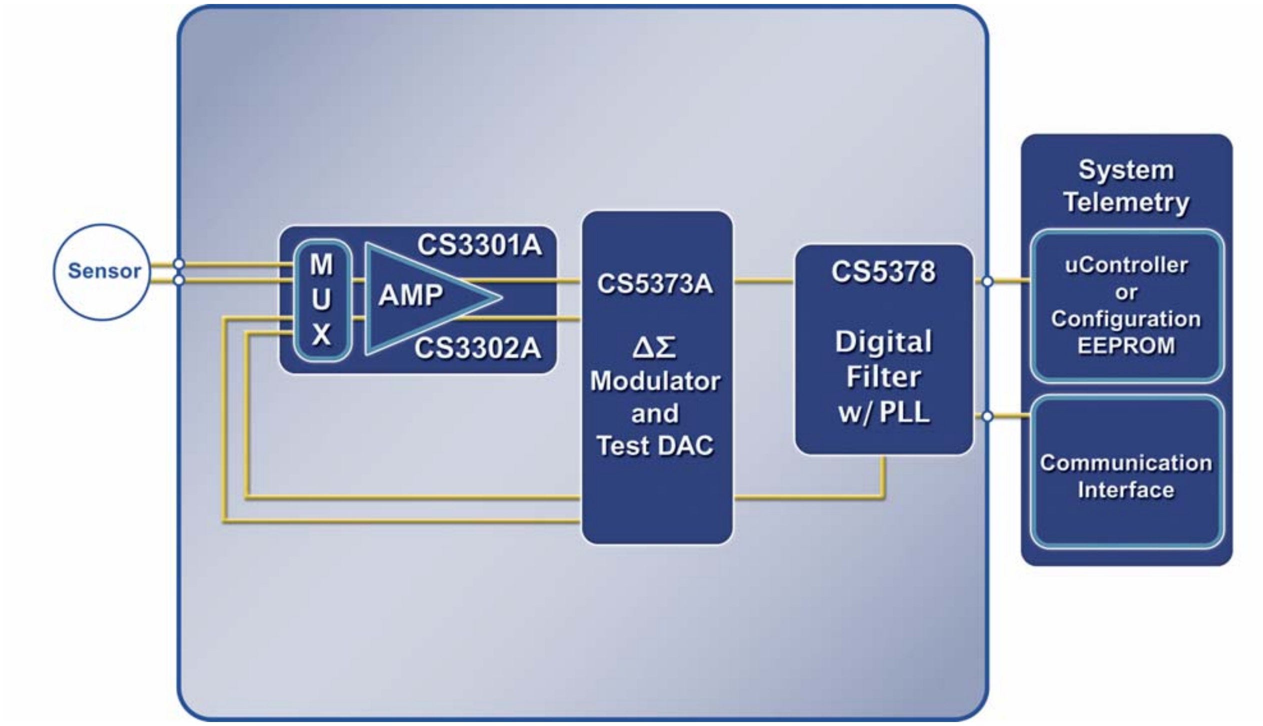


Figure 1. CRD5378 Block Diagram

Major blocks of the CRD5378 reference design include:

- **CS3302A Hydrophone Amplifier**
- **CS5373A ΔΣ Modulator + Test DAC**
- **CS5378 Digital Filter + PLL**
- **Precision Voltage Reference**
- **Microcontroller with USB**
- **RS-485 Transceivers**
- **Voltage Regulators**

2.2 Analog Hardware

2.2.1 Analog Inputs

2.2.1.1 External Inputs - INA

External signals into CRD5378 are from two major classes of sensors, moving coil geophones and piezo-electric hydrophones. Geophones are low-impedance sensors optimized to measure vibrations in land applications. Hydrophones are high-impedance sensors optimized to measure pressure in marine applications. Other sensors for earthquake monitoring and military applications are considered as geophones for this data sheet.

External signals connect to CRD5378 through a 3-pin header on the left side of the PCB. This header makes a connection to the differential INA amplifier inputs and to either a GND or GUARD signal for connection to the sensor cable shields, if present.

Signal Input	Pin Header
CH1 INA	J4

Table 6. Pin Header Input Connections

2.2.1.2 GUARD Output, GND Connection

The CS3302A hydrophone amplifier provides a GUARD signal output on pin 13 designed to actively drive the cable shield of a high impedance sensor with the common mode voltage of the sensor differential signal. This GUARD output on the cable shield minimizes leakage by minimizing the voltage differential between the sensor signal and the cable shield. The CS3301A geophone amplifier does not have a GUARD output. Instead, the CS3301A amplifier expects an MCLK clock input to pin 13, which is needed for its chopper stabilization circuitry. When using a CS3301A amplifier, a cable shield termination to GND is provided for the sensor connection.

By default, CRD5378 uses the CS3302A amplifier. Therefore, the GUARD signal is connected to pin 3 of the input signal header, J4.

To configure CRD5378 with the CS3301A geophone amplifier, simply make the following three changes:

1) De-solder the 0 Ω resistor at R10 to remove the GUARD signal from pin 3 of J4.
2) Populate R8 with a 0 Ω resistor to provide a cable shield termination to GND.
3) Populate R9 with a 0 Ω resistor so that the CS3301A amplifier can receive its required master clock (MCLK) from the CS5378 digital filter.

2.2.1.3 Internal Inputs - DAC_OUT, DAC_BUF

The CS5373A test DAC has two high performance differential test outputs, a precision output (DAC_OUT) and a buffered output (DAC_BUF). The DAC_OUT signal is wired directly to the INB inputs of the CS3302A amplifier for testing the performance of the electronics channel. The DAC_BUF signal is wired to the INA inputs of the amplifier and is used to test the performance of the measurement channel with a sensor attached.

2.2.1.4 Input Protection

Sensor inputs must have circuitry to protect the analog electronics from voltage spikes. Geophone coils are susceptible to magnetic fields (especially from lightning) and hydrophones can produce large voltage spikes if located near an air gun source.

Discrete switching diodes quickly clamp the analog inputs to the power supply rails when the input voltage spikes. These diodes are reverse biased in normal operation and have low reverse bias leakage and capacitance characteristics to maintain high linearity on the analog inputs.

Specification	Value
Dual Series Switching Diode - ON Semiconductor	BAV99LT1
Surface Mount Package Type	SOT-23
Non-Repetitive Peak Forward Current (1 µs, 1 ms, 1 s)	2.0 A, 1.0 A, 500 mA
Reverse Bias Leakage (25 C to 85 C)	0.004 µA - 0.4 µA
Reverse Bias Capacitance (0 V to 5 V)	1.5 pF - 0.54 pF

2.2.1.5 Input RC Filters

Following the diode clamps is an RC filter network that bandwidth limits the sensor inputs into the amplifiers to 'chop-the-tops-off' residual voltage spikes not clamped by the discrete diodes. In addition, all Cirrus Logic component ICs have built in ESD protection diodes guaranteed to 2000 V HBM / 200 V MM (JEDEC standard). The small physical size of these ESD diodes restricts their current capacity to 10 mA.

For land applications that use the CS3301A amplifier, the INA input has a common mode and differential RC filter. The common mode filter sets a low-pass corner to shunt very high frequency components to ground with minimal noise contribution. The differential filter sets a low-pass corner high enough not to affect the magnitude response of the measurement bandwidth.

For marine applications that use the CS3302A amplifier, the inherent capacitance of the piezoelectric sensor is combined with large resistors to create an analog high-pass RC filter to eliminate the low-frequency components of ocean noise.

Land Common Mode Filter Specification	Value
Common Mode Capacitance	10 nF ± 10%
Common Mode Resistance	200 Ω
Common Mode -3 dB Corner @ 6 dB/octave	80 kHz ± 10%

Land Differential Filter Specification	Value
Differential Capacitance	10 nF ± 10%
Differential Resistance	200 Ω + 200 Ω = 400 Ω
Differential -3 dB Corner @ 6 dB/octave	40 kHz ± 10%

Marine Common Mode Filter Specification	Value
Hydrophone Group Capacitance	128 nF ± 10%
Differential Resistance	412 kΩ + 2 kΩ
-3 dB Corner @ 6 dB/octave	3 Hz ± 10%

2.2.1.6 Common Mode Bias

Differential analog signals into the CS3301A/02A amplifiers are required to be biased to the center of the power supply voltage range, which for bipolar supplies is near ground potential. Resistors to create the common mode bias are selected based on the sensor impedance and may need to be modified from the CRD5378 defaults depending on the sensor to be used. Refer to the recommended operating bias conditions for the selected sensor, which are available from the sensor manufacturer.

Specification	Value
Geophone Sensor Bias Resistance	20 kΩ || 20 kΩ = 10 kΩ
Hydrophone Sensor Bias Resistance	18 MΩ || 18 MΩ = 9 MΩ

2.2.2 Differential Amplifiers

The CS3301A/02A amplifiers act as a low-noise gain stage for internal or external differential analog signals.

Analog Signals	Description
INA	Sensor analog input
INB	Test DAC analog input
OUTR, OUTF	Analog rough / fine outputs
GUARD	CS3302A guard output (R10 = 0 Ω, R9 = NO POP)

Digital Signals	Description
MUX[0..1]	Input mux selection
GAIN[0..2]	Gain range selection
PWDN	Power down mode enable
CLK	CS3301A clock input (R10 = NO POP, R9 = 0 Ω)

2.2.2.1 MCLK Input vs. GUARD Output

By default, CRD5378 uses the CS3302A hydrophone amplifier. The CS3302A amplifier is a very high input impedance device and achieves a 1/f noise performance typically buried below the low-frequency ocean noise. To minimize leakage from high impedance sensors connected to the CS3302A amplifier, pin 13 produces a GUARD signal output to actively drive a sensor cable shield with the common mode voltage of the sensor signal.

Comparing the CS3301A and CS3302A amplifiers, the functionality of pin 13 (MCLK input vs. GUARD output) is the only external difference. The CS3301A amplifier is chopper-stabilized requiring a clock source on input pin 13. In order to run the chopper circuitry synchronous to the modulator analog sampling clock, the CS3301A amplifier pin 13 connects to the CS5378 digital filter (MCLK).

CRD5378 can be converted to use either the CS3301A and CS3302A amplifiers by installing the amplifier device and populating R8, R9, and R10 with 0 Ω resistors accordingly.

Amplifier	CS3301A	CS3302A
U19	R8 + R9	*R10

Table 7. Amplifier Pin 13 Resistor Settings

Replacement amplifiers can be requested as samples from the local Cirrus Logic sales representative.

2.2.2.2 Rough-Fine Outputs - OUTR, OUTF

The analog outputs of the CS3301A/02A differential amplifiers are split into rough charge and fine charge signals for input to the CS5373A ΔΣ modulator.

Analog signal traces out of the CS3301A/02A amplifiers and into the CS5373A modulator are 4-wire INR+, INF+, INF-, INR- quad groups, and are routed with INF+ and INF- as a traditional differential pair and INR+ and INR- as guard traces outside the respective INF+ and INF- traces.

2.2.2.3 Anti-alias RC Filters

The CS5373A ΔΣ modulator is 4th order and high frequency input signals can cause instability. Simple single-pole anti-alias RC filters are required between the CS3301A/02A amplifier outputs and the CS5373A modulator inputs to bandwidth limit analog signals into the modulator.

For the CRD5378, the CS3301A/02A amplifier outputs are connected to external 680 Ω series resistors and a differential anti-alias RC filter is created by connecting 20 nF of high linearity differential capacitance (2x 10 nF C0G) between each half of the rough and fine signals.

2.2.3 Delta-Sigma Modulator

The CS5373A ΔΣ modulator performs the A/D function for differential analog signals from the CS3301A/02A amplifier. The digital output from the modulator is an oversampled ΔΣ bit stream.

Analog Signals	Description
INR, INF	Modulator analog rough / fine inputs
VREF	Voltage reference analog inputs

Digital Signals	Description
MDATA	Modulator delta-sigma data output
MFLAG	Modulator over-range flag output
MCLK	Modulator clock input
MSYNC	Modulator synchronization input

2.2.3.1 Rough-Fine Inputs - INR, INF

The modulator analog inputs are separated into rough and fine signals, each of which has an anti-alias RC filter to limit the signal bandwidth into the modulator inputs.

2.2.4 Delta-Sigma Test DAC

The CS5373A test DAC creates differential analog signals for system tests. Multiple test modes are available and their use is described in the CS5373A data sheet.

Analog Signals	Description
OUT	Precision differential analog output
BUF	Buffered differential analog output
CAP	Capacitor connection for internal anti-alias filter
VREF	Voltage reference analog inputs

Digital Signals	Description
TDATA	Delta-sigma test data input
MCLK	Clock input
SYNC	Synchronization input
MODE[0..2]	Test mode selection
ATT[0..2]	Attenuation range selection

2.2.4.1 Precision Output - DAC_OUT

The CS5373A test DAC has a precision output (DAC_OUT) that is routed directly to the amplifier INB inputs. The input impedance of the CS3301A/02A INB amplifier inputs are high enough that the precision output can be directly connected to the INB inputs.

2.2.4.2 Buffered Output - DAC_BUF

The CS5373A test DAC has a buffered output (DAC_BUF) that is routed to the amplifier INA inputs. This output is less sensitive to loading than the precision outputs, and can drive a sensor attached to the amplifier INA inputs provided the sensor meets the impedance requirements specified in the CS5373A data sheet.

2.2.5 Voltage Reference

A voltage reference on CRD5378 creates a precision voltage from the regulated analog supplies for the modulator and test DAC VREF inputs. Because the voltage reference output is generated relative to the negative analog power supply, VREF+ is near GND potential for bipolar power supplies.

Specification	Value
Precision Reference - Linear Tech	LT1019AIS8-2.5
Surface Mount Package Type	SO-8
Output Voltage Tolerance	+/- 0.05%
Temperature Drift	10 ppm / degC
Quiescent Current	0.65 mA
Output Voltage Noise, 10 Hz - 1 kHz	4 ppm_{RMS}
Ripple Rejection, 10 Hz - 200 Hz	> 100 dB

2.2.5.1 VREF_MOD

The voltage reference output is provided to the CS5373A ΔΣ modulator and test DAC through a low-pass RC filter. By filtering the voltage reference to the device, high-frequency noise is eliminated and any signal-dependent sampling of VREF is isolated. The voltage reference signal is routed as a separate differential pair from the large RC filter capacitor to control the sensitive VREF source-return currents and keep them out of the ground plane. In addition to the RC filter function, the 68 uF filter capacitor provides a large charge-well to help settle voltage reference sampling transients.

2.3 Digital Hardware

2.3.1 Digital Filter

The CS5378 digital filter performs filtering and decimation of the ΔΣ bit stream from the CS5373A modulator. It also creates a ΔΣ bit stream output to create analog test signals in the CS5373A test DAC.

The CS5378 requires several control signal inputs from the external system.

Control Signals	Description
RESETz	Reset input, active low
BOOT	Microcontroller / EEPROM boot mode select
TIMEB	Time Break input, rising edge triggered
CLK	Master clock input, 32.768 MHz
SYNC	Master synchronization input, rising edge triggered

Configuration and data collection are through the SPI port.

SPI1 Signals	Description
DRDYz	Data ready output, active low
SCK	Serial clock
MISO	Master in / slave out serial data
MOSI	Master out /slave in serial data
SS: EECSz	Serial chip select, active low

Modulator ΔΣ data is input through the modulator interface, and test DAC ΔΣ data is generated by the test bit stream generator.

Modulator Signals	Description
MCLK	Modulator clock output
MSYNC	Modulator synchronization output
MDATA	Modulator delta-sigma data input
MFLAG	Modulator over-range flag input
TBSDATA	Test DAC delta-sigma data output

Amplifier, modulator and test DAC pin settings are controlled through the GPIO port.

GPIO Signals	Description
GPIO[0]:MUX[0]	Amplifier input mux selection
GPIO[1..3]:MODE[0..2]	Test DAC mode selection
GPIO[4..6]:GAIN[0..2]	Amplifier gain / test DAC attenuation
GPIO[7]:MUX[1]	Amplifier input mux selection

2.3.1.1 Reset Options - BOOT, PLL

Immediately following the reset signal rising edge, the CS5378 digital filter latches the states of the GPIO[4..6]:PLL[0..2] and GPIO7:BOOT pins. The reset states of the GPIO[4..6]:PLL[0..2] pins select the master clock input frequency and type, while the reset state of the GPIO7:BOOT pin selects how the CS5378 digital filter receives configuration data.

At reset, the CS5378 digital filter GPIO pins default as inputs with weak pull-up resistors enabled. Therefore, if left floating, the GPIO state will read high upon reset.

The CRD5378 provides the option to connect the GPIO[4..6]:PLL[0..2] and GPIO7:BOOT pins to 10k Ω pull-down resistors (R15, R41, and R42) so they will read low at reset. Because the pin states are latched only during reset, GPIO pins can be programmed and used normally after reset without affecting the PLL and BOOT selections.

Detailed information about the PLL input clock and BOOT mode selections at reset can be found in the CS5378 data sheet.

2.3.1.2 Configuration - SPI Port

On CRD5378, configuration of the digital filter is through the SPI port by the on-board 8051 microcontroller, which receives commands from the PC evaluation software via the USB interface. Evaluation software commands can write/read digital filter registers, specify digital filter coefficients and start/stop digital filter operation.

By default the BOOT signal is set low to indicate configuration information is written by the microcontroller.

2.3.1.3 Phase Locked Loop

To make synchronous analog measurements throughout a distributed system, a synchronous system clock needs to be provided to each measurement node. For evaluation testing purposes, the CRD5378 can receive an external system clock by access through J1 and by non-population of R2, R3, R4, R60, and R70. With this external clock, a synchronous local clock can be created using the CS5378 PLL. The

CS5378 PLL input frequency is specified at reset by the state of the GPIO[4..6]:PLL[0..2] pins, as detailed in the CS5378 data sheet.

Specification	Value
Input Clock Frequency	1.024, 2.048, 4.096 MHz
Distributed Clock Synchronization	± 240 ns
Maximum Input Clock Jitter, RMS	1 ns

Specification	Value
PLL Internal Clock Frequency	32.768 MHz
Maximum Jitter, RMS	300 ps
Loop Filter Architecture	Internal

If no external system clock is supplied to CRD5378, the CRD5378 can select a PLL input clock from a local oscillator. Using a clock divider, the on-board oscillator produces 1.024 MHz, 2.048 MHz, 4.096 MHz and 32.768 MHz clock outputs that can be applied to the CS5378 CLK input.

.

Specification	Value
Oscillator - Citizen 32.768 MHz VCXO	CSX750VBEL32.768MTR
Surface Mount Package Type	Leadless 6-Pin, 5x7 mm
Supply Voltage, Current	3.3 V, 11 mA
Frequency Stability, Pullability	± 50 ppm, ± 90 ppm
Startup Time	4 ms

Specification	Value
Clock Divider - TI LittleLogic D-Flop	SN74LVC2G74DCTR
Surface Mount Package Type	SSOP8-199
Supply Voltage, Current	3.3 V, 10 µA

2.3.2 Microcontroller

Included on CRD5378 is an 8051-type microcontroller with integrated hardware SPI and USB interfaces. This C8051F320 microcontroller is a product of Silicon Laboratories (http://www.silabs.com). Key features of the C8051F320 microcontroller are:

- **8051 compatibility** - uses industry standard 8051 software development tools
- **In-circuit debugger** - software development on the target hardware
- **Internal memory** - 16k flash ROM and 2k static RAM included on-chip
- **Multiple serial connections** - SPI, USB, I^2C, and UART
- **High performance** - 25 MIPS maximum
- **Low power** - 0.6 mA @ 1 MHz w/o USB, 9 mA @ 12 MHz with USB
- **Small size** - 32 pin LQFP package, 9mm x 9mm
- **Industrial temperature** - full performance (including USB) from -40 C to +85 C
- **Internal temperature sensor** - with range violation interrupt capability
- **Internal timers** - four general purpose plus one extended capability
- **Power on reset** - can supply a reset signal to external devices
- **Analog ADC** - 10 bit, 200 ksps SAR with internal voltage reference
- **Analog comparators** - arbitrary high/low voltage compare with interrupt capability

The exact use of the microcontroller features is controlled by embedded firmware.

C8051F320 has dedicated pins for power and the USB connection, plus 25 general purpose I/O pins that connect to the various internal resources through a programmable crossbar. Hardware connections on CRD5378 limit how the blocks can operate, so the port mapping of microcontroller resources is detailed below.

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Pin #	Pin Name	Assignment	Description
1	P0.1	SYNC	SYNC signal output
2	P0.0	SYNC_IO	SYNC signal input from RS-485
3	GND		Ground
4	D+		USB differential data transceiver
5	D-		USB differential data transceiver
6	VDD		+3.3 V power supply input
7	REGIN		+5 V power supply input
8	VBUS		USB voltage sense input

Pin #	Pin Name	Assignment	Description
9	/RST C2CK	RESETz	Power on reset output, active low Clock input for debug interface
10	P3.0 C2D	GPIO	General purpose I/O Data in/out for debug interface
11	P2.7	AIN-	ADC input
12	P2.6	AIN+	ADC input
13	P2.5	GPIO	General Purpose I/O (unused in CRD5378)
14	P2.4	MODE2	CS5373A mode control
15	P2.3	MODE1	CS5373A mode control
16	P2.2	MODE0	CS5373A mode control

Pin #	Pin Name	Assignment	Description
17	P2.1	GPIO	General Purpose I/O (unused in CRD5378)
18	P2.0	GPIO	General Purpose I/O (CS5378 RESETz)
19	P1.7	BYP_EN	I2C bypass switch control
20	P1.6	SDA_DE	I2C data driver enable
21	P1.5	SCL	I2C clock in/out
22	P1.4	SDA	I2C data in/out
23	P1.3	SS	SPI chip select output, active low
24	P1.2	MOSI	SPI master out / slave in

Pin #	Pin Name	Assignment	Assignment
25	P1.1	MISO	SPI master in / slave out
26	P1.0	SCK	SPI serial clock
27	P0.7		Internal VREF bypass capacitors
28	P0.6	DRDYz	Data ready input, active low
29	P0.5	RX	UART receiver
30	P0.4	TX	UART transmitter
31	P0.3	4.096MHZ	External clock input
32	P0.2	TIMEB	Time Break output

Many connections to the C8051F320 microcontroller are inactive by default, but are provided for convenience during custom reprogramming. Listed below are the default active connections to the microcontroller and how they are used.

2.3.2.1 SPI Interface

The microcontroller SPI interface communicates with the CS5378 digital filter to write/read configuration information and collect conversion data from the SPI port. Detailed information about interfacing to the digital filter SPI port can be found in the CS5378 data sheet.

2.3.2.2 USB Interface

The microcontroller USB interface communicates with the PC evaluation software to receive configuration commands and return collected conversion data. The USB interface uses the Silicon Laboratories API and Windows drivers, which are available free from the internet (http://www.silabs.com).

2.3.2.3 Reset Source

By default, the C8051F320 microcontroller receives its reset signal from the internal power-on reset. This reset signal can be used to output to the CS5378 digital filter.

2.3.2.4 Clock Source

By default, the C8051F320 microcontroller uses an internally generated 12 MHz clock for compatibility with USB standards.

2.3.2.5 Timebreak Signal

By default, the C8051F320 microcontroller sends the TIMEB signal to the digital filter for the first collected sample of a data record. By default, 100 initial samples are skipped during data collection to ensure the CS5378 digital filters are fully settled, and the timebreak signal is automatically set for the first ‘real’ collected sample.

2.3.2.6 C2 Debug Interface

Through the PC evaluation software, the microcontroller default firmware can be automatically flashed to the latest version without connecting an external programmer. To flash custom firmware, software tools and an inexpensive hardware programmer that connects to the C2 Debug Interface on CRD5378 is available for purchase from Silicon Laboratories (DEBUGADPTR1-USB).

2.3.3 RS-485 Telemetry

By default, CRD5378 communicates with the PC evaluation software through the microcontroller USB port. Additional hardware is designed onto CRD5378 to use the microcontroller I^2C port as a low-level local telemetry, but it is provided for custom programming convenience only and is not directly supported by the CRD5378 PC evaluation software or microcontroller firmware.

Telemetry signals enter CRD5378 through RS-485 transceivers, which are differential current mode transceivers that can reliably drive long distance communication. Data passes through the RS-485 transceivers to the microcontroller I^2C interface and the clock and synchronization inputs.

Specification	Value
RS-485 Transceiver - Linear Tech	LTC1480IS8
Surface Mount Package Type	SOIC-8, 5mm x 6mm
Supply Voltage, Quiescent Current	3.3V, 600 µA
Maximum Data Rate	2.5 Mbps
Transmitter Delay, Receiver Delay	25 - 80 ns, 30 - 200 ns
Transmitter Current, Full Termination (60 Ω)	25 mA
Transmitter Current, Half Termination (120 Ω)	13 mA

2.3.3.1 CLK, SYNC

Clock and synchronization telemetry signals into CRD5378 are received through RS-485 twisted pairs. These signals are required to be distributed through the external system with minimal jitter and timing skew, and so are normally driven through high-speed bus connections.

Specification	Value
Synchronous Inputs, 2 wires each	CLK±, SYNC±

Specification	Value
Distributed SYNC Signal Synchronization	± 240 ns
Distributed Clock Synchronization	± 240 ns
Analog Sampling Synchronization Accuracy	± 480 ns

Synchronization of the measurement channel is critical to ensure simultaneous analog sampling across a network. Several options are available for connecting a SYNC signal through the RS-485 telemetry to the digital filter.

A direct connection is made when the SYNC_IO signal is received over the dedicated RS-485 twisted pair and sent directly to the digital filter SYNC pin (with a 0 Ω resistor installed at R71). The incoming SYNC_IO signal must be synchronized to the network at the transmitter since no local timing adjustment is available.

A microcontroller hardware connection is made when the SYNC_IO signal is received over the dedicated RS-485 twisted pair and detected by a microcontroller interrupt. The microcontroller can then use an internal counter to re-time the SYNC signal output to the digital filter SYNC input as required.

A microcontroller software connection is made when the SYNC signal output is created by the microcontroller on command from the system telemetry. The microcontroller can use an internal counter to re-time the SYNC signal output to the digital filter SYNC input as required.

2.3.3.2 I^2C - SCL, SDA, Bypass

The I^2C® telemetry connections to CRD5378 transmit and receive through RS-485 twisted pairs. Because signals passing through the transceivers are actively buffered, full I^2C bus arbitration and error detection cannot be used (i.e. high-impedance NACK).

The I^2C inputs and outputs can be externally wired to create either a daisy chain or a bus type network, depending how the telemetry system is to be implemented. Analog switches included on CRD5378 can bypass the I^2C signals to create a bus network from a daisy chain network following address assignment.

Specification	Value
I2C Inputs, 2 wires each	SCL±, SDA±
I2C Outputs, 2 wires each	BYP_SCL±, BYP_SDA±
I2C Bypass Switch Control	BYP_EN

When CRD5378 is used in a distributed measurement network, each node must have a unique address. This address is used to transmit individual configuration commands and tag the source of returned conversion data. Address assignment can be either dynamic or static, depending how the telemetry system is to be implemented.

Dynamic address assignment uses daisy-chained I^2C connections to assign an address to each measurement node. Once a node receives an address, it enables the I^2C bypass switches to the next node so it can be assigned an address.

Static address assignment has a serial number assigned to each node during manufacturing. When placed in the network the location is recorded and a master list of serial numbers vs. location is maintained. Alternately, a location dependent serial number can be assigned during installation.

2.3.4 UART Connection

A UART connection on CRD5378 provides a low-speed standardized connection for telemetry solutions not using I^2C. UART connections are provided for custom programming convenience only and are not directly supported by the CRD5378 PC evaluation software or microcontroller firmware.

Specification	Value
UART Connections, 2 wires each	TX/GND, RX/GND

2.3.5 External Connector

Power supplies and telemetry signals route to J26, a 20-pin double row connector with 0.1" spacing. This header provides a compact standardized connection to the CRD5378 external signals.

Pins	Name	Signal
1, 2	CLK+, CLK-	Clock Input
3, 4	SYNC+, SYNC-	Synchronization Input
5, 6	SCL+, SCL-	I2C Clock
7, 8	SDA+, SDA-	I2C Data
9, 10	BYP_SDA+, BYP_SDA-	I2C Data Bypass
11, 12	BYP_SCL+, BYP_SCL-	I2C Clock Bypass
13, 14	TX, GND	UART transmit
15, 16	RX, GND	UART receive
17, 18	-3.3V, GND	Negative Power Supply
19, 20	+3.3V, GND	Positive Power Supply

2.4 Power Supplies

Power is supplied to CRD5378 through the +3.3 V and -3.3 V voltage inputs on the external connector (J26), which are typically from an external AC-DC or DC-DC converter. Digital circuitry on CRD5378 is driven directly from the +3.3 V input, while on-board linear regulators create +2.5 V and - 2.5 V analog power supplies from +3.3 V and -3.3 V.

The +3.3 V and -3.3 V power supply inputs have zener protection diodes that limit the maximum input voltages to +5 V or -5 V with respect to ground. Each input also has 68 uF bulk capacitance for bypassing and to help settle transients and another 0.01 uF capacitor to bypass high frequency noise.

2.4.1 Analog Voltage Regulators

Linear voltage regulators create the positive and negative analog power supply voltages to the analog components on CRD5378. These regulate the +3.3 V and -3.3 V power supply inputs to create the +2.5 V and -2.5 V analog power supplies.

Specification	Value
Positive Analog Power Supply	+2.5 V
Low Noise Micropower Regulator - Linear Tech	LT1962ES8-2.5
Surface Mount Package Type	MSOP-8
Load Regulation, -40 C to +85 C	+/- 25 mV
Quiescent Current, Current @ 100 mA Load	30 µA, 2 mA
Output Voltage Noise, 10 Hz - 100 kHz	20 μV_{RMS}
Ripple Rejection, DC - 200 Hz	> 60 dB

Specification	Value
Negative Analog Supply	-2.5 V
Low Noise Micropower Regulator - Linear Tech	LT1964ES5-BYP
Surface Mount Package Type	SOT-23
Load Regulation, -40 C to +85 C	+/- 30 mV
Quiescent Current, Current @ 100 mA Load	30 µA, 1.3 mA
Output Voltage Noise, 10 Hz - 100 kHz	20 μV_{RMS}
Ripple Rejection, DC - 200 Hz	> 45 dB

The +2.5 V and -2.5 V power supplies to the analog components on CRD5378 include reverse biased Schottky diodes to ground to protect against reverse voltages that could latch-up the CMOS analog components. Also included on +2.5 V and -2.5 V are 68 uF bulk capacitors for bypassing and to help settle transients plus individual 0.1 uF bypass capacitors local to the power supply pins of each device.

2.5 PCB Layout

2.5.1 Layer Stack

CRD5378 layers 1 and 6 are dedicated as analog routing layers. All critical routes are on these two layers. Some microcontroller digital routes are also included on these layers away from the analog signal routes.

CRD5378 layer 2 is a solid ground plane without splits or routing. A solid ground plane provides the best return path for bypassed noise to leave the system. No separate analog ground is required since analog signals on CRD5378 are differentially routed.

CRD5378 layer 3 is dedicated for power supply routing. Each power supply net includes at least 68 µF bulk capacitance as a charge well for settling transient currents.

CRD5378 layer 4 is dedicated as a digital routing layer.

CRD5378 layer 5 is a solid ground plane without splits or routing. A solid ground plane provides the best return path for bypassed noise to leave the system. No separate analog ground is required since analog signals on CRD5378 are differentially routed.

2.5.2 Differential Pairs

Analog signal routes on CRD5378 are differential with dedicated + and - traces. All source and return analog signal currents are constrained to the differential pair route and do not return through the ground plane. Differential traces are routed together with a minimal gap between them so that noise events affect them equally and are rejected as common mode noise.

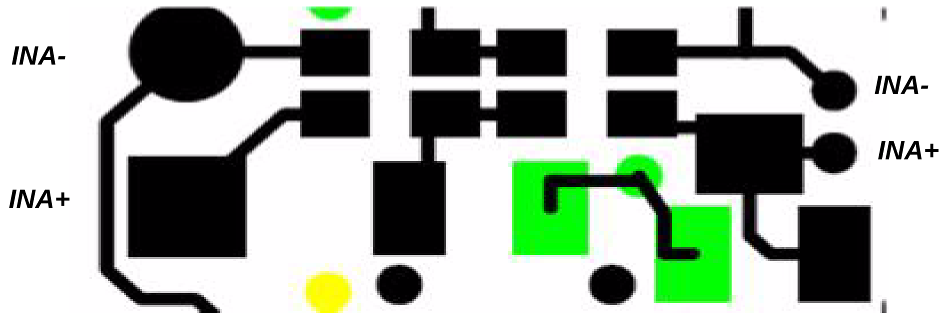


Figure 2. Differential Pair Routing

Analog signal connections into the CS3301A/02A amplifiers are 2-wire IN+ and IN- differential pairs, and are routed as such. Analog signal connections out of the CS3301A/02A amplifiers and into the CS5372 modulators are 4-wire INR+, INF+, INF-, INR- quad groups, and are routed with INF+ and INF- as a traditional differential pair and INR+ and INR- as guard traces outside the respective INF+ and INF- traces.

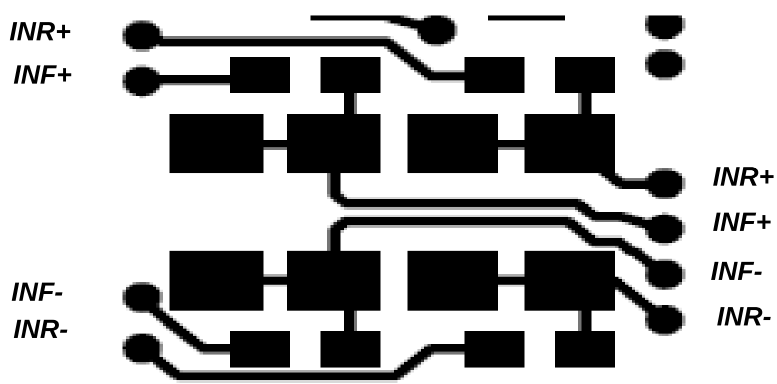


Figure 3. Quad Group Routing

2.5.3 Bypass Capacitors

Each device power supply pin includes 0.1 µF bypass capacitors placed as close as possible to the pin. Each power supply net includes at least 68 µF bulk capacitance as a charge well for transient current loads.

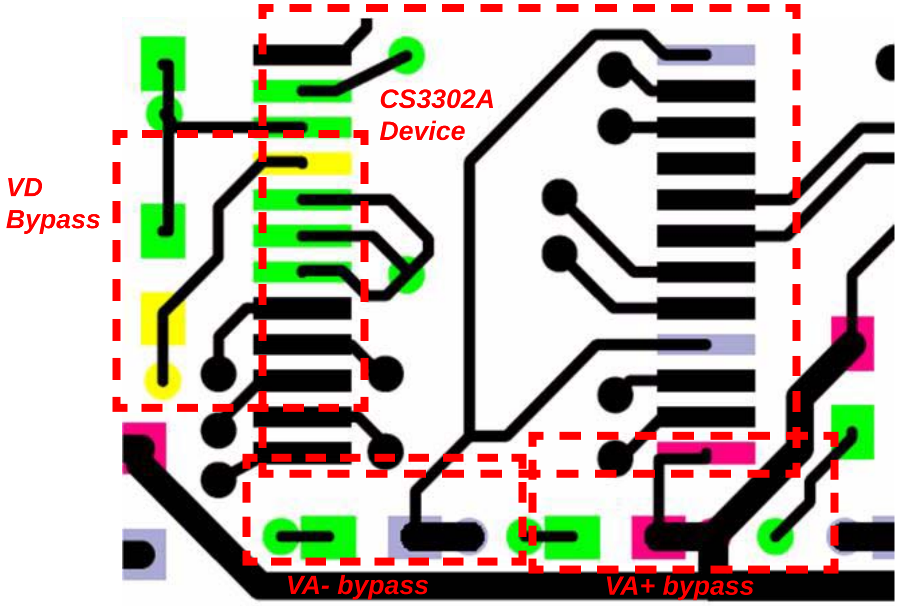


Figure 4. Bypass Capacitor Placement

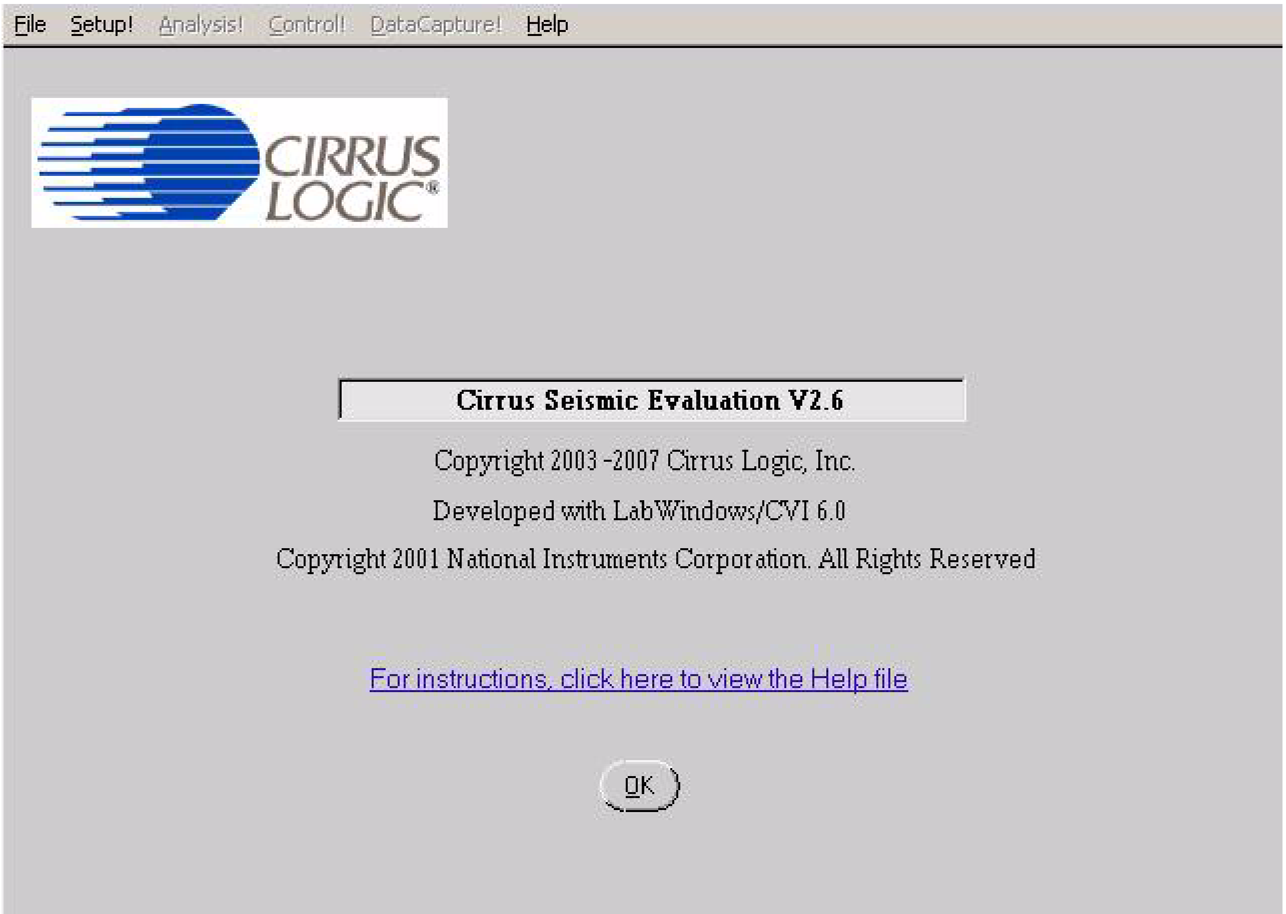
3. SOFTWARE DESCRIPTION

3.1 Menu Bar

The menu bar is always present at the top of the software panels and provides typical *File* and *Help* pull-down menus. The menu bar also selects the currently displayed panel.

Control		Description
File		
	Load Data Set	Loads a data set from disk.
	Save Data Set	Saves the current data set to disk.
	Copy Panel to Clipboard	Copies a bitmap of the current panel to the clipboard.
	Print Analysis Screen	Prints the full Analysis panel, including statistics fields.
	Print Analysis Graph	Prints only the graph from the Analysis panel.
	High Resolution Printing	Prints using the higher resolution of the printer.
	Low Resolution Printing	Prints using the standard resolution of the screen.
	Quit	Exits the application software.
Setup!		Displays the Setup Panel.
Analysis!		Displays the Analysis Panel.
Control!		Displays the Control Panel.
DataCapture!		Displays the Setup Panel and starts Data Capture.
Help		
	Contents	Find help by topic.
	Search for help on	Find help by keywords.
	About	Displays the About Panel.

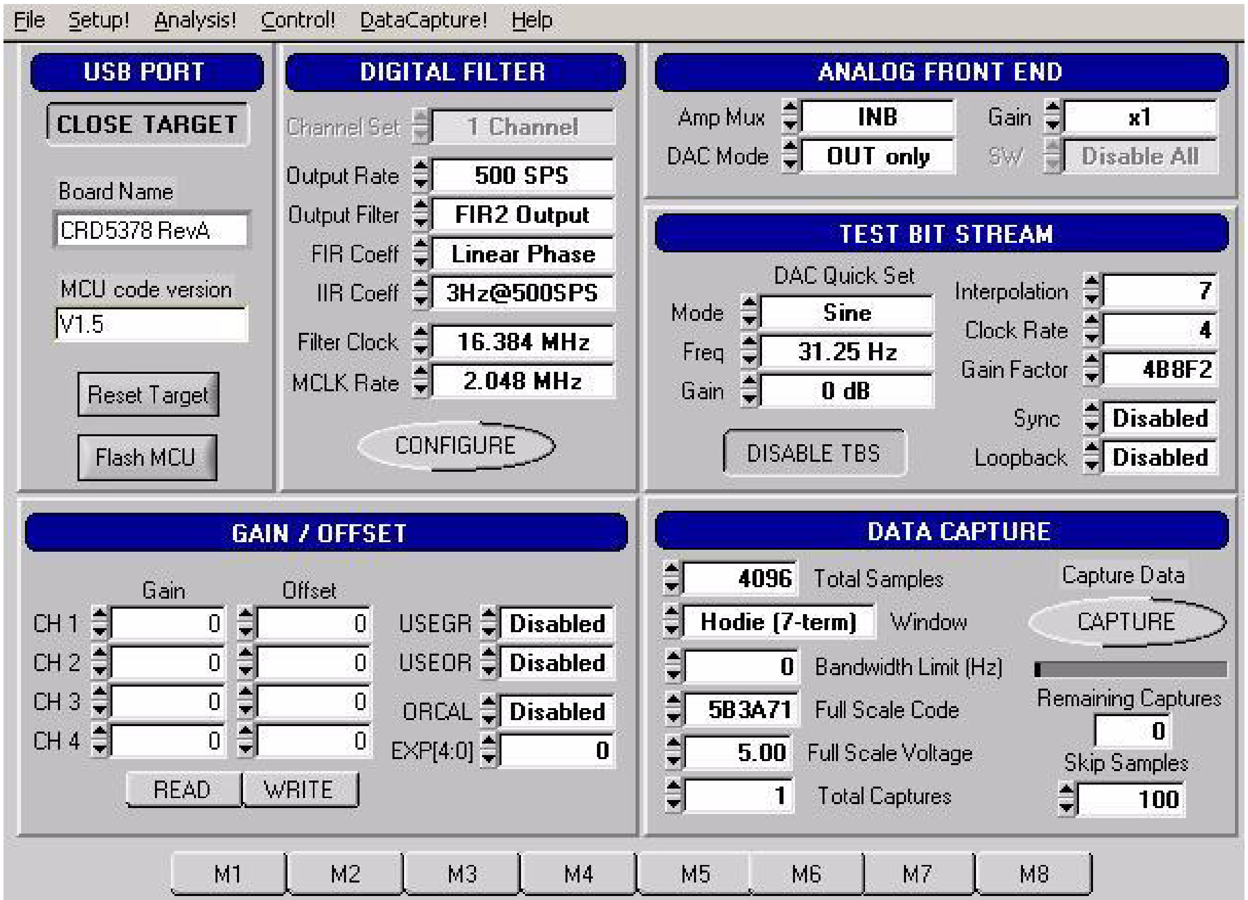
3.2 *About* Panel



The ***About*** panel displays copyright information for the Cirrus Seismic Evaluation software.

Click *OK* to exit this panel. Select *Help* ⇨ *About* from the menu bar to display this panel.

3.3 *Setup* Panel



The ***Setup*** panel initializes the evaluation system to perform data acquisition. It consists of the following sub-panels and controls.

- ***USB Port***
- ***Digital Filter***
- ***Analog Front End***
- ***Test Bit Stream***
- ***Gain/Offset***
- ***Data Capture***
- ***External Macros***

3.3.1 USB Port

The ***USB Port*** sub-panel sets up the USB communication interface between the PC and the target board.

Control	Description
Open Target	Open USB communication to the target board and read the board name and micro-controller firmware version. When communication is established, the name of this control changes to *'Close Target'* and ***Setup***, ***Analysis*** and ***Control*** panel access becomes available in the menu bar.
Close Target	Disconnects the previously established USB connection. On disconnection, this control changes to *'Open Target'* and the ***Setup***, ***Analysis*** and ***Control*** panel access becomes unavailable in the menu bar. The evaluation software constantly monitors the USB connection status and automatically disconnects if the target board is turned off or the USB cable is unplugged.
Board Name	Displays the type of target board currently connected.
MCU code version	Displays the version number of the microcontroller code on the connected target board.
Reset Target	Sends a software reset command to the target board.
Flash MCU	Programs the microcontroller code on the target board using the *.thx* file found in the *"C:\Program Files\Cirrus Seismic Evaluation"* directory. This feature permits reprogramming of the microcontroller (without using a hardware programmer) when a new version of the MCU code becomes available.

3.3.2 Digital Filter

The ***Digital Filter*** sub-panel sets up the digital filter configuration options.

By default the ***Digital Filter*** sub-panel configures the system to use on-chip coefficients and test bit stream data. The on-chip data can be overwritten by loading custom coefficients and test bit stream data from the ***Customize*** sub-panel on the ***Control*** panel.

Any changes made under this sub-panel will not be applied to the target board until the *Configure* button is pushed. The *Configure* button writes the new configuration to the target board and then enables the data *Capture* button.

Control	Description
Channel Set	Selects the number of channels that are enabled in the digital filter. For the CS5378 digital filter, only 1 can be enabled.
Output Rate	Selects the output word rate of the digital filter. Output word rates from 4000 SPS to 1 SPS (0.25 mS to 1 S) are available.
Output Filter	Selects the output filter stage from the digital filter. Sinc output, FIR1 output, FIR2 output, IIR 1st order output, IIR 2nd order output, or IIR 3rd order output can be selected. FIR2 output provides full decimation of the modulator data.
FIR Coeff	Selects the on-chip FIR coefficient set to use in the digital filter. Linear phase or minimum phase FIR coefficients can be selected.
IIR Coeff	Selects the on-chip IIR coefficient set to use in the digital filter. Coefficient sets producing a 3 Hz high-pass corner at 2000 SPS, 1000 SPS, 500 SPS, 333 SPS, and 250 SPS can be selected.
Filter Clock	Sets the digital filter internal clock rate. Lower internal clock rates can save power when using slow output word rates.
MCLK Rate	Sets the analog sample clock rate. The CS5373A modulator and test DAC typically run with MCLK set to 2.048 MHz.
Configure	Writes all information from the ***Setup*** panel to the digital filter. The data *Capture* button becomes available once the configuration information is written to the target board.

3.3.3 Analog Front End

The ***Analog Front End*** sub-panel configures the amplifier, modulator, and test DAC pin options. Pin options are controlled through the GPIO outputs of the digital filter.

Any changes made under this sub-panel will not be applied to the target board until the *Configure* button is pushed. The *Configure* button writes the new configuration to the target board and then enables the data *Capture* button.

Control	Description
Amp Mux	Selects the input source for the CS3301A/02A amplifiers. An internal termination, external INA inputs or external INB inputs can be selected.
DAC Mode	Selects the operational mode of the CS5373A test DAC. The test DAC operational modes are AC dual output (OUT&BUF), AC precision output (OUT only), AC buffered output (BUF only), DC common mode output (DC Common), DC differential output (DC Diff), or AC common mode output (AC Common). The test DAC can also be powered down (PWDN) when not in use to save power.
Gain	Sets the amplifier gain range and test DAC attenuation. Amplifier gain and DAC attenuation settings of 1x, 2x, 4x, 8x, 16x, 32x, or 64x can be selected and are controlled together.
Sw	Selects how the DAC_BUF to INA analog switches are enabled when connected to the CRD5376. This control is not applicable to the CRD5378 and is disabled.

3.3.4 Test Bit Stream

The ***Test Bit Stream*** sub-panel configures test bit stream (TBS) generator parameters. The digital filter data sheet describes TBS operation and options.

The *DAC Quick Set* controls automatically set the *Interpolation*, *Clock Rate*, and *Gain Factor* controls based on the selected *Mode*, *Freq*, and *Gain*. Additional configurations can be programmed by writing the *Interpolation*, *Clock Rate*, and *Gain Factor* controls manually.

Any changes made under this sub-panel will not be applied to the target board until the *Configure* button is pushed. The *Configure* button writes the new configuration to the target board and then enables the data *Capture* button.

Control	Description
DAC Quick Set	Automatically sets test bit stream options. *Mode* selects sine or impulse output mode, *Freq* selects the test signal frequency for sine mode, and *Gain* selects the test signal amplitude in dB.
Interpolation	Manual control for the data interpolation factor of the test bit stream generator.
Clock Rate	Manual control for the output clock and data rate of the test bit stream generator.
Gain Factor	Manual control to set the test bit stream signal amplitude.
Sync	Enables test bit stream synchronization by the MSYNC signal.
Loopback	Enables digital loopback from the test bit stream generator output to the digital filter input.

3.3.5 Gain/Offset

The ***Gain / Offset*** sub-panel controls the digital filter GAIN and OFFSET registers for each channel.

The OFFSET and GAIN registers can be manually written with any 24-bit 2's complement value from 0x800000 to 0x7FFFFF. The USEGR, USEOR, ORCAL, and EXP[4:0] values enable gain correction, offset correction, and offset calibration in the digital filter.

The offset calibration routine built into the digital filter is enabled by writing the ORCAL and EXP[4:0] bits. The EXP[4:0] value can range from 0x00 to 0x18 and represents an exponential shift of the calibration feedback, as described in the digital filter data sheet. Offset calibration results are automatically written to the OFFSET registers and remain there, even after offset calibration is disabled.

Control	Description
Gain	Displays the digital filter GAIN1 to GAIN4 registers.
Offset	Displays the digital filter OFFSET1 to OFFSET4 registers.
Read	Reads values from the GAIN and OFFSET registers.
Write	Writes values to the GAIN and OFFSET registers.
USEGR	Enables gain correction. When enabled, output samples are gained down by the value in the GAIN register.(Output = GAIN / 0x7FFFFF).
USEOR	Enables offset correction. When enabled, output samples are offset by the value in the OFFSET register. (Output = Sample - OFFSET).
ORCAL	Enables offset calibration using the exponent value from the EXP[4:0] control. Results are automatically written to the OFFSET registers as they are calculated.
EXP[4:0]	Sets the exponential value used by offset calibration.

3.3.6 Data Capture

The ***Data Capture*** sub-panel collects samples from the target board and sets analysis parameters.

When the *Capture* button is pressed, the requested number of samples are collected from the target board through the USB port. The maximum number of samples that can be collected is 1,048,576 (1M). The number of samples per channel should be a power of two for the analysis FFT routines to work properly.

After data is collected, analysis is performed using the selected parameters and the results are displayed on the ***Analysis*** panel. The selected analysis *window*, *bandwidth limit*, *full scale code*, and *full scale voltage* parameters can be modified for the data set currently in memory and the analysis re-run by pressing the *REFRESH* button on the ***Analysis*** Panel.

Control	Description
Total Samples	Sets the total number of samples to be collected. Multichannel acquisitions split the requested number of samples among the channels. A maximum of 1,048,576 (1M) samples can be collected.
Window	Selects the type of analysis windowing function to be applied to the collected data set. Used to ensure proper analysis of discontinuous data sets.
Bandwidth Limit (Hz)	Sets the frequency range over which to perform analysis, used to exclude higher-frequency components. Default value of zero performs analysis for the full Nyquist frequency range.
Full Scale Code	Defines the maximum positive full-scale 24-bit code from the digital filter. Used during FFT noise analysis to set the 0 dB reference level.
Full Scale Voltage	Defines the maximum peak-to-peak input voltage for the $nV/\sqrt{Hz}$ Spot Noise analysis.
Total Captures	Sets the number of data sets to be collected and averaged together in the FFT magnitude domain. The maximum number of data sets that can be averaged is 100.
Capture	Starts data collection from the target board through the USB port. After data collection, analysis is run using parameters from this sub-panel.
Remaining Captures	Indicates how many more data captures are remaining to complete the requested number of *Total Captures*. A zero value means that the current data capture is the last one.
Skip Samples	Sets the total number of samples to be skipped prior to data collection. A maximum of 64K samples can be skipped

3.3.7 External Macros

Macros are generated within the ***Macros*** sub-panel on the ***Control*** panel. Once a macro has been built it can either be saved with a unique macro name to be run within the ***Macros*** sub-panel, or saved as an external macro and be associated with one of the *External Macro* buttons.

A macro is saved as an *External Macro* by saving it in the *. /macros/* subdirectory using the name *'m1.mac'*, *'m2.mac'*, etc. Depending on the selected name the macro will be associated with the corresponding *External Macro* button *M1*, *M2*, etc.

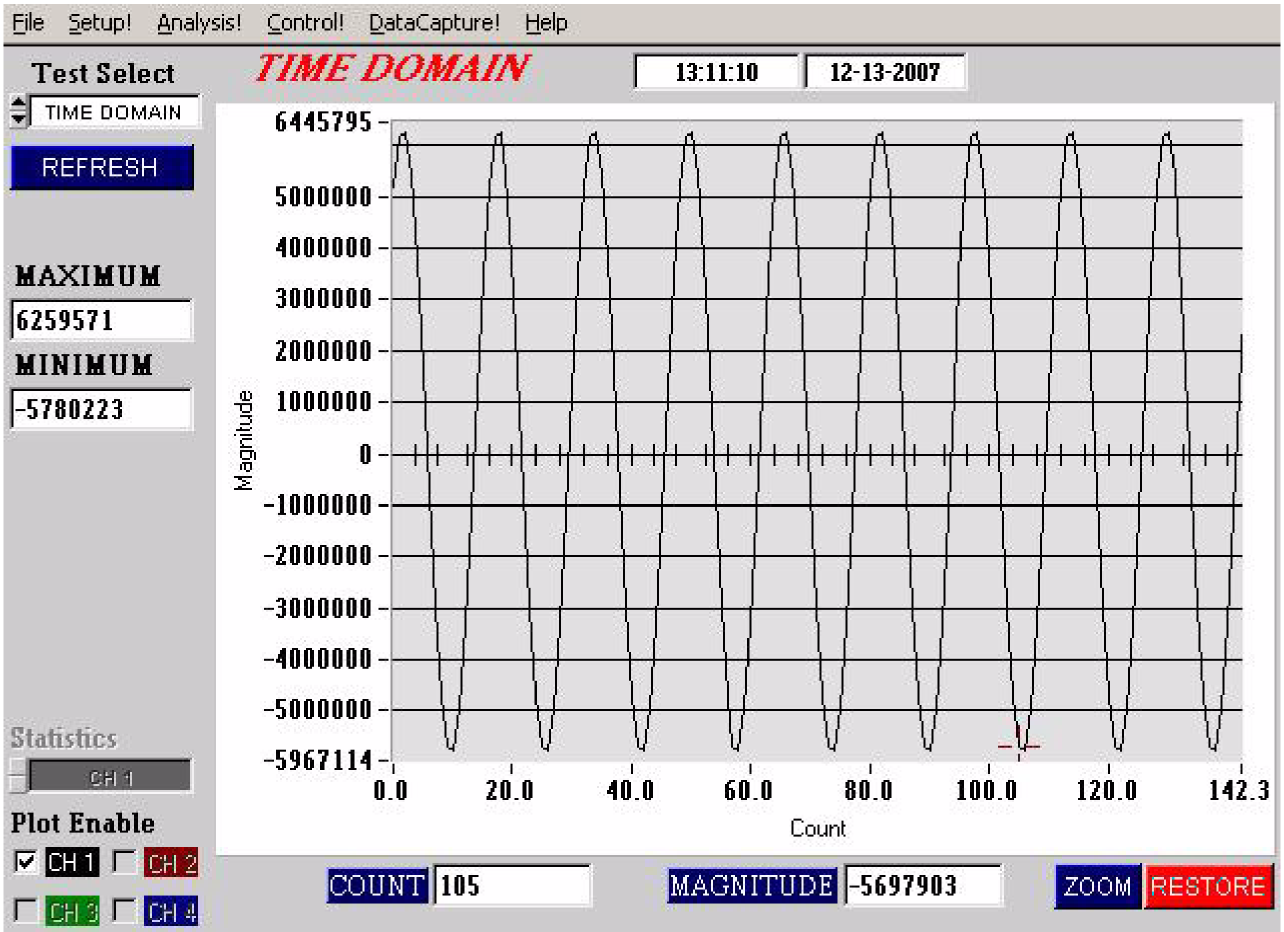
- M1 = . /macros/m1.mac
- M2 = . /macros/m2.mac
- etc.

External Macro buttons can be re-named on the panel by right clicking on them. The button name will change, but the macro associated with that button is always saved as '*m1.mac'*, *'m2.mac'*, etc., in the *. /macros/* subdirectory. The *External Macro* button names are stored in the file *'Mnames.txt'*, also in the *. /macros/* subdirectory.

*External Macro*s allow up to eight macros to be accessed quickly without having to load them into the ***Macros*** sub-panel on the ***Control*** panel. These *External Macro*s operate independently of the ***Macros*** sub-panel and are not affected by operations within it, except when a macro is saved to the *. /macros/* subdirectory to replace a currently existing *External Macro*.

Control	Description
M1 - M8	Runs the *External Macro* associated with that button.

3.4 *Analysis* Panel



The ***Analysis*** panel is used to display the analysis results on collected data. It consists of the following controls.

- ***Test Select***
- ***Statistics***
- ***Plot Enable***
- ***Cursor***
- ***Zoom***
- ***Refresh***
- ***Harmonics***
- ***Spot Noise***
- ***Plot Error***

3.4.1 Test Select

The *Test Select* control sets the type of analysis to be run on the collected data set.

Control	Description
Time Domain	Runs a min / max calculation on the collected data set and then plots sample data value vs. sample number.
Histogram	Runs a histogram calculation on the collected data set and then plots sample occurrence vs. sample value. Only valid for noise data since sine wave data varies over too many codes to plot as a histogram.
Signal FFT	Runs an FFT on the collected data set and then plots frequency magnitude vs. frequency. Statistics are calculated using the largest frequency bin as a full-scale signal reference.
Noise FFT	Runs an FFT on the collected data set and then plots frequency magnitude vs. frequency. Statistics are calculated using a simulated full-scale signal as a full-scale signal reference.

3.4.2 Statistics

The *Statistics* control displays calculated statistics for the selected analysis channel. For multichannel data captures, only one channel of calculated statistics are displayed at a time and is selected using the *Statistics* channel control.

Errors that affect statistical calculations will cause the *Plot Error* control to appear. Information about errors on specific channels can be accessed by enabling the plot of the channel using the *Plot Enable* control and then accessing the *Plot Error* controls.

Control	Description
Time Domain	
Max	Maximum code of collected data set.
Min	Minimum code of collected data set.
Histogram	
Max	Maximum code of collected data set.
Min	Minimum code of collected data set.
Mean	Mean of collected data set.
Std Dev	Standard Deviation of collected data set.
Variance	Variance of collected data set.
Signal FFT	
S/N	Signal to Noise of calculated FFT.
S/PN	Signal to Peak Noise of calculated FFT.
S/D	Signal to Distortion of calculated FFT.
S/N+D	Signal to Noise plus Distortion of calculated FFT.
# of bins	Number of Bins covering the Nyquist frequency.
Noise FFT	
S/N	Signal to Noise of calculated FFT.
S/PN	Signal to Peak Noise of calculated FFT.
Spot Noise dB	Spot Noise in dB/$\sqrt{Hz}$ of calculated FFT.
Spot Noise nV	Spot Noise in nV/$\sqrt{Hz}$ of calculated FFT.
# of bins	Number of Bins covering the Nyquist frequency.

3.4.3 Cursor

The *Cursor* control is used to identify a point on the graph using the mouse and then display its plot values. When any point within the plot area of the graph is clicked, the *Cursor* will snap to the closest plotted point and the plot values for that point display below the graph.

When using the *Zoom* function, the *Cursor* is used to select the corners of the area to zoom.

3.4.4 Zoom

The *ZOOM* function allows an area on the graph to be expanded.

To use the zoom function, click the *ZOOM* button and select the box corners of the area on the graph to expand. The graph will then expand to show the details of this area, and the plot axes will be re-scaled. While zoomed, you can zoom in farther by repeating the process.

To restore the graph to its original scale, click the *RESTORE* button that appears while zoomed. If multiple zooms have been initiated, the *RESTORE* button will return to the previously viewed plot scale. Repeated *RESTORE* will eventually return to the original plot scale. From within multiple zooms the original scale can be directly restored by clicking the *REFRESH* button.

3.4.5 Refresh

The *REFRESH* button will clear and re-plot the current data set. *Refresh* can be used to apply new analysis parameters from the ***Data Capture*** sub-panel, or to restore a *ZOOM* graph to its default plot scale.

3.4.6 Harmonics

The *HARMONICS* control is only visible during a Signal FFT analysis and highlights the fundamental and harmonic bins used to calculate the Signal FFT statistics. *HARMONICS* highlighting helps to understand the source of any Signal FFT plot errors.

3.4.7 Spot Noise

The *Spot Noise* control (labeled *dB* or *nV*) is only visible during a Noise FFT analysis and selects the units used for plotting the graph, either dB/$\sqrt{Hz}$ or nV/$\sqrt{Hz}$. The dB/Hz plot applies the *Full Scale Code* value from the ***Data Capture*** sub-panel on the ***Setup*** panel to determine the 0 dB point of the dB axis. The nV/$\sqrt{Hz}$ plot applies the *Full Scale Voltage* value from the ***Data Capture*** sub-panel on the ***Setup*** panel to determine the absolute scaling of the nV axis.

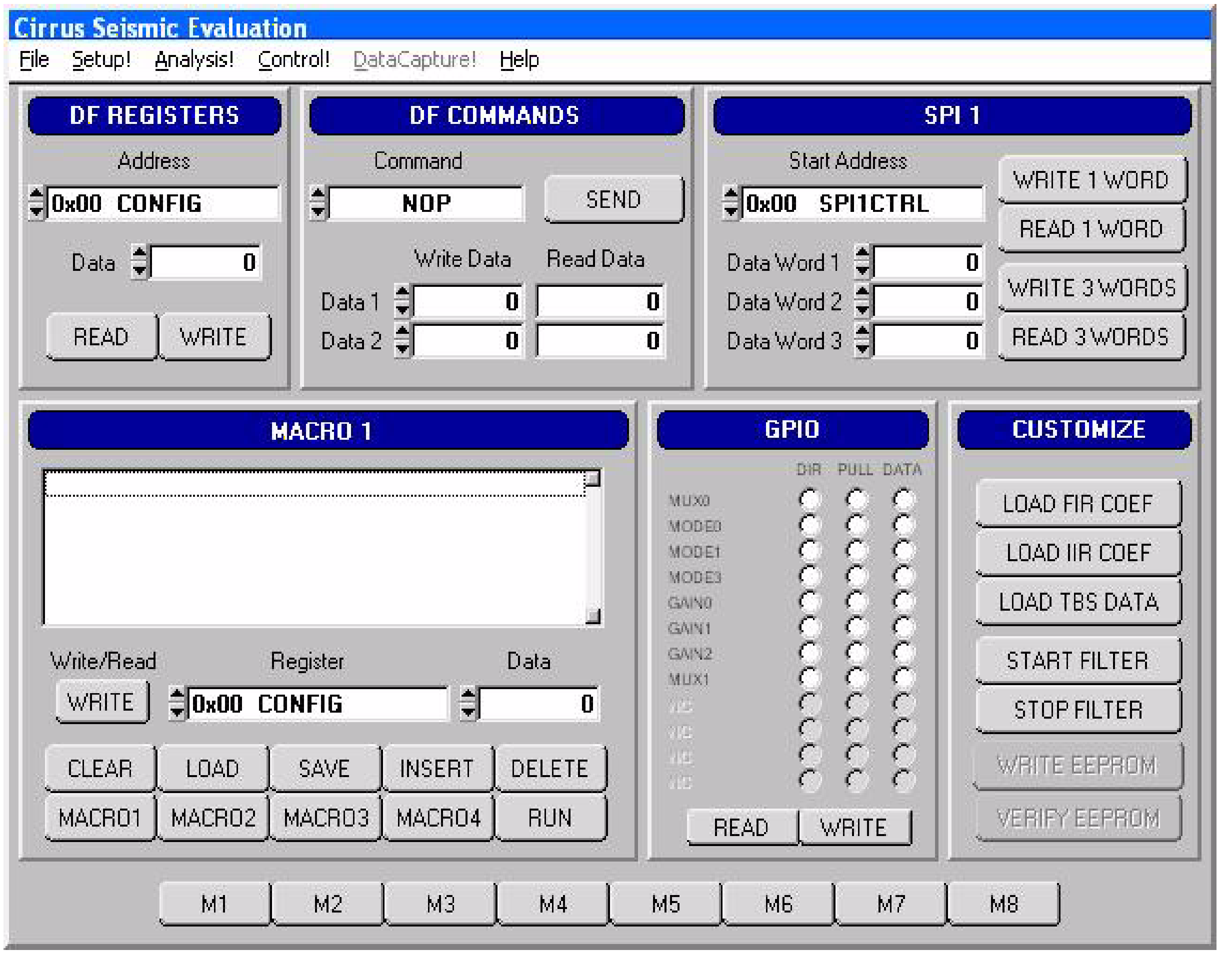
3.4.8 Plot Error

The *PLOT ERROR* control provides information about errors that occurred during an analysis. Analysis errors are only reported if the channel that has the error is currently plotted.

An analysis error stores an error code in the numerical display box of the *PLOT ERROR* control. If more than one error occurs, all error codes are stored and the last error code is displayed. Any of the accumulated error codes can be displayed by clicking on the numerical box and selecting it.

Once an error code is displayed in the numerical box, a description can be displayed by clicking the *PLOT ERROR* button. This causes a dialog box to display showing the error number, the error channel, and a text error message.

3.5 *Control* Panel



The ***Control*** panel is used to write and read register settings and to send commands to the digital filter. It consists of the following sub-panels and controls.

- ***DF Registers***
- ***DF Commands***
- ***SPI1***
- ***Macros***
- ***GPIO***
- ***Customize***
- ***External Macros***

3.5.1 DF Registers

The ***DF Registers*** sub-panel writes and reads registers within the digital filter. Digital filter registers control operation of the digital filter and the included hardware peripherals, as described in the digital filter data sheet.

Control	Description
Address	Selects a digital filter register.
Data	Contains the data written to or read from the register.
Read	Initiates a register read.
Write	Initiates a register write.

3.5.2 DF Commands

The ***DF Commands*** sub-panel sends commands to the digital filter. The digital filter commands and their required parameters are described in the digital filter data sheet.

Not all commands require write data values, and not all commands will return read data values. Some commands require formatted data files for uploading custom coefficients or test bit stream data Example formatted data files are included in the SPI sub-directory of the software installation.

Control	Description
Command	Selects the command to be written to the digital filter.
Write Data 1	Contains the SPI1DAT1 data to be written to the digital filter.
Write Data 2	Contains the SPI1DAT2 data to be written to the digital filter.
Read Data 1	Contains the SPI1DAT1 data read from the digital filter.
Read Data 2	Contains the SPI1DAT2 data read from the digital filter.
Send	Initiates the digital filter command.

3.5.3 SPI

The ***SPI*** sub-panel writes and reads registers in the digital filter SPI register space. They can be used to check the SPI serial port status bits or to manually write commands to the digital filter.

Control	Description
Start Address	Selects the address to begin the SPI transaction.
Data Word 1	Contains the first data word written to or read from the SPI registers.
Data Word 2	Contains the second data word written to or read from the SPI registers.
Data Word 3	Contains the third data word written to or read from the SPI registers.
Read 1 Word	Initiates a 1 word SPI read transaction.
Read 3 Words	Initiates a 3 word SPI read transaction.
Write 1 Word	Initiates a 1 word SPI write transaction.
Write 3 Words	Initiates a 3 word SPI write transaction.

3.5.4 Macros

The ***Macros*** sub-panel is designed to write a large number of registers with a single command. This allows the target evaluation system to be quickly set into a specific state for testing.

The *Register* control gives access to both digital filter registers and SPI1 registers. These registers can be written with data from the *Data* control, or data can be read and output to a text window. The *Register* control can also select special commands to be executed, with the *Data* control used to define a parameter value for the special command, if necessary.

Control	Description
Write / Read	Selects the type of operation to be performed by the inserted macro command.
Register	Selects the target register for the inserted macro command. Also selects special commands that can be performed.
Data	Sets the register data value for the inserted macro command. Also sets the parameter value for special commands.
Clear	Clears the currently displayed macro.
Load	Loads a previously saved macro.
Save	Saves the currently displayed macro. Macros can be saved with unique names or can be saved as *External Macros*.
Insert	Inserts a macro command at the selected macro line. The macro command is built from the *Write/Read*, *Register*, and *Data* controls.
Delete	Deletes the macro command at the selected macro line.
Macro1 - Macro4	Selects which of the four working macros is displayed.
Run	Runs the currently displayed working macro.

3.5.5 GPIO

The ***GPIO*** sub-panel controls the digital filter GPIO pin configurations. GPIO pins have dedicated functions on the target board, but can be used in any manner for custom designs.

Control	Description
Direction	Sets the selected GPIO pin as an output (*) or input ( ).
Pull Up	Turns the pull up resistor for the selected GPIO pin on (*) or off ( ).
Data	Sets the selected output GPIO pin to a high (*) or low ( ) level.
Write	Initiates a write to GPIO registers.The *Direction*, *Pull Up* and *Data* controls are read to determine the register values to be written.
Read	Initiates a read from GPIO registers.The *Direction*, *Pull Up* and *Data* controls are updated based on the register values that are read.

3.5.6 Customize

The ***Customize*** sub-panel sends commands to upload custom FIR and IIR filter coefficients, upload custom test bit stream data, start the digital filter, stop the digital filter, and write/read custom EEPROM configuration files to the on-board boot EEPROM. Example data files are included in a sub-directory of the software installation.

Control	Description
Load FIR Coef	Write a set of FIR coefficients into the digital filter from a file.
Load IIR Coef	Write a set of IIR coefficients into the digital filter from a file.
Load TBS Data	Write a set of test bit stream data into the digital filter from a file.
Start Filter	Enables the digital filter by sending the *Start Filter* command.
Stop Filter	Disables the digital filter by sending the *Stop Filter* command.

3.5.7 External Macros

Macros are generated within the ***Macros*** sub-panel on the ***Control*** panel. Once a macro has been built it can either be saved with a unique macro name to be run within the ***Macros*** sub-panel, or saved as an external macro and be associated with one of the *External Macro* buttons.

A macro is saved as an *External Macro* by saving it in the *. /macros/* subdirectory using the name *'m1.mac'*, *'m2.mac'*, etc. Depending on the selected name the macro will be associated with the corresponding *External Macro* button *M1*, *M2*, etc.

- M1 = . /macros/m1.mac
- M2 = . /macros/m2.mac
- etc.

External Macro buttons can be re-named on the panel by right clicking on them. The button name will change, but the macro associated with that button is always saved as *'m1.mac'*, *'m2.mac'*, etc., in the *. /macros/* subdirectory. The *External Macro* button names are stored in the file *'Mnames.txt'*, also in the *. /macros/* subdirectory.

*External Macro*s allow up to eight macros to be accessed quickly without having to load them into the ***Macros*** sub-panel on the ***Control*** panel. These *External Macro*s operate independently of the ***Macros*** sub-panel and are not affected by operations within it, except when a macro is saved to the *. /macros/* subdirectory to replace a currently existing *External Macro*.

Control	Description
M1 - M8	Runs the *External Macro* associated with that button.

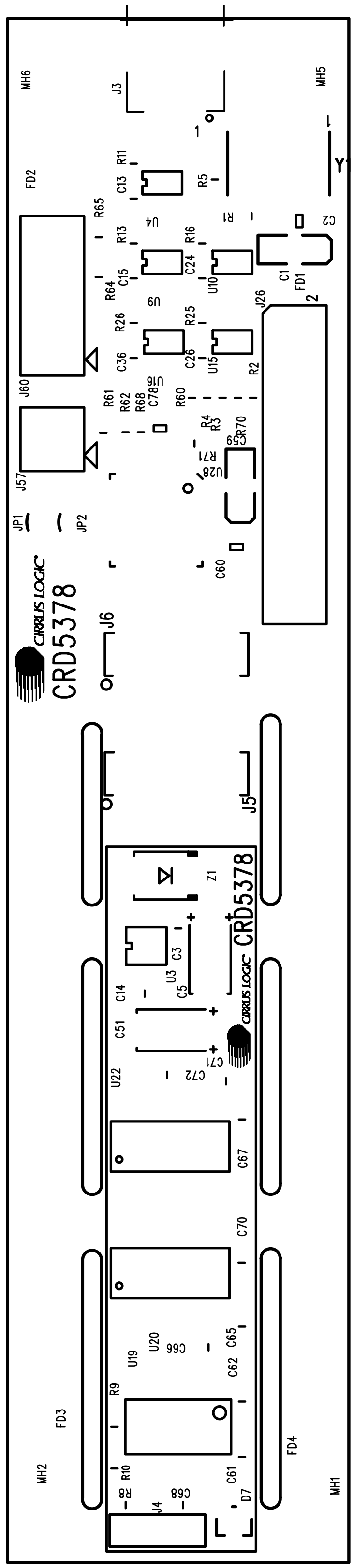
4. BILL OF MATERIALS

CIRRUS LOGIC
CRD5378_Rev_A1.PL

BILL OF MATERIAL

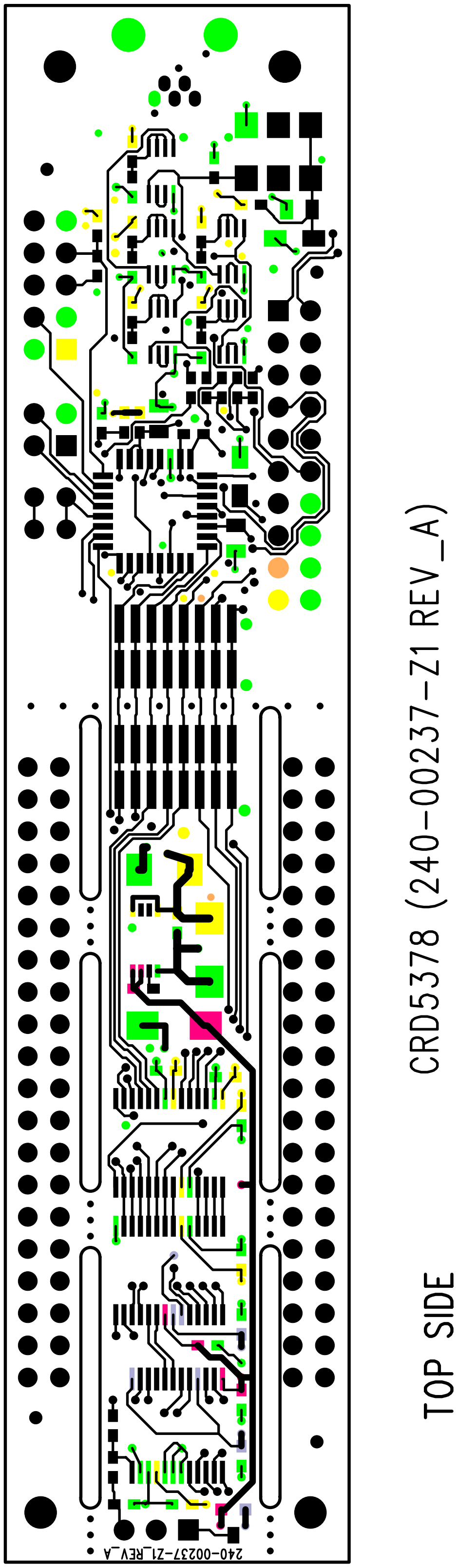
Item	Cirrus P/N	Rev	Description	Qty	Reference Designator	MFG	MFG P/N	Notes
1	004-00068-Z1	A	CAP 4.7uF ±10% 10V NPb TANT CASE A	2	C1 C59	KEMET	T491A475K010AS	
2	001-04345-Z1	A	CAP 0.1uF ±10% 50V X7R NPb 0805	7	C2 C11 C12 C31 C48 C60 C78	KEMET	C0805C104K5RAC	
3	001-01997-Z1	A	CAP 0.01uF ±10% 25V X7R NPb 0603	4	C3 C6 C7 C14	KEMET	C0603C103K3RAC	
4	004-00092-Z1	A	CAP 68uF ±10% 10V TANT NPb CASE C	5	C4 C5 C20 C51 C53	KEMET	T491C686K010AT	
5	001-02194-Z1	A	CAP 0.1uF ±10% 25V X7R NPb 0603	21	C13 C15 C16 C24 C25 C26 C30 C33 C36 C44 C45 C49 C61 C62 C65 C66 C67 C68 C70 C71 C72	KEMET	C0603C104K3RAC	
6	001-06603-Z1	A	CAP 0.01uF ±5% 25V C0G NPb 1206	5	C37 C38 C39 C40 C41	KEMET	C1206C103J3GAC	
7	000-00008-Z1	A	NO POP CAP NPb 0805	0	C46 C50	NO POP	NP-CAP-0805	DO NOT POPULATE
8	070-00010-Z1	A	DIODE SCHTKY BAR 30V 0.2A NPb SOT23	1	D1	PHILIPS SEMICONDUCTORS	BAT54	
9	070-00024-Z1	A	DIODE SWT 70V 215mA NPb SOT-23	2	D7 D8	ON SEMICONDUCTOR	BAV99LT1G	
10	070-00055-Z1	A	DIODE ARRAY 5V (TVS) ESD NPb SOT143	1	D9	LITTELFUSE	SP0503BAHTG	
11	115-00221-Z1	A	HDR 8X2 ML .050" ST GLD NPb SM	4	J1 J2 J5 J6	SAMTEC	FTS-108-01-L-DV	
12	110-00263-Z1	A	CON USB RCPT RA 5POS MINI-B NPb TH	1	J3	MOLEX	54819-0519	
13	115-00054-Z1	A	HDR 3x1 ML .1"CTR S GLD NPb	1	J4	SAMTEC	TSW-103-26-G-S	
14	115-00011-Z1	A	HDR 10x2 ML .1" 062BD ST GLD NPb TH	1	J26	SAMTEC	TSW-110-07-G-D	
15	115-00013-Z1	A	HDR 2x2 ML .1"CTR .062BD S GLD NPb	1	J57	SAMTEC	TSW-102-07-G-D	
16	115-00003-Z1	A	HDR 5x2 ML .1"CTR S GLD NPb	1	J60	SAMTEC	TSW-105-07-G-D	
17	080-00004-Z1	A	WIRE JUMPER 2P 0.1" BRASS NPb TH	0	JP1 JP2	COMPONENTS CORPORATION	TP-101-10	NO POP
18	304-00004-Z1	A	SPCR STANDOFF 4-40 THR NPb .500"L	4	MH1 MH2 MH5 MH6	KEYSTONE	2203	REQUIRES SCREW 4-40X5X16" PH STEEL, 300-00001-01
19	020-00788-Z1	A	RES 10 OHM 1/10W ±1% NPb 0603 FILM	9	R1 R11 R13 R14 R16 R25 R26 R60 R68	DALE	CRCW060310R0FKEA	
20	000-00002-Z1	A	NO POP RES NPb 0603	0	R2 R3 R4 R8 R9 R15 R17 R22 R23 R32 R33 R39 R40 R41 R42 R45 R49 R50 R51 R55 R56 R61 R63 R69 R70	NO POP	NP-RES-0603	DO NOT POPULATE
21	020-01095-Z1	A	RES 4.99k OHM 1/10W ±1% NPb 0603	1	R5	DALE	CRCW06034K99FKEA	
22	020-01128-Z1	A	RES 9.53k OHM 1/10W ±1% NPb 0603	1	R6	DALE	CRCW06039K53FKEA	
23	020-01130-Z1	A	RES 10k OHM 1/10W ±1% NPb 0603 FILM	1	R7	DALE	CRCW060310K0FKEA	
24	020-00673-Z1	A	RES 0 OHM 1/10W ±5% NPb 0603 FILM	16	R10 R24 R34 R36 R43 R44 R46 R47 R48 R52 R53 R54 R57 R59 R62 R71	DALE	CRCW0603000Z0EA	ECO554
25	021-01391-Z1	A	RES 18M OHM 1/8W ±5% NPb 0805	2	R31 R38	PANASONIC	ERJ6GEYK186V	
26	020-01048-Z1	A	RES 2k OHM 1/10W ±1% NPb 0603 FILM	2	R35 R37	DALE	CRCW06032K00FKEA	
27	020-01016-Z1	A	RES 1k OHM 1/10W ±1% NPb 0603 FILM	4	R64 R65 R66 R67	DALE	CRCW06031K00FKEA	
28	020-06253-Z1	A	RES 412k OHM 1/4W ±1% NPb 1206	1	R147	DALE	CRCW1206412KFKEA	
29	060-00195-Z1	A	IC LOW V DUL SPST ANA SW NPb MSP8	2	U1 U2	VISHAY	DG2003DQ-T1-E3	
30	060-00163-Z1	A	IC LNR 300mA LSE LDO REG NPb MSOP8	1	U3	LINEAR TECH	LT1962EMS8-2.5#PBF	
31	061-00062-Z1	A	IC LOG SGL D-FF CLR PREST NPb SSOP8	5	U4 U9 U10 U15 U16	TEXAS INSTRUMENTS	SN74LVC2G74DCTRE4	
32	060-00063-Z1	A	IC LNR V REG200mA NEGADJ NPbSOT23-5	1	U5	LINEAR TECH	LT1964ES5-BYP#PBF	
33	060-00162-Z1	A	IC 3.3V U LW PWR RS485 XCVR NPSOIC8	4	U12 U13 U17 U18	LINEAR TECH	LTC1480IS8#PBF	
34	060-00236-Z1	A	IC LNR PRC VRF 2.5V TC10 NPbSO8-150	1	U14	LINEAR TECH	LT1019AIS8-2.5#PBF	
35	065-00229-Z2	G	IC CRUS HI-Z DIDO AMP NPb SSOP24	1	U19	CIRRUS LOGIC	CS3302A-ISZ/G	ECO554
36	065-00196-Z1	A	IC CRUS TEST DAC NPb SSOP28	1	U20	CIRRUS LOGIC	CS5373A-ISZ/A	
37	065-00130-Z1	A	IC CRUS 1CH DIG FLTR NPb SSOP28	1	U22	CIRRUS LOGIC	CS5378-ISZ/A	
38	062-00079-Z1	A	IC PGM USB 16kB FLAS MCU NPb LQFP32	1	U28	SILICON LABORATORIES INC	C8051F320-GQ	
39	102-00017-Z2	A	OSC 32.768MHz 90ppm 3.3V VCL NPb SM	1	Y1	CITIZEN	CSX750VBEL32.768M-UT	
40	070-00053-Z1	A	DIODE ZEN TR SUP 5V 600W PK NPb SM	2	Z1 Z2	ON SEMICONDUCTOR	1SMB5.0AT3G	
41	603-00237-Z1	A	ASSY DWG PWA CRD5378-Z NPb	REF		CIRRUS LOGIC	603-00237-Z1	
42	240-00237-Z1	A	PCB CRD5378-Z NPb	1		CIRRUS LOGIC	240-00237-Z1	
43	600-00237-Z1	A1	SCHEM CRD5378-Z NPb	REF		CIRRUS LOGIC	600-00237-Z1	ECO554
44	300-00025-Z1	A	SCREW 4-40X5/16" PH MACH SS NPb	4	XMH1 XMH2 XMH5 XMH6	BUILDING FASTENERS	PMSSS 440 0031 PH	
45	020-06288-Z1	A	RES 680 OHM 1/10W ±1% NPb 0603 FILM	4	R27 R28 R29 R30	DALE	CRCW0603680RFKEA	ECO554

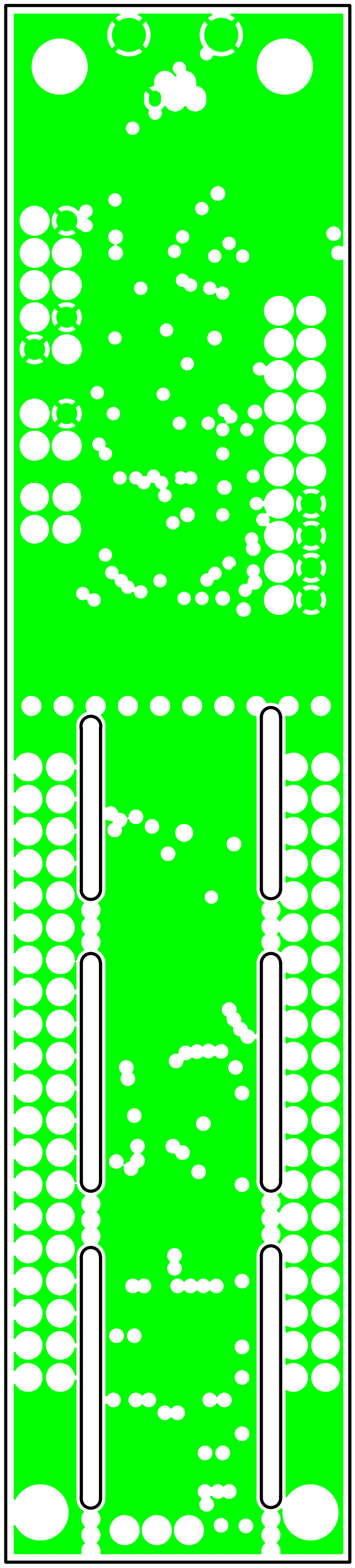
5. LAYER PLOTS



CRD5378 (240-00237-Z1 REV_A)

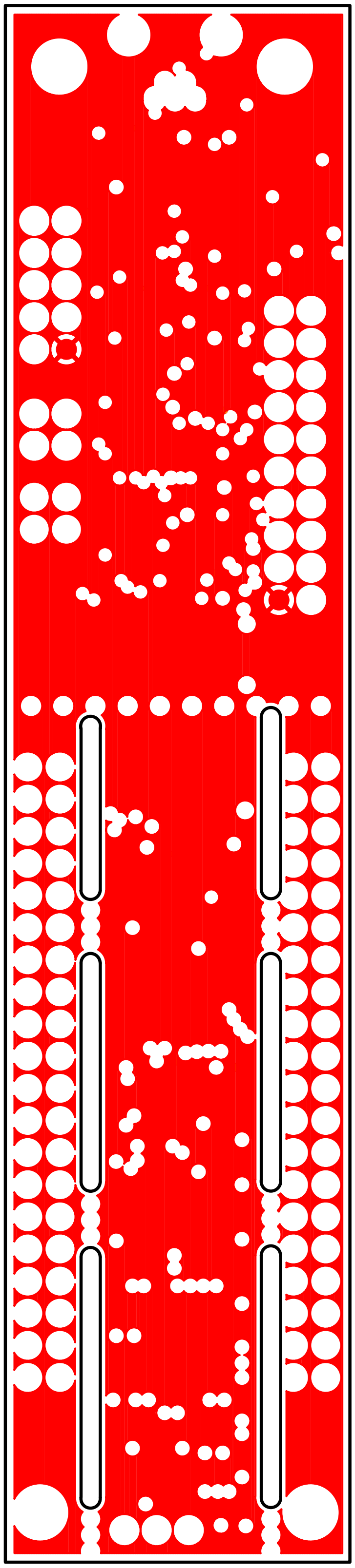
SILKSCREEN TOP


CRD5378 (240-00237-Z1 REV_A)
TOP SIDE
240-00237-Z1_REV_A



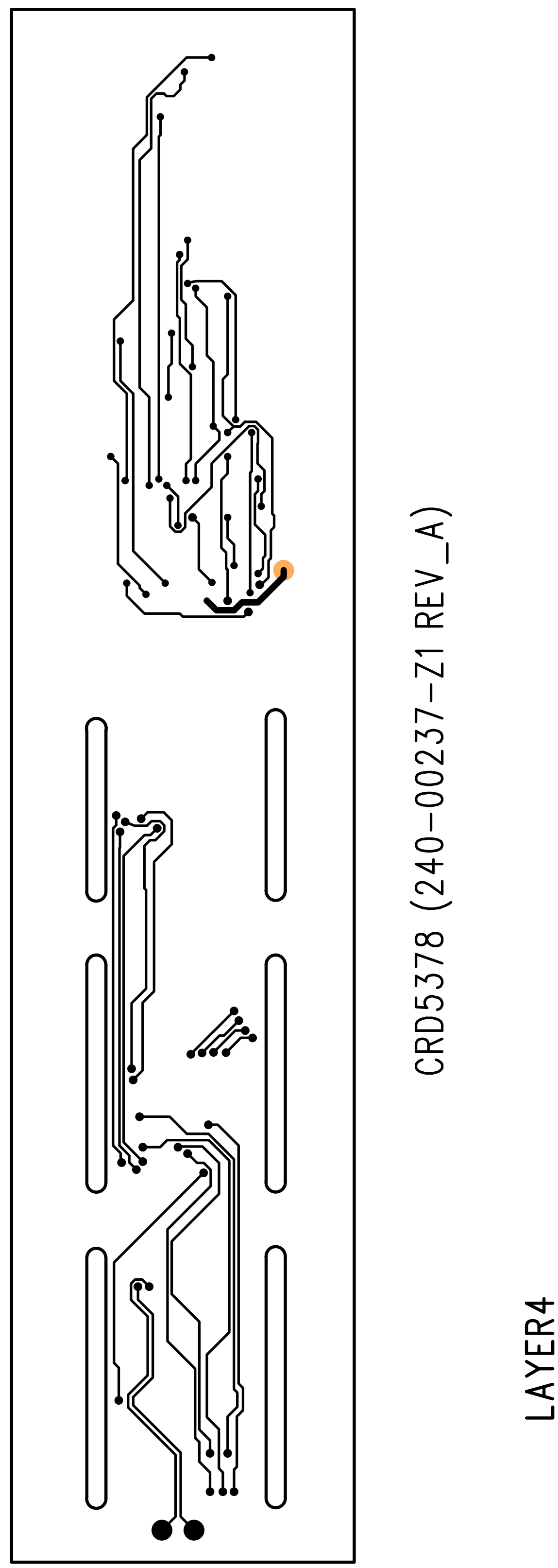
CRD5378 (240-00237-Z1 REV_A)

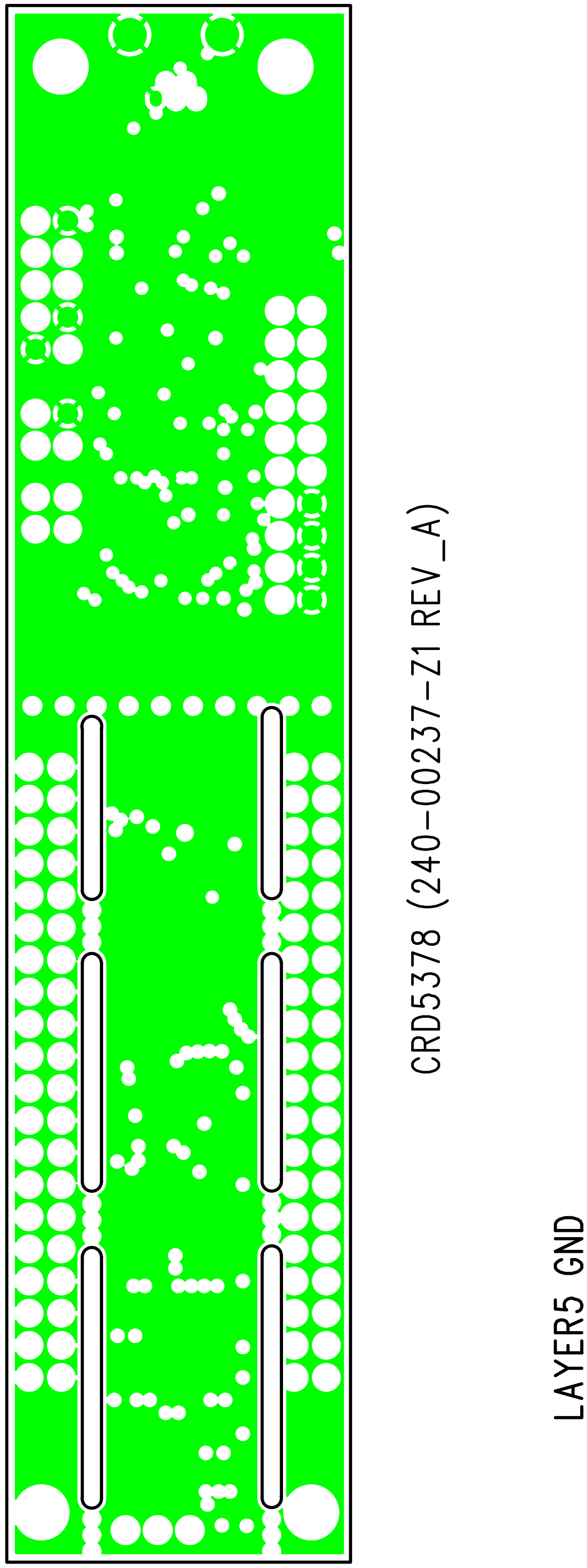
LAYER2 GND PLANE

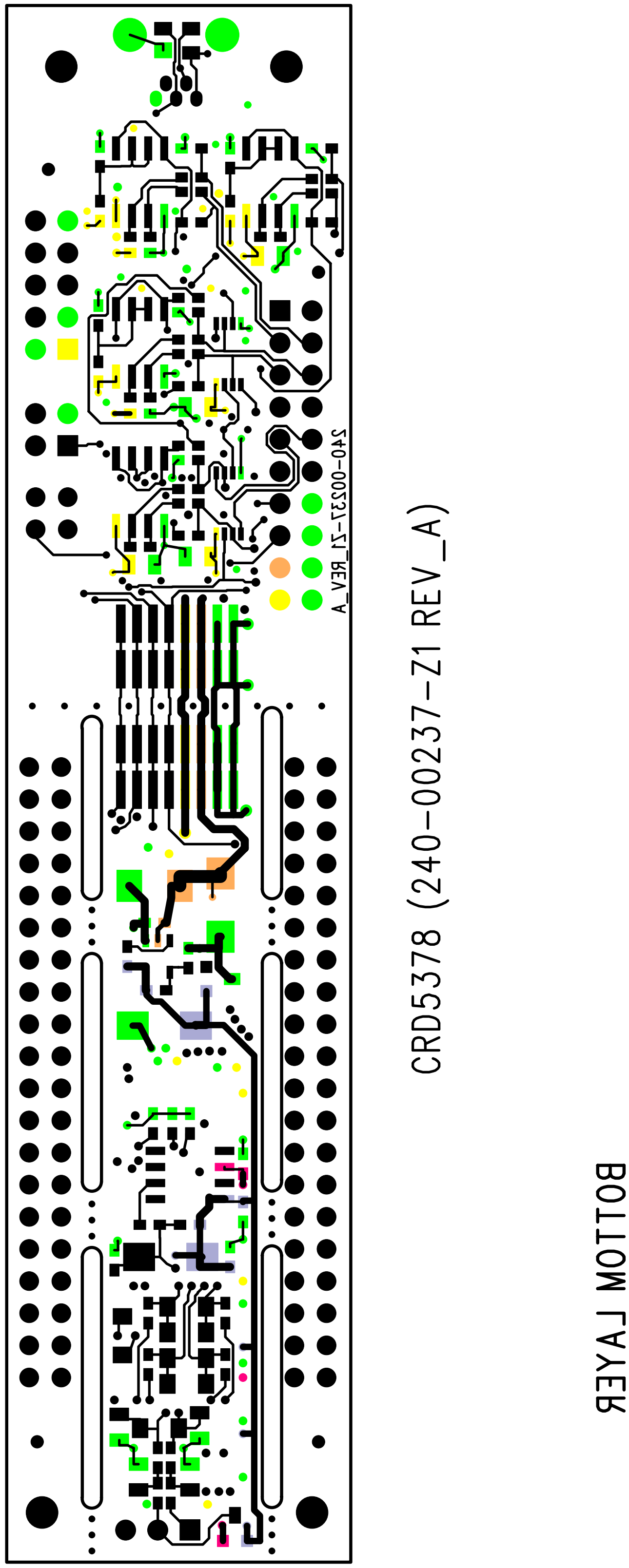


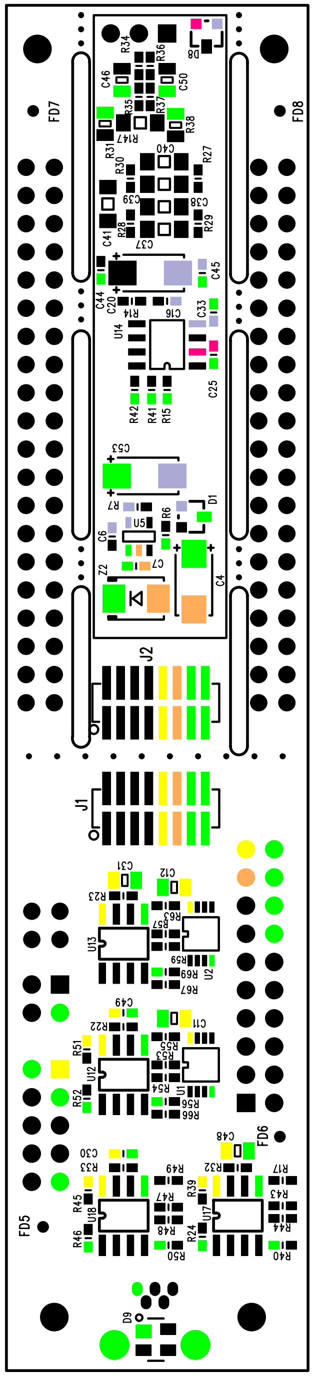
CRD5378 (240-00237-Z1 REV_A)

LAYER3 PWR PLANE


CRD5378 (240-00237-Z1 REV_A)
LAYER4


CRD5378 (240-00237-Z1 REV_A)
LAYER5 GND

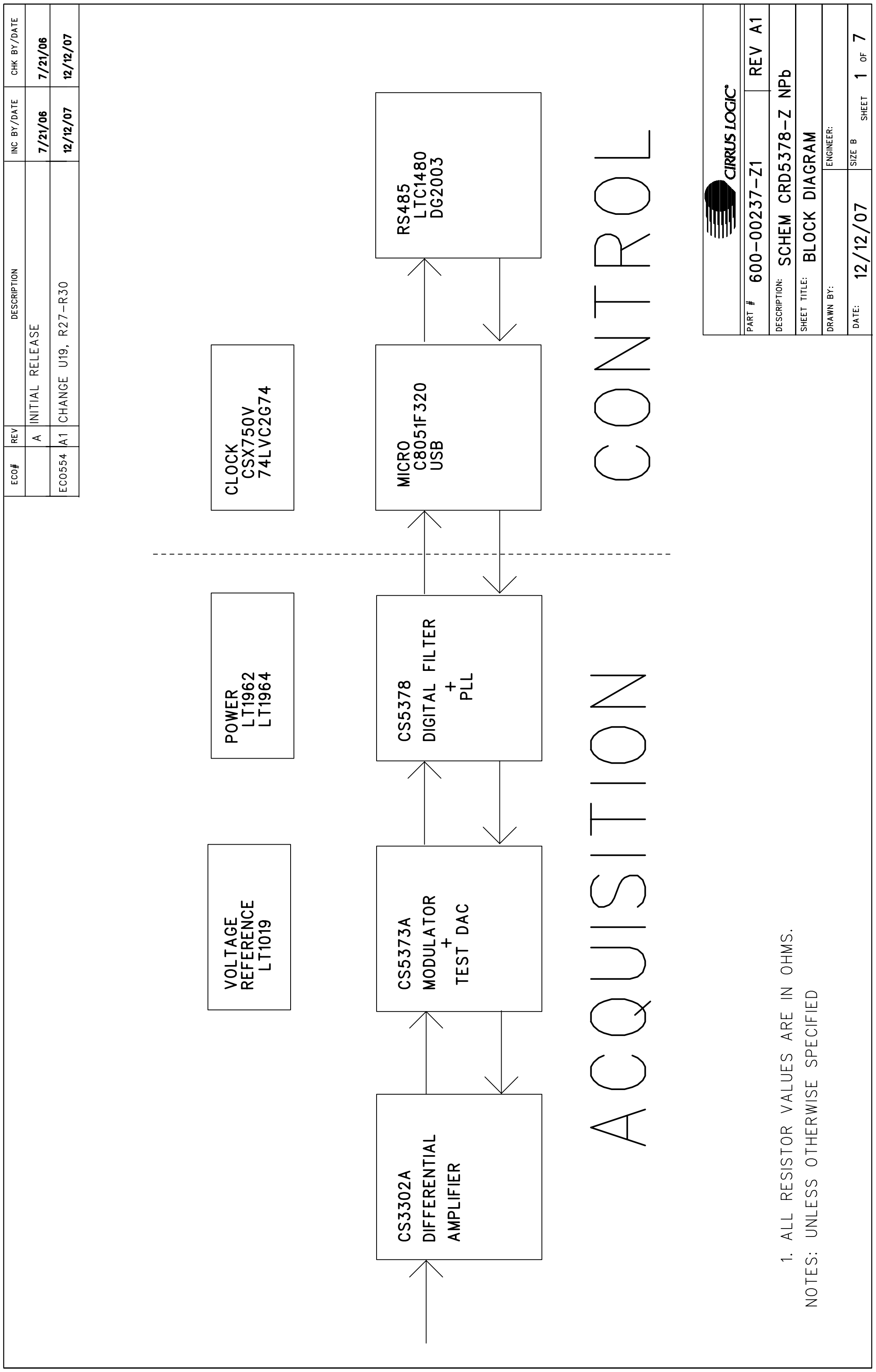

240-00237-Z1_REV_A
CRD5378 (240-00237-Z1 REV_A)
BOTTOM LAYER

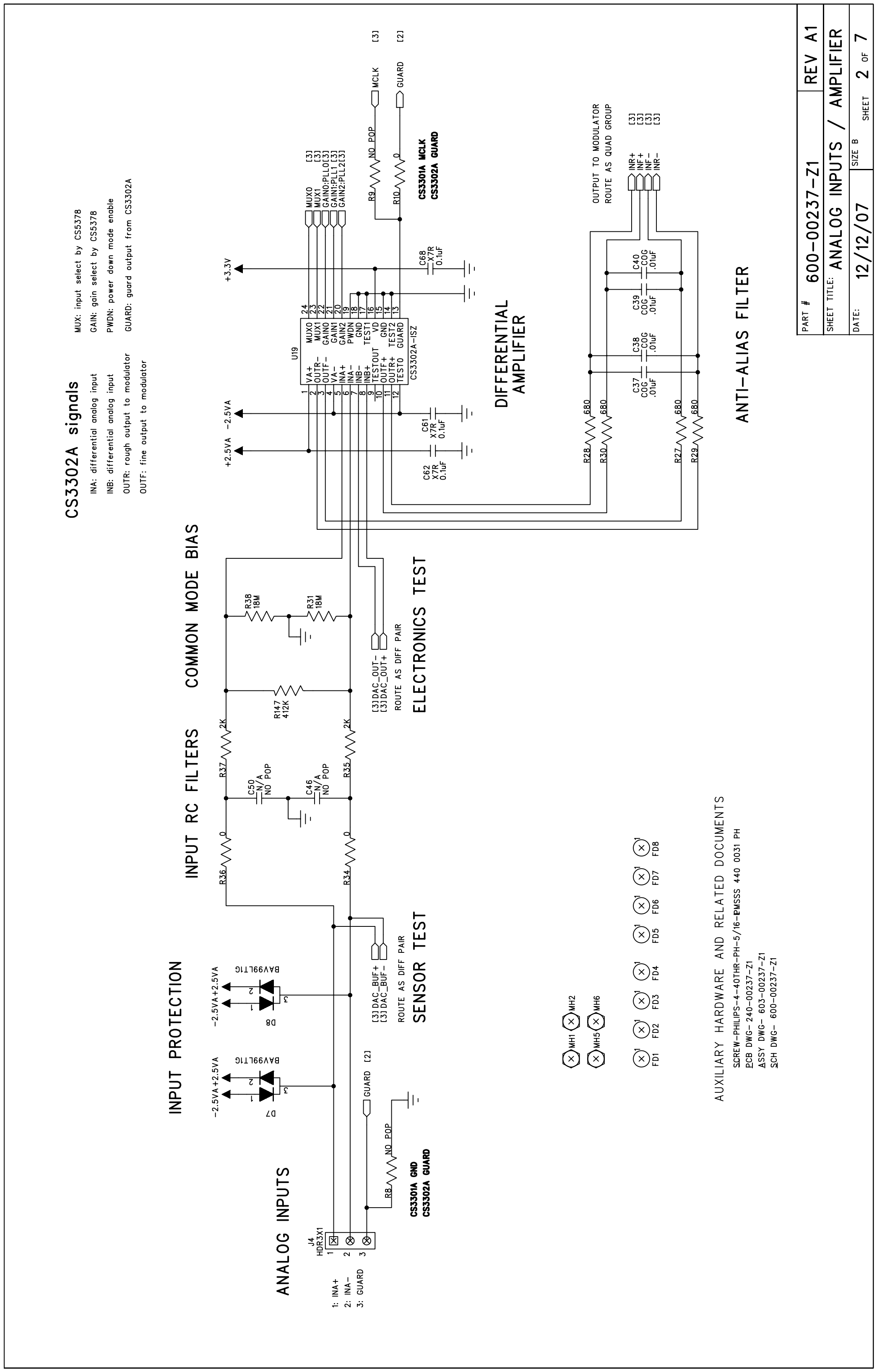


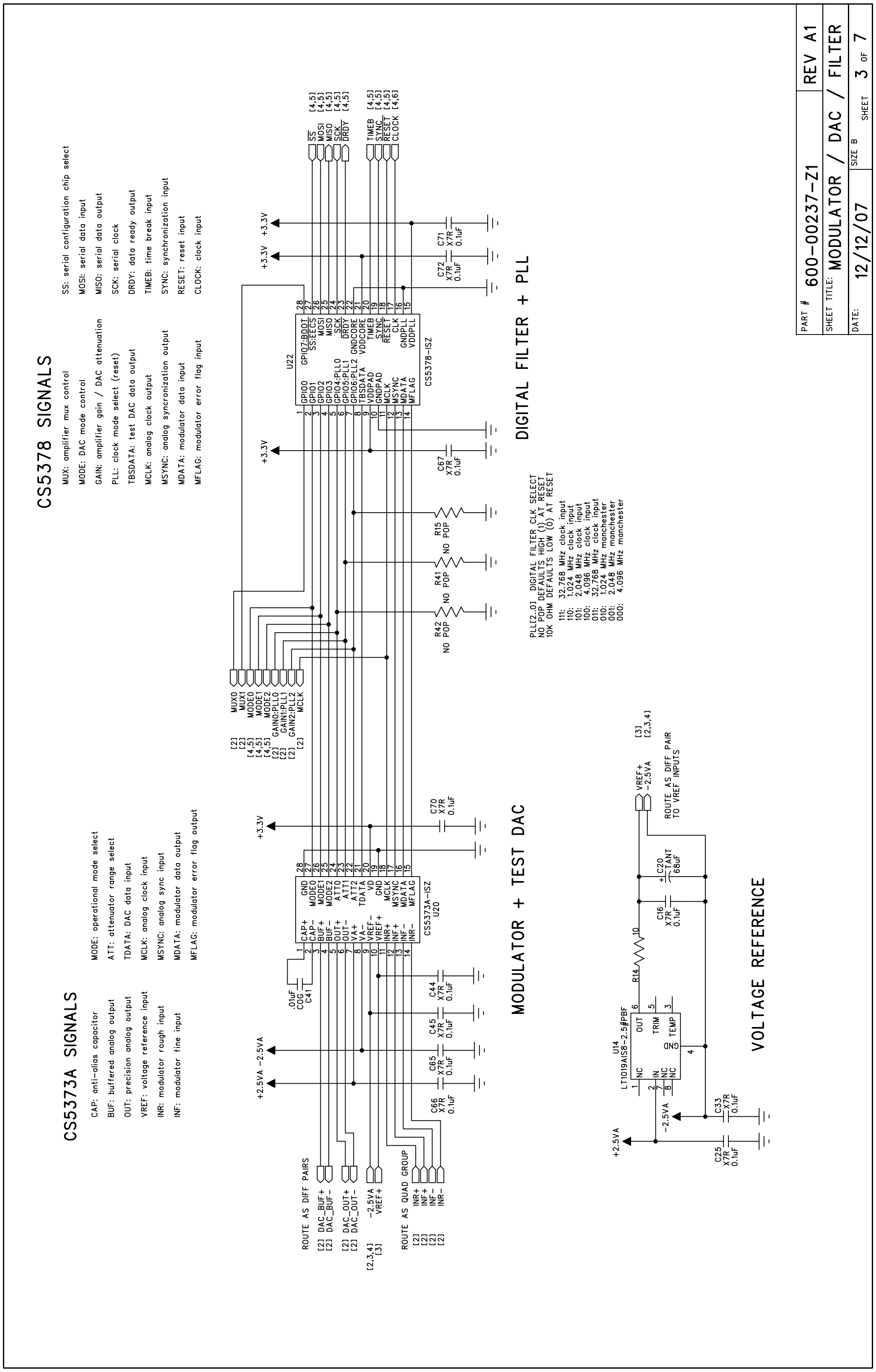
CRD5378 (240-00237-Z1 REV_A)

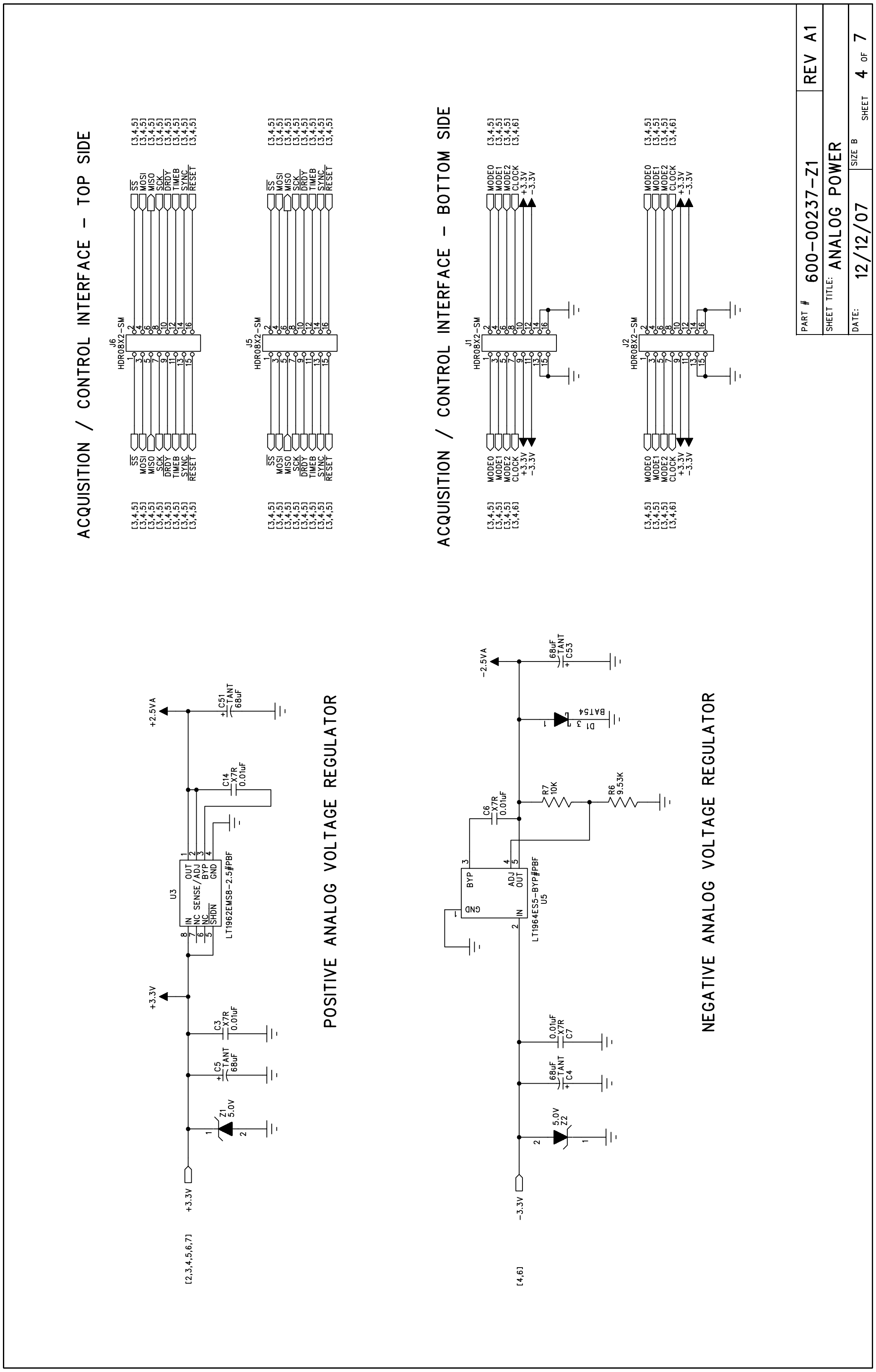
SILKSCREEN BOTTOM

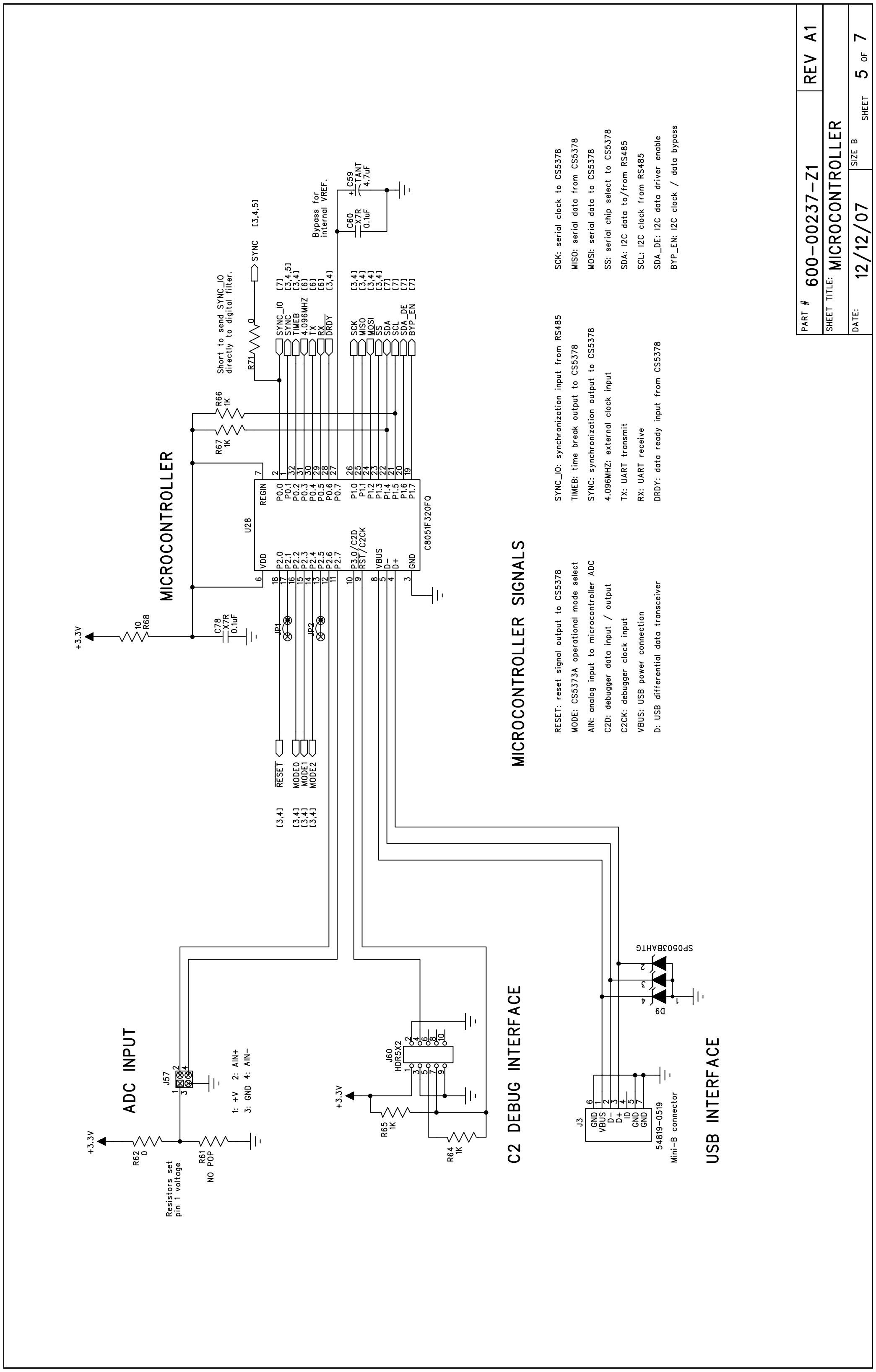
6. SCHEMATICS

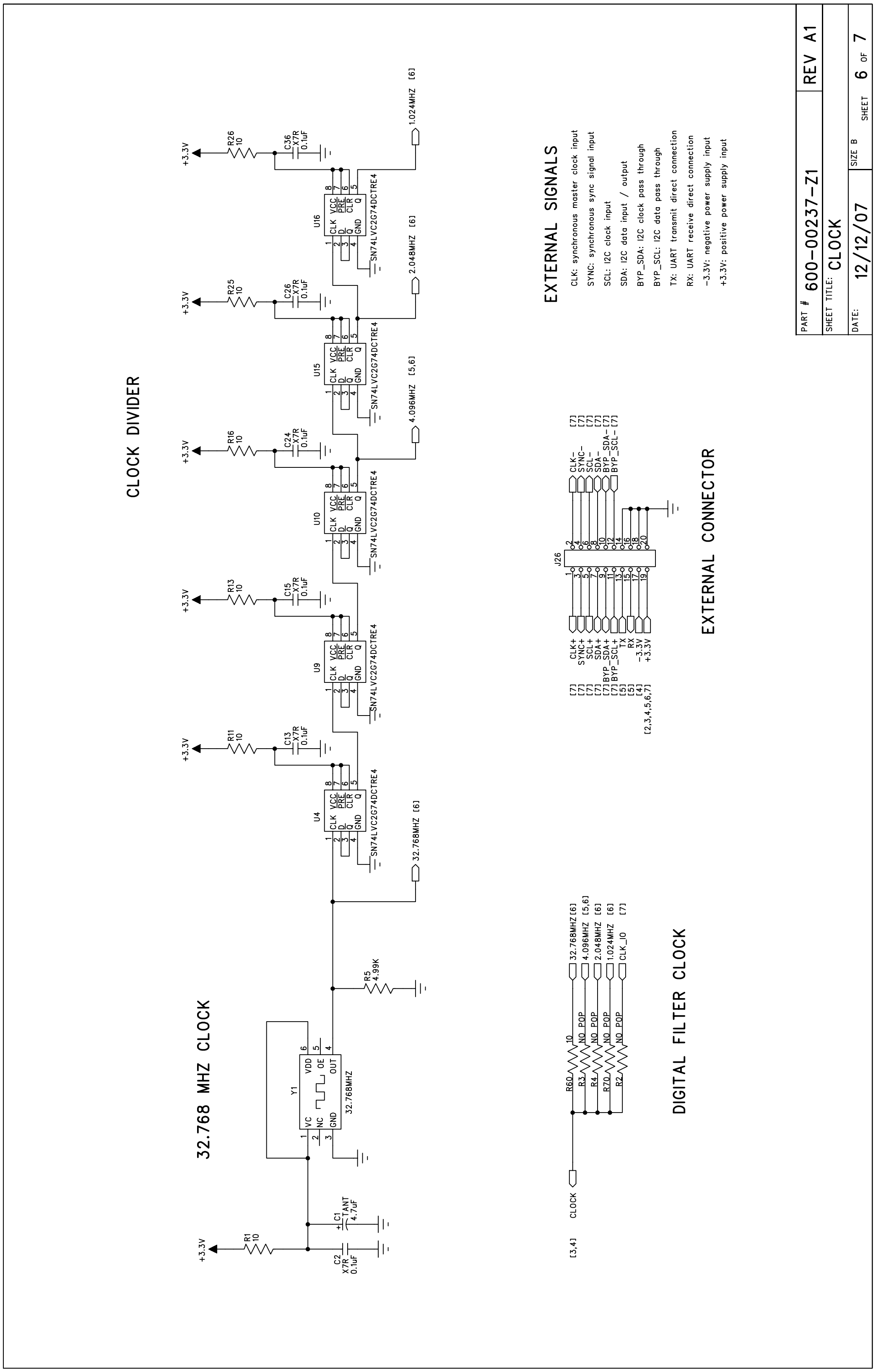


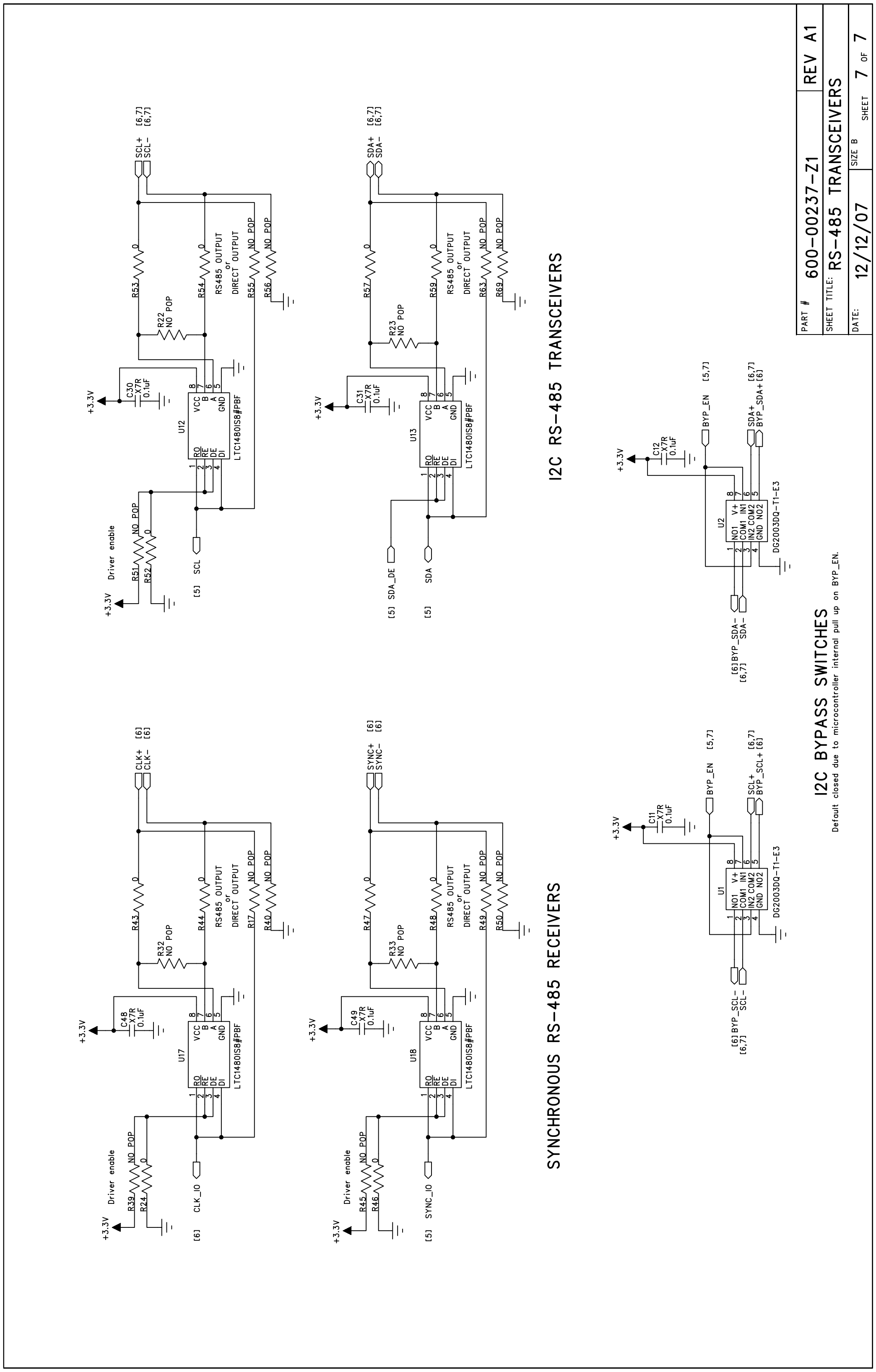

CS3302A signals
INA: differential analog input
INB: differential analog input
OUTR: rough output to modulator
OUTF: fine output to modulator
MUX: input select by CS5378
GAIN: gain select by CS5378
PWDN: power down mode enable
GUARD: guard output from CS3302A
ANALOG INPUTS
INPUT PROTECTION
INPUT RC FILTERS
COMMON MODE BIAS
SENSOR TEST
ELECTRONICS TEST
DIFFERENTIAL AMPLIFIER
ANTI-ALIAS FILTER
OUTPUT TO MODULATOR
ROUTE AS QUAD GROUP
ROUTE AS DIFF PAIR
CS3301A MCLK
CS3302A GUARD
CS3301A GND
CS3302A GUARD
AUXILIARY HARDWARE AND RELATED DOCUMENTS
SCREW-PHILIPS-4-40THR-PH-5/16-PMSSS 440 0031 PH
PCB DWG- 240-00237-Z1
ASSY DWG- 603-00237-Z1
SCH DWG- 600-00237-Z1
PART # 600-00237-Z1
REV A1
SHEET TITLE: ANALOG INPUTS / AMPLIFIER
DATE: 12/12/07
SIZE B
SHEET 2 OF 7


CS5378 SIGNALS
MUX: amplifier mux control
MODE: DAC mode control
GAIN: amplifier gain / DAC attenuation
PLL: clock mode select (reset)
TBSDATA: test DAC data output
MCLK: analog clock output
MSYNC: analog syncronization output
MDATA: modulator data input
MFLAG: modulator error flag input
SS: serial configuration chip select
MOSI: serial data input
MISO: serial data output
SCK: serial clock
DRDY: data ready output
TIMEB: time break input
SYNC: synchronization input
RESET: reset input
CLOCK: clock input
CS5373A SIGNALS
CAP: anti-alias capacitor
BUF: buffered analog output
OUT: precision analog output
VREF: voltage reference input
INR: modulator rough input
INF: modulator fine input
MODE: operational mode select
ATT: attenuator range select
TDATA: DAC data input
MCLK: analog clock input
MSYNC: analog sync input
MDATA: modulator data output
MFLAG: modulator error flag output
DIGITAL FILTER + PLL
MODULATOR + TEST DAC
VOLTAGE REFERENCE
PLL[2..0] DIGITAL FILTER CLK SELECT
NO POP DEFAULTS HIGH (1) AT RESET
10K OHM DEFAULTS LOW (0) AT RESET
111: 32.768 MHz clock input
110: 1.024 MHz clock input
101: 2.048 MHz clock input
100: 4.096 MHz clock input
011: 32.768 MHz clock input
010: 1.024 MHz manchester
001: 2.048 MHz manchester
000: 4.096 MHz manchester
ROUTE AS DIFF PAIRS
ROUTE AS QUAD GROUP
ROUTE AS DIFF PAIR TO VREF INPUTS
U22 CS5378-ISZ
U20 CS5373A-ISZ
U14 LT1019AIS8-2.5#PBF
PART # 600-00237-Z1
REV A1
SHEET TITLE: MODULATOR / DAC / FILTER
DATE: 12/12/07
SIZE B
SHEET 3 OF 7


ACQUISITION / CONTROL INTERFACE - TOP SIDE
ACQUISITION / CONTROL INTERFACE - BOTTOM SIDE
POSITIVE ANALOG VOLTAGE REGULATOR
NEGATIVE ANALOG VOLTAGE REGULATOR
J6 HDR08X2-SM
J5 HDR08X2-SM
J1 HDR08X2-SM
J2 HDR08X2-SM
SS
MOSI
MISO
SCK
DRDY
TIMEB
SYNC
RESET
MODE0
MODE1
MODE2
CLOCK
+3.3V
-3.3V
U3 LT1962EMS8-2.5#PBF
U5 LT1964ES5-BYP#PBF
+2.5VA
-2.5VA
C51 TANT 68uF
C14 X7R 0.01uF
C3 X7R 0.01uF
C5 TANT 68uF
Z1 5.0V
C53 TANT 68uF
D1 BAT54
R7 10K
R6 9.53K
C6 X7R 0.01uF
C7 X7R 0.01uF
C4 TANT 68uF
Z2 5.0V
PART # 600-00237-Z1
REV A1
SHEET TITLE: ANALOG POWER
DATE: 12/12/07
SIZE B
SHEET 4 OF 7


MICROCONTROLLER
U28
C8051F320FQ
Short to send SYNC_IO directly to digital filter.
Bypass for internal VREF.
MICROCONTROLLER SIGNALS
RESET: reset signal output to CS5378
MODE: CS5373A operational mode select
AIN: analog input to microcontroller ADC
C2D: debugger data input / output
C2CK: debugger clock input
VBUS: USB power connection
D: USB differential data transceiver
SYNC_IO: synchronization input from RS485
TIMEB: time break output to CS5378
SYNC: synchronization output to CS5378
4.096MHZ: external clock input
TX: UART transmit
RX: UART receive
DRDY: data ready input from CS5378
SCK: serial clock to CS5378
MISO: serial data from CS5378
MOSI: serial data to CS5378
SS: serial chip select to CS5378
SDA: I2C data to/from RS485
SCL: I2C clock from RS485
SDA_DE: I2C data driver enable
BYP_EN: I2C clock / data bypass
ADC INPUT
Resistors set pin 1 voltage
1: +V 2: AIN+
3: GND 4: AIN-
C2 DEBUG INTERFACE
USB INTERFACE
54819-0519
Mini-B connector
SP0503BAHTG
PART # 600-00237-Z1
REV A1
SHEET TITLE: MICROCONTROLLER
DATE: 12/12/07
SIZE B
SHEET 5 OF 7


CLOCK DIVIDER
32.768 MHZ CLOCK
EXTERNAL SIGNALS
CLK: synchronous master clock input
SYNC: synchronous sync signal input
SCL: I2C clock input
SDA: I2C data input / output
BYP_SDA: I2C clock pass through
BYP_SCL: I2C data pass through
TX: UART transmit direct connection
RX: UART receive direct connection
-3.3V: negative power supply input
+3.3V: positive power supply input
EXTERNAL CONNECTOR
DIGITAL FILTER CLOCK
SN74LVC2G74DCTRE4
1.024MHZ [6]
2.048MHZ [6]
4.096MHZ [5,6]
32.768MHZ [6]
PART # 600-00237-Z1
REV A1
SHEET TITLE: CLOCK
DATE: 12/12/07
SIZE B
SHEET 6 OF 7


I2C RS-485 TRANSCEIVERS
SYNCHRONOUS RS-485 RECEIVERS
I2C BYPASS SWITCHES
Default closed due to microcontroller internal pull up on BYP_EN.
PART # 600-00237-Z1
REV A1
SHEET TITLE: RS-485 TRANSCEIVERS
DATE: 12/12/07
SIZE B
SHEET 7 OF 7