VINCULUM

BINDING USB TECHNOLOGIES

Future Technology Devices International Ltd.

V2-EVAL

Vinculum II Evaluation Board

Datasheet

Document Reference No.: FT_000247

Version 1.0

Issue Date: 2010-04-15

Future Technology Devices International Ltd (FTDI)

Unit 1, 2 Seaward Place, Centurion Business Park, Glasgow, G41 1HH, United Kingdom

Tel.: +44 (0) 141 429 2777 Fax: + 44 (0) 141 429 2758

E-Mail (Support): support1@ftdichip.com

Web: http://www.vinculum.com

Table of Contents

1 Introduction

The following document details the features and specifications of the V2-EVAL board. The V2-EVAL is a hardware platform designed to support easy evaluation of FTDI's Vinculum-II (VNC2) series of embedded USB host controller devices.

The V2-Eval kit includes the following hardware items as standard

- 1 x V2-Eval base board.
- 1 x 5V/1A mains adapter PSU – UK, US, European and Japanese versions available.
- 1 x USB A/B cable to connect to a host PC in programming / terminal emulation or debugging modes.
- 1 x USB gender changer for USB slave mode applications.

NOTE:

The V2-EVAL kit requires a VNC2 based daughterboard module to be installed into the V2-EVAL base board socket site, in order to enable development with the kit.

Daughterboard modules are sold separately, with 3 versions available for 32-pin, 48-pin and 64-pin package devices. Daughterboard modules can be purchased from FTDI or via our website http://www.ftdichip.com.

Before you proceed:
Please check that all the contents of the package are not damaged.

Ensure that your kit includes a proper version of the power supply, depending on the region where you live. Eval application software and project examples can be downloaded from: http://www.ftdichip.com

1.1 Handling the board

Static discharge precaution – Without proper anti-static handling the board can be damaged. Therefore, take anti-static precautions while handling the board.

1.2 Environmental requirements

The V2-Eval Board must be stored between -40°C and 80°C. The recommended operating temperature is between 0°C and 55°C

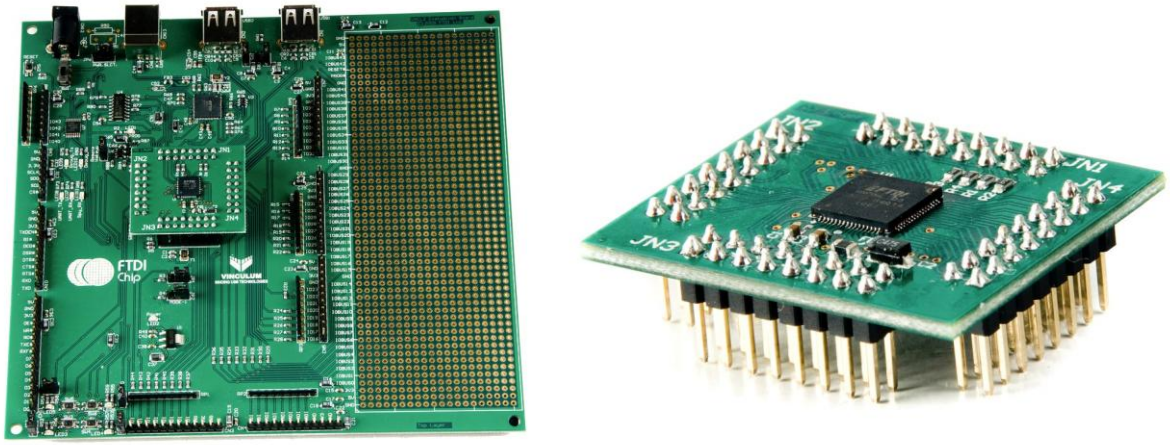


Figure 1.1 - V2-EVAL Motherboard(left) with Daughterboard Module(right)

1.3 Part Numbers

Part Number	Description
V2-EVAL	V2-EVAL kit with base board, power supply and cables.
V2-EVAL-EXT32	VNC2 daughterboard module with 32-pin QFN VNC2 device for use with V2-EVAL.
V2-EVAL-EXT48	VNC2 daughterboard module with 48-pin QFN VNC2 device for use with V2-EVAL.
V2-EVAL-EXT64	VNC2 daughterboard module with 64-pin QFN VNC2 device for use with V2-EVAL.

Table 1.0 Part Numbers.

1.4 References

The document contains references to the following websites and documents. Links to most documents are available from the FTDI website, http://www.ftdichip.com.

Document Name	Description
1. FT_000138	Vinculum-II Embedded Dual USB Host Controller IC Data Sheet.
2. FT_000060	FT4232H Data Sheet.
3. AN_137	Vinculum-II IO Cell Description.
4. AN_138	Vinculum-II Debug Interface Description.
5. AN_139	Vinculum-II IO Mux Explained.
6. AN_140	Vinculum-II PWM Example.
7. USB 2.0	Universal Serial Bus Specification Revision 2.0 USB Implementers Forum http://www.usb.org.

Table 1.1 Document References.

1.5 Acronyms and Abbreviations

Terms	Description
FIFO	First In First Out.
GPIO	General Purpose Input Output.
I/O	Input / Output.
MISO	Master In Slave Out.
MOSI	Master Out Slave In.
SPI	Serial Peripheral Interface.
UART	Universal Asynchronous Receiver/Transmitter.
USB	Universal Serial Bus.
VNC2	Vinculum-II.

Table 1.2 Acronyms and Abbreviations

2 Board Description

V2-Eval Board is intended for use as a hardware platform to enable easy evaluation of FTDI's Vinculum-II VNC2 series of embedded USB Host / Slave controllers. The V2-Eval Board includes all the necessary components required by a user to begin developing USB Host / Slave system applications based on the VNC2 device.

2.1 V2-EVAL Board Features

- VNC2 – Embedded USB Host / Slave chip accessible via daughterboard.
- Selection of VNC2 daughterboards to support 32-pin, 48-pin and 64-pin QFN packages.
- Two USB type A connectors for connecting to USB slave peripherals.
- VNC2 IO port connectors grouped by port name/or function.
- FT42232H –USB to quad channel UART device for VNC2 programming & debug functions.
- One USB type B connector for connection to PC host via FT4232H.
- 4 User-programmable LEDs.
- 4 User-programmable push button switches.

2.2 Specifications

- Board supply voltage: 4.75V … 5.25V.
- Board supply current: 60mA (with no USB devices on USB1 or USB2 port).
- IO connectors power output: 5V/150mA, 3.3V/150mA.
- Base board dimensions: 167mm x 156mm x 1.5mm (L x W x H).
- VNC2 daughterboard dimensions: 37.9mm x 32.48mm x 10.0mm (L x W x H).

3 V2-Eval Board Components and Interfaces

This chapter describes the operational and connectivity information for the V2-Eval board major components and interfaces.

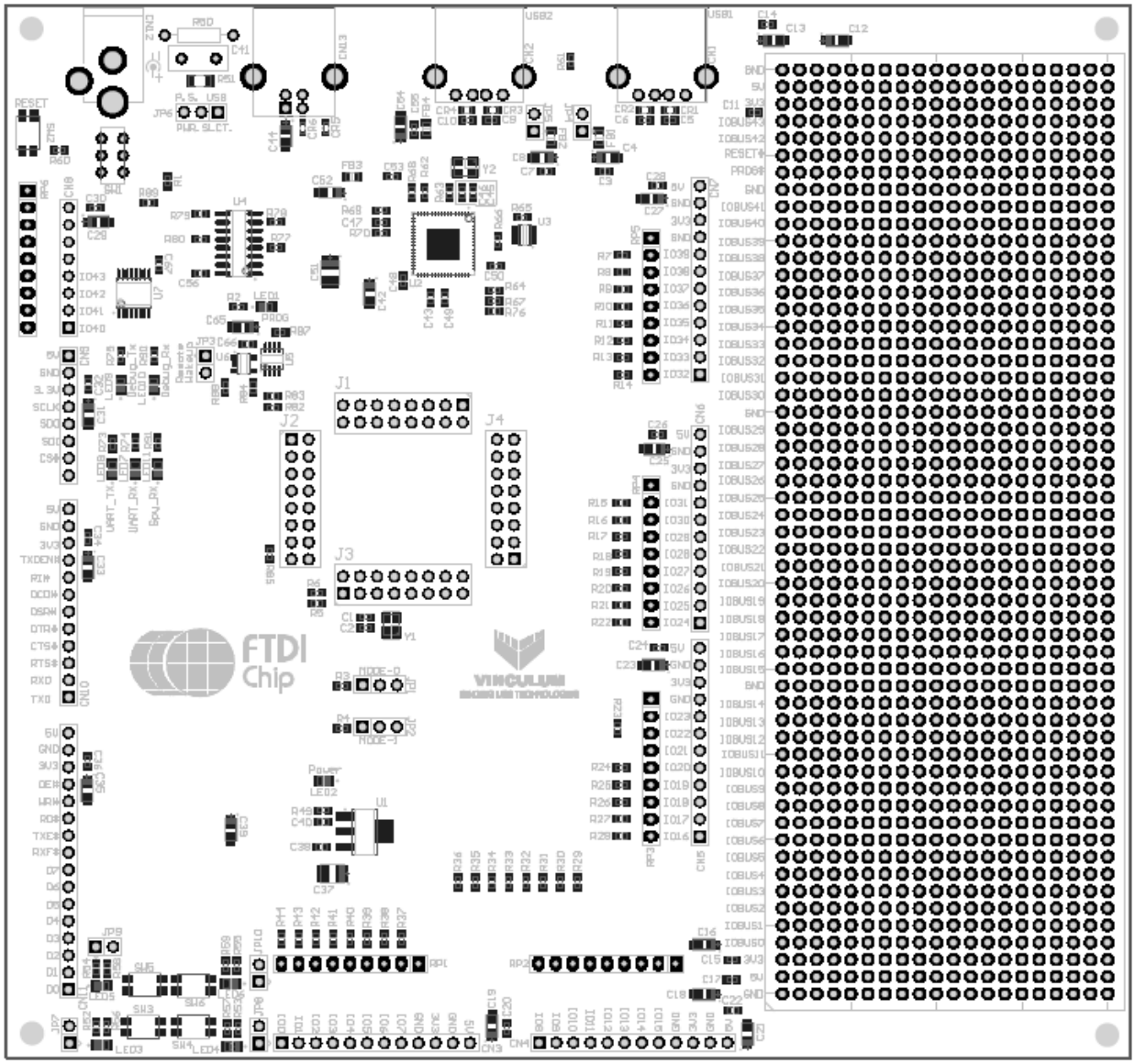


Figure 3.1 V2-EVAL Board Layout

3.1 Block Diagram

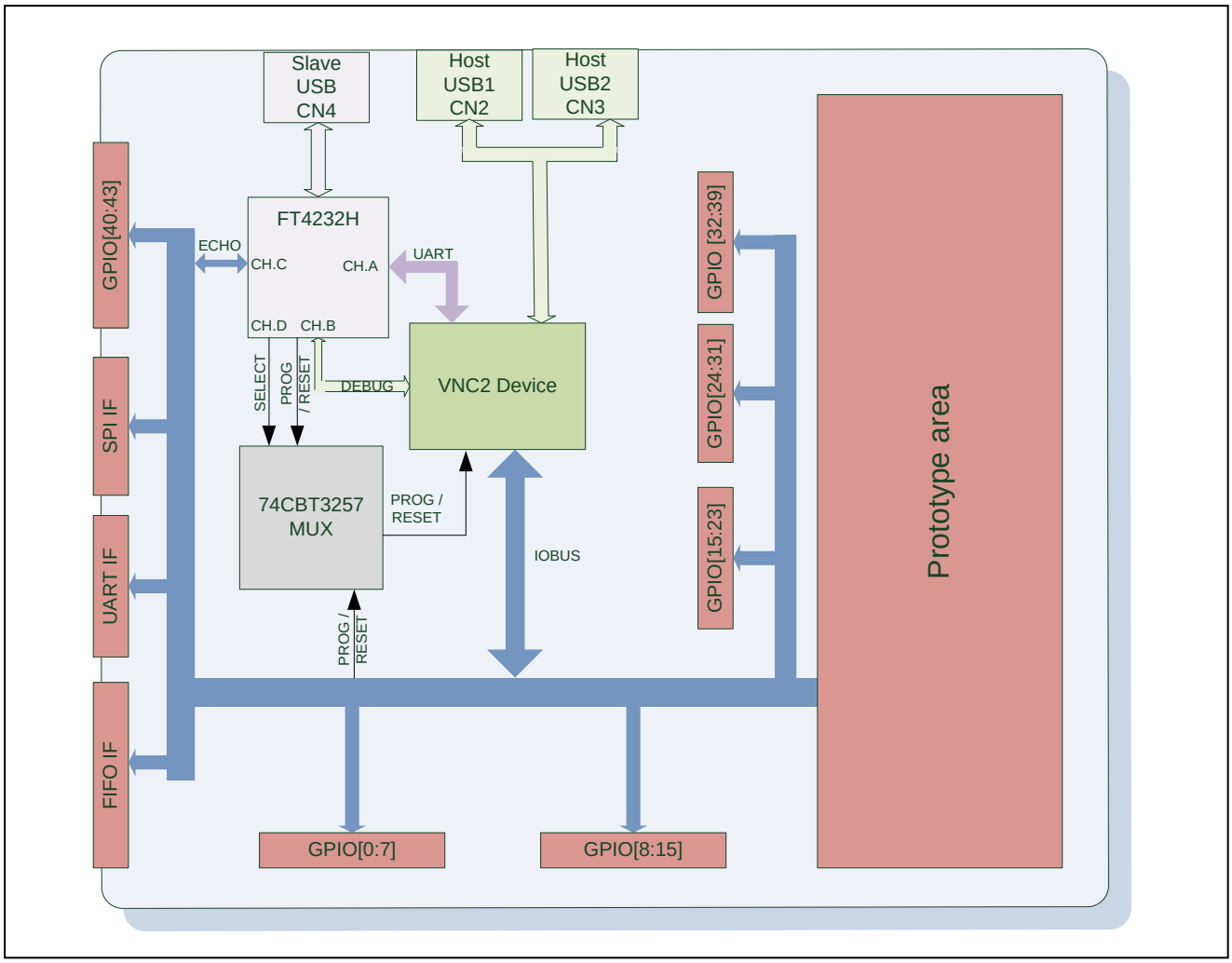


Figure 3.2 V2-EVAL Board Block Diagram.

3.1.1 Components.

Component	Board designator	Description
USB-UART bridge	U2	FT4232H USB ⇔ Quad UART/FIFO device.
Configuration memory	U3	9356 Serial SPI EEPROM for FT4232H configuration data.
IO multiplexer	U4	74CBT3257 4-bit, 1to2, FET Multiplexer/Demultiplexer.
3.3V regulator	U1	AIC1735-33 Ultra low dropout 3.3V voltage regulator.
12MHz crystal	Y2	12MHz crystal for FT4232H.
Single 5V DC power supply	CN12	Board adapter for included 5V DC power supply.
Power switch	SW1	Power On/Off switch.
Power source select	JP6	Power source selection jumper.
Reset button	SW2	Push-button switch for manual reset of VNC2 device.
Keyboard	SW3-SW6	Four user push-button switches.
User LEDs	LED3-LED6	Four green user LEDs.
PROG LED	LED1	Red LED.
Power LED	LED2	Green LED.
UART RX LED	LED7	Green LED.
UART TX LED	LED8	Red LED.
Debug TX	LED9	Red LED.
Debug RX	LED10	Green LED.
SPI_RX	LED11	Green LED.
LEDs enable jumpers	JP7-JP10	Enable/disable user-defined LEDs.
GPIO I/O Jumpers	JP1, JP2	GPIO I/O jumpers .
REMOTE WAKEUP	JP3	VNC2 remote wakeup jumper.
VBUS jumpers	JP4, JP5	USB1, USB2 power bus enable jumpers.

Table 3.1 V2-Eval Board Components.

3.1.2 Interfaces.

Component	Board designator	Description
USB1, USB2 (1)	CN1, CN2	VNC2 USB host ports 1&2.
USB Type B	CN13	FT4232H USB Slave connection.
VNC2 Socket	J1 -J4	Daughterboard connectors for VNC2 Daughterboard.
SPI (2)	CN9	VNC2 SPI interface pins.
UART (2)	CN10	VNC2 UART interface pins.
FIFO (2)	CN11	VNC2 FIFO interface pins.
IOBUS[7..0] (2)	CN3	VNC2 IOBUS [7:0] port pins.
IOBUS[8..15] (2)	CN4	VNC2 IOBUS [8:15] port pins.
IOBUS[16..23] (2)	CN5	VNC2 IOBUS [16:23] port pins.
IOBUS[24..31] (2)	CN6	VNC2 IOBUS [24:31] port pins.
IOBUS[32..39] (2)	CN7	VNC2 IOBUS [32:39] port pins.
IOBUS[40..43] (2)	CN8	VNC2 IOBUS [40:43] port pins.
Prototyping area (2)	P1	All of VNC2 IO ports and PROG#, RESET# pins are brought on to this area.

Notes

(1) Gender changer required when ports are configured as slave ports by VNC2 firmware, to enable connection to a USB host port.

(2) Those pins are shared between different areas and connectors on the board. You can use only one device at time connected to those pins.

Table 3.2 V2-Eval Board Interfaces.

4 Initial Board Set-up & Test

4.1 Installing VNC2 Daughterboard

Prior to first powering the board, users must ensure that the daughterboard module hosting the VNC2 chip is correctly installed on to the main V2-Eval board. The V2-Eval board has 4 socket connectors, J1-J4, onto which the VNC2 daughterboard module is installed.

On the VNC2 daughterboard module, connector JN1 connects to corresponding socket J1, JN2 connects to socket J2, JN3 connects to socket J3 and JN4 connects to J4 on the V2-Eval board.

Warning!

Please check that the VNC2 daughterboard module is correctly installed onto the V2-Eval board prior to power-up. Incorrect installation can cause the VNC2 to not function.

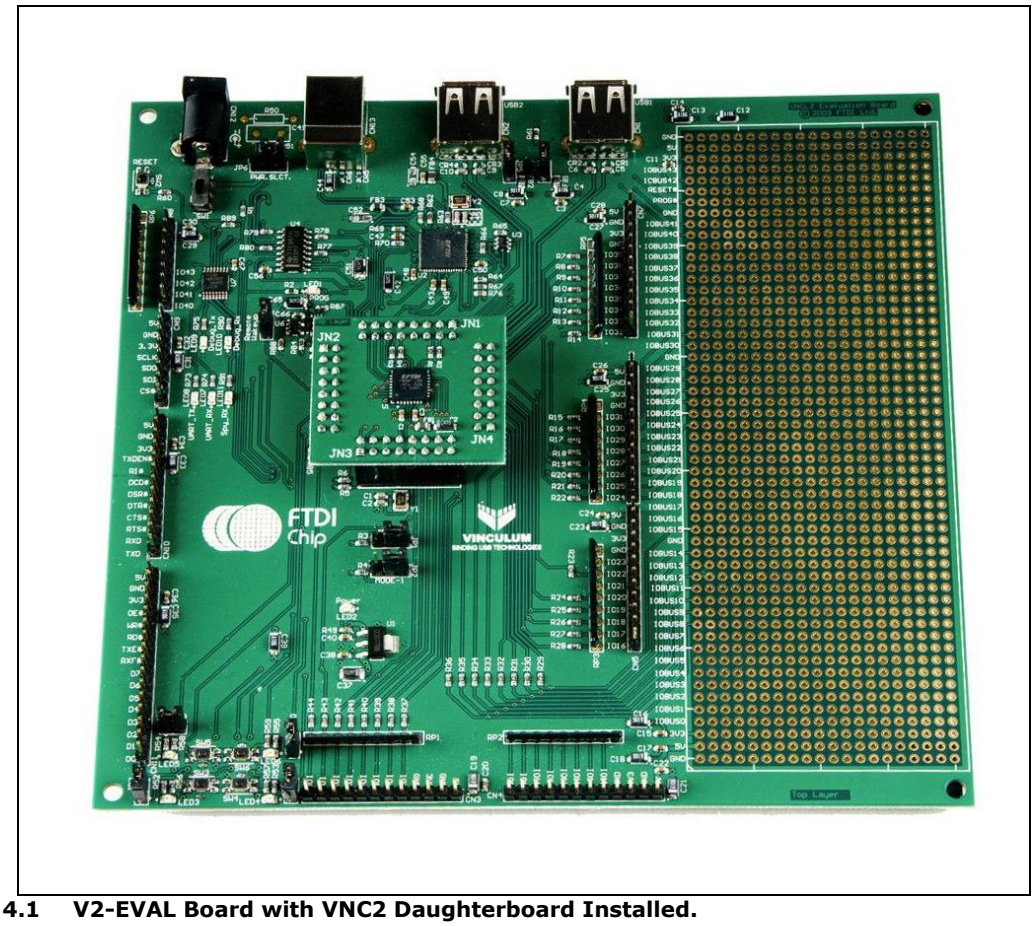


Figure 4.1 V2-EVAL Board with VNC2 Daughterboard Installed.

4.2 Testing the board.

Ensure that the Power Select jumper JP6 is in 'P.S.' position (pins 2 & 3 shorted), to enable the board to be powered from the external power adapter.

Connect the 5V DC/1A power supply included in V2-Eval Kit to the external input power adapter connector (CN12), connect USB A/B cable to USB B connector (CN13) on V2-Eval Board and to a free USB port on host PC. Switch SW1 to the ON position (towards board edge). LED2 – POWER should now be on.

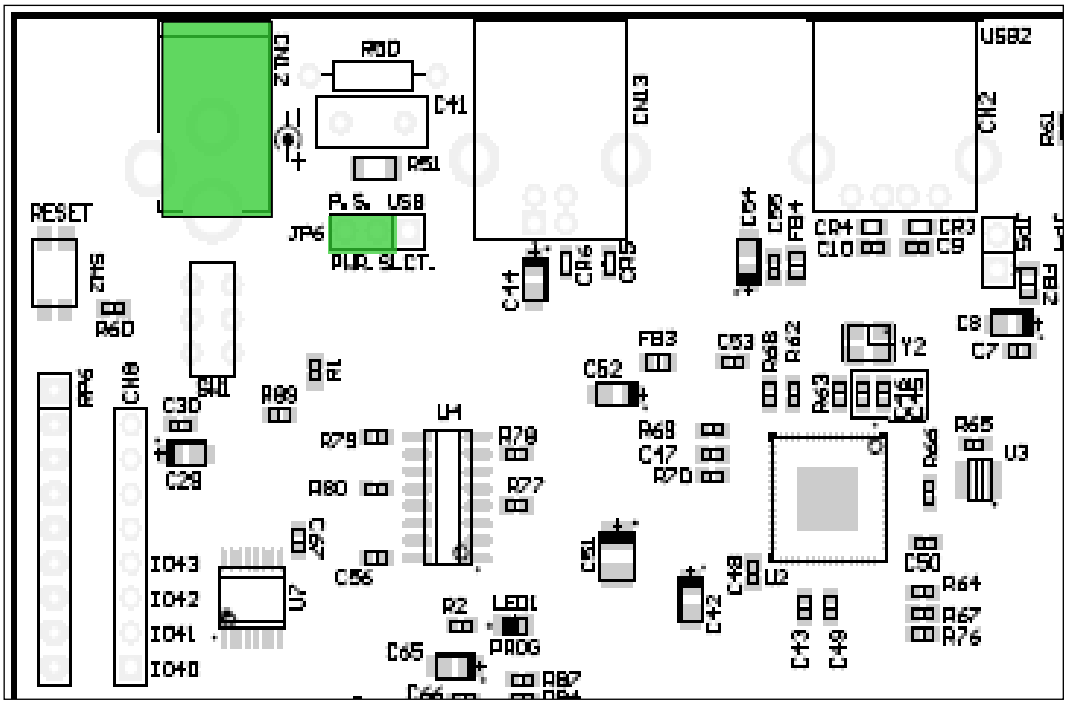


Figure 4.2 Power connector with Jumper JP6.

The PCB circuitry will draw power either directly from the board 5V supply or from a 3.3V regulator that is powered by this 5V supply. This includes the VNC2 daughterboard module that is installed on the board. Upon power up, the power LED (LED2) will illuminate.

5 Detailed Description of Board Components.

5.1 Power Select Jumper JP6.

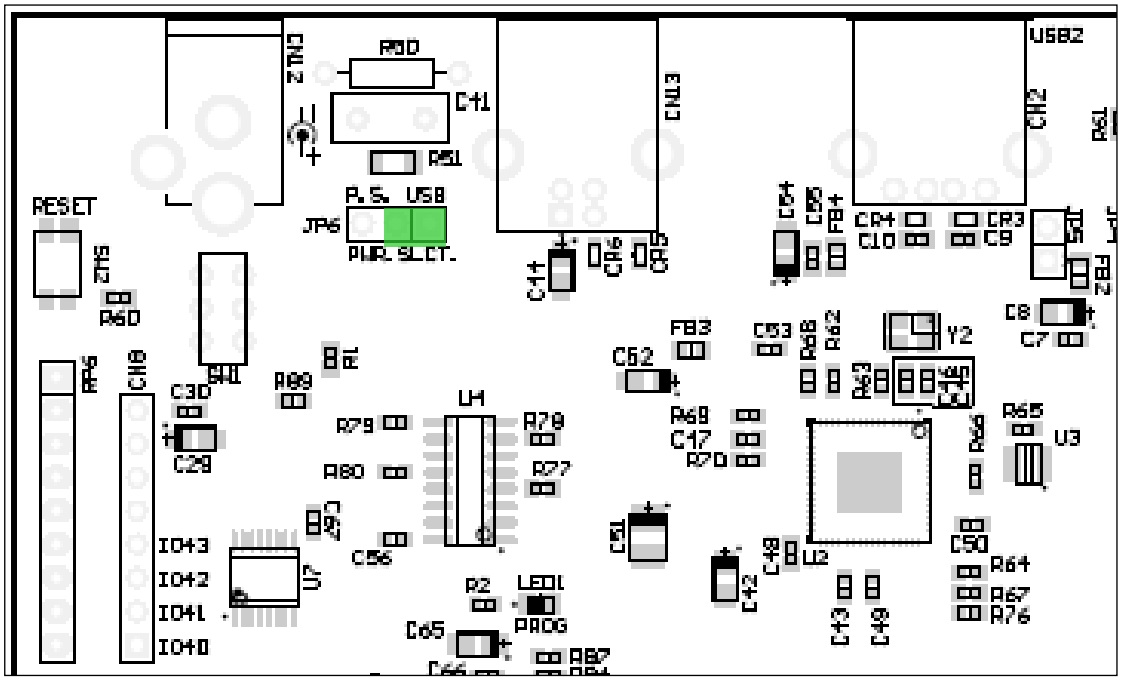


Figure 5.1 Power Select Jumper Configuration for USB Power.

V2-Eval Board can draw its power either from the external 5V/1A DC Power Supply or from the USB interface when connected to a USB host via the B type connector (CN13). To enable USB power supply feature, switch the jumper JP6 to USB position, pins 1&2 shorted (pin 1 has a rectangle shaped pad on the bottom side of the board).

Warning!

Please remember that every device connected to the PC through USB port can draw NO MORE than 500mA from the USB host PC 5V power bus.

5.2 GPIO BUS Connectors

The V2-EVAL board features a set of 6 connectors providing access to GPIO capable pins on the VNC2 device. The GPIO pins are distributed across 6 connectors. The configuration of each connector is outlined in subsequent sections. Further each connector has a 5V and 3.3V power and GND pins.

5.2.1 GPIO [0:7] Connector CN3

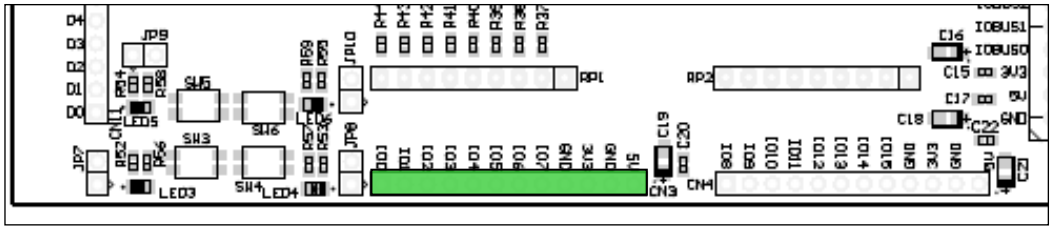


Figure 5.2 GPIO[0:7] Connector CN3.

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
GPIO0 (3)	1	11	11	11	IO	GPIO data bit 0
GPIO1 (3)	2	12	12	12	IO	GPIO data bit 1
GPIO2 (3)	3	14	13	13	IO	GPIO data bit 2
GPIO3 (3)	4	15	14	14	IO	GPIO port, data bit 3
GPIO4 (3)	5	-	-	15	IO	GPIO port, data bit 4
GPIO5 (3)	6	-	-	16	IO	GPIO port, data bit 5
GPIO6 (3)	7	-	-	17	IO	GPIO port, data bit 6
GPIO7 (3)	8	-	-	18	IO	GPIO port, data bit 7
GND	9	-	-	-	-	Ground pin
3.3V(4)	10	-	-	-	-	3.3V power rail.
GND	11	-	-	-	-	Ground pin
5V(5)	12	-	-	-	-	5V power rail.

Notes:

(3) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels.
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(4) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(5) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.1 GPIO port connector CN3.

5.2.2 GPIO [8:15] Connector CN4

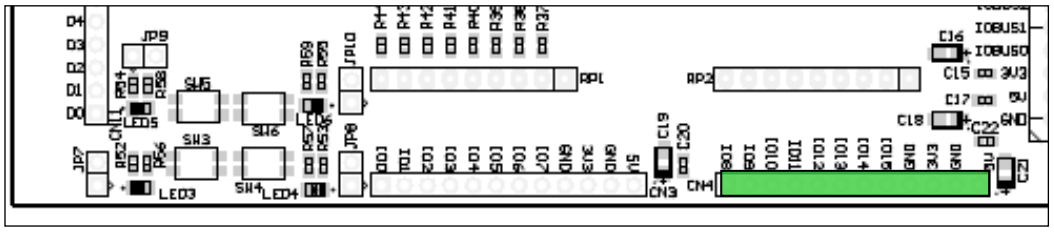


Figure 5.3 GPIO[8:15] Connector CN4.

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
GPIO8 (6)	1	-	-	19	IO	GPIO port, data bit 8
GPIO9 (6)	2	-	-	20	IO	GPIO port, data bit 9
GPIO10 (6)	3	-	-	22	IO	GPIO port, data bit 10
GPIO11 (6)	4	-	-	23	IO	GPIO port, data bit11
GPIO12 (6)	5	-	-	24	IO	GPIO port, data bit 12
GPIO13 (6)	6	-	-	25	IO	GPIO port, data bit 13
GPIO14 (6)	7	-	-	26	IO	GPIO port, data bit 14
GPIO15 (6)	8	-	-	27	IO	GPIO port, data bit 15
GND	9	-	-	-	-	Ground pin
3.3V(7)	10	-	-	-	-	3.3V power rail.
GND	11	-	-	-	-	Ground pin
5V(8)	12	-	-	-	-	5V power rail.

Notes:

(6) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels.
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(7) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(8) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.2 GPIO[8:15] connector CN4.

5.2.3 GPIO [16:23] Connector CN5

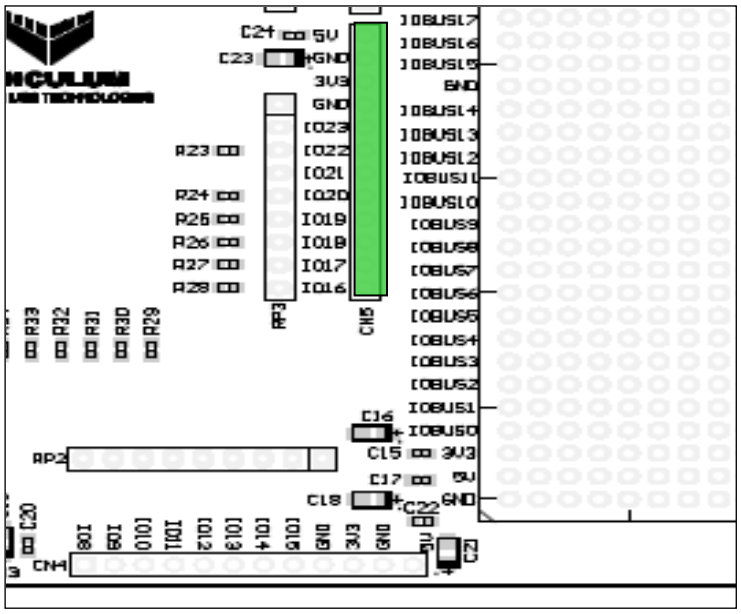


Figure 5.4 GPIO[16:23] Connector CN5.

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
GPIO16 (9)	1	-	-	27	IO	GPIO port, data bit 16
GPIO17 (9)	2	-	46	28	IO	GPIO port, data bit 17
GPIO18 (9)	3	-	45	29	IO	GPIO port, data bit 18
GPIO19 (9)	4	-	48	31	IO	GPIO port, data bit19
GPIO20 (9)	5	23	31	32	IO	GPIO port, data bit 20
GPIO21 (9)	6	24(10)	32(10)	39	IO	GPIO port, data bit 21
GPIO22 (9)	7	25	33	40	IO	GPIO port, data bit 22
GPIO23 (9)	8	26(10)	34 (10)	41	IO	GPIO port, data bit 23
GND	9	-	-	-	-	Ground pin
3.3V(11)	10	-	-	-	-	3.3V power rail.
GND	11	-	-	-	-	Ground pin
5V(12)	12	-	-	-	-	5V power rail.

Notes:

(9) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels.
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(10) The following pins are only accessible on VNC2 when the onboard multiplexer select input is high. See section 6.4 for details.

(11) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(12) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.3 GPIO port connector CN5.

5.2.4 GPIO [24:31] Connector CN6

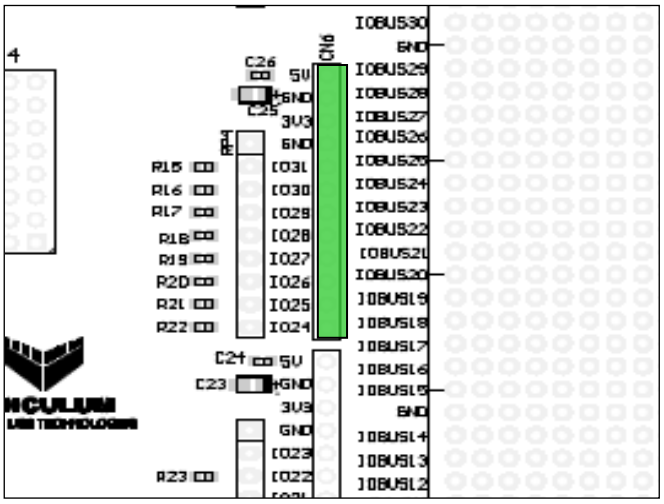


Figure 5.5 GPIO[24:31] Connector CN6.

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
GPIO24 (13)	1	-	35	43	IO	GPIO port, data bit 24
GPIO25 (13)	2	-	36	44	IO	GPIO port, data bit 25
GPIO26 (13)	3	-	37	45	IO	GPIO port, data bit 26
GPIO27 (13)	4	-	38	46	IO	GPIO port, data bit 27
GPIO28 (13)	5	-	41	47	IO	GPIO port, data bit 28
GPIO29 (13)	6	-	42	48	IO	GPIO port, data bit 29
GPIO30 (13)	7	-	43	49	IO	GPIO port, data bit 30
GPIO31 (13)	8	-	44	50	IO	GPIO port, data bit 31
GND	9	-	-	-	-	Ground pin
3.3V(14)	10		-	-	-	3.3V power rail.
GND	11		-	-	-	Ground pin
5V(15)	12		-	-	-	5V power rail.

Notes:

(13) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels. The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(14) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(15) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB bus.

Table 5.4 GPIO port connector CN6.

5.2.5 GPIO [32:39] Connector CN7

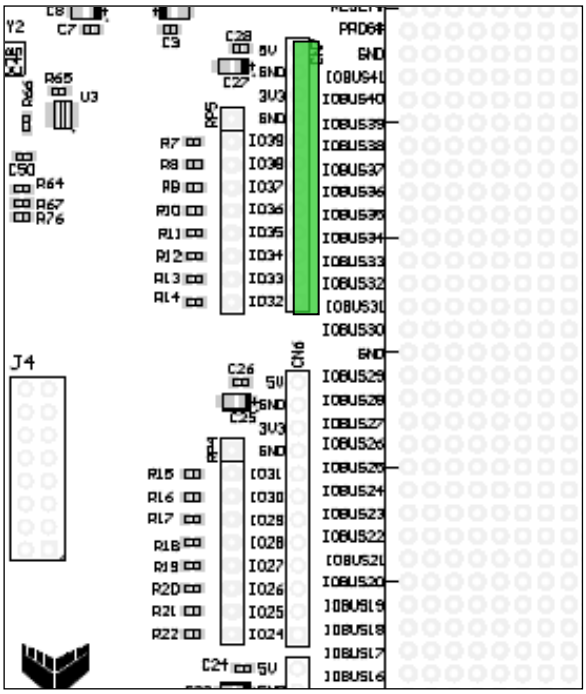


Figure 5.6 GPIO[32:39] Connector CN7.

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
GPIO32 (16)	1	29	15	51	IO	GPIO port, data bit 32
GPIO33 (16)	2	30	16	52	IO	GPIO port, data bit 33
GPIO34 (16)	3	31	18	55	IO	GPIO port, data bit 34
GPIO35 (16)	4	32	19	56	IO	GPIO port, data bit 35
GPIO36 (16)	5	-	-	57	IO	GPIO port, data bit 36
GPIO37 (16)	6	-	-	58	IO	GPIO port, data bit 37
GPIO38 (16)	7	-	-	59	IO	GPIO port, data bit 38
GPIO39 (16)	8	-	-	60	IO	GPIO port, data bit 39
GND	9	-	-	-	-	Ground pin
3.3V(17)	10	-	-	-	-	3.3V power rail.
GND	11	-	-	-	-	Ground pin
5V(18)	12	-	-	-	-	5V power rail.

Notes:

(16) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels. The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(17) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(18) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

Table 5.5 GPIO port connector CN7.

5.2.6 GPIO [40:43] Connector CN8

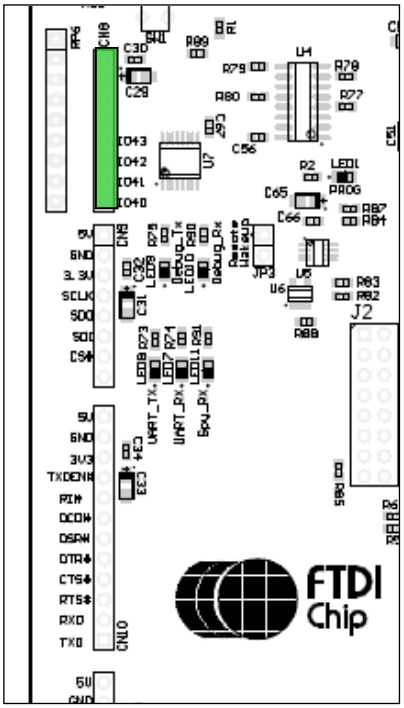


Figure 5.7 GPIO[32:39] Connector CN8.

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
GPIO40 (19)	1	-	20	61	IO	GPIO port, data bit 40
GPIO41 (19)	2	-	21	62	IO	GPIO port, data bit 41
GPIO42 (19)	3	-	22	63	IO	GPIO port, data bit 42
GPIO43 (19)	4	-	23	64	IO	GPIO port, data bit 43
GND	5	-	-	-	-	Ground pin
3.3V(20)	6	-	-	-	-	3.3V power rail.
GND	7	-	-	-	-	Ground pin
5V(21)	8	-	-	-	-	5V power rail.

Notes:

(19) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels. The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(20) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(21) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.6 GPIO port connector CN8.

5.3 SPI Connector C9

Table 5.7 details connector pinout for the SPI connector C9. A full description of each signal is available in the VNC2 data sheet.

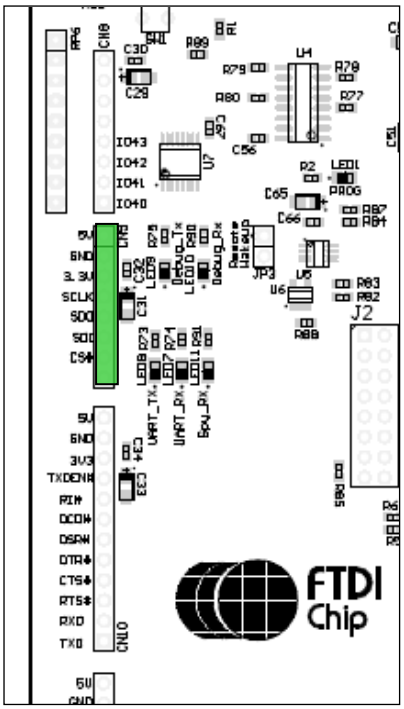


Figure 5.8 SPI Connector CN9.

Signal name	Connector pin	VCN2 Pin No		IO type	Description
		48-PIN	64-PIN		
5V(22)	1	-	-	-	5V power rail.
GND	2	-	-	-	Ground pin
3.3V(23)	3	-	-	-	3.3V power rail.
SCLK (24)	4	20	61	Input	SPI CLK Input
SDO (24)	5	21	62	Output	SPI Master out slave in
SDI(24)	6	22	63	Input	SDI Master in slave out
CS# (24)	7	23	64	Output	Active low slave chip select 0 from master to slave 0
GND	8	-	-	-	Ground pin

Notes:

(22) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(23) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(24) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels..
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

Table 5.7 SPI Port Connector CN9.

5.4 UART Interface Connector C10

Table 5.8 details connector pinout for the UART connector C10. A full description of each signal is available in the VNC2 data sheet.

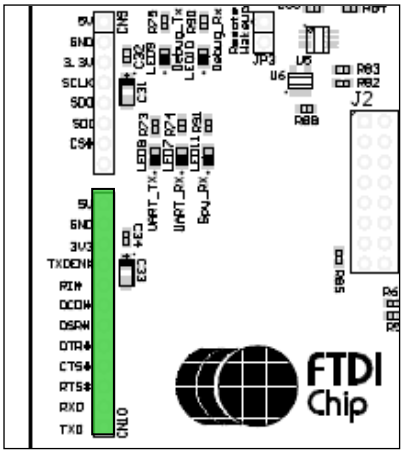


Figure 5.9 UART Connector CN10.

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
TXD (25)	1	23	31	39	Output	Transmit data
RXD (25)	2	24(26)	32(26)	40	Input	Receive data
RTS# (25)	3	25	33	41	Output	Request to Send Control Output / Handshake signal.
CTS# (25)	4	26(26)	34(26)	42	Input	Clear to Send Input / Handshake signal.
DTR# (25)	5		35	43	Output	Data Terminal Ready Output / Handshake signal.
DSR# (25)	6		36	44	Input	Data Set Ready Input / Handshake signal.
DCD# (25)	7		37	45	Input	Data Carrier Detect Control Input
RI# (25)	8		38	46	Input	Ring Indicator Control Input
TXDEN#(25)	9		-	47	Output	Transmit Data Enable
3.3V(27)	10		-	-	-	3.3V power rail.
GND	11		-	-	-	Ground pin
5V(28)	12		-	-	-	5V power rail.

Notes:

(25) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels..
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(26) The following pins are only accessible on VNC2 when the onboard multiplexer select input is high. See section 6.4 for details.

(27) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

(28) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

Table 5.8 UART Interface Connector CN10.

5.5 FIFO Interface Connector CN11

Table 5.9 details connector pinout for the FIFO connector C11. A full description of each signal is available in the VNC2 data sheet.

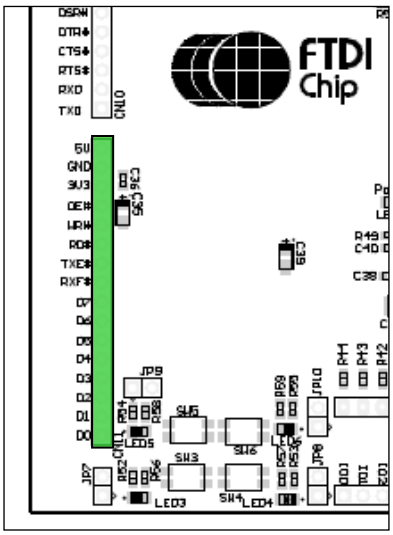


Figure 5.10 FIFO Connector CN11.

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
D0 (29)	1	-	-	15	IO	FIFO data bit 0, bidirectional
D1 (29)	2	-	-	16	IO	FIFO data bit 1, bidirectional
D2 (29)	3	-	-	17	IO	FIFO data bit 2, bidirectional
D3 (29)	4	-	-	18	IO	FIFO data bit 3, bidirectional
D4 (29)	5	-	-	19	IO	FIFO data bit 4, bidirectional
D5 (29)	6	-	-	20	IO	FIFO data bit 5, bidirectional
D6 (29)	7	-	-	22	IO	FIFO data bit 6, bidirectional
D7 (29)	8	-	-	23	IO	FIFO data bit 7, bidirectional
RXF#	9	-	-	24	Output	FIFO receive full output
TXE#	10	-	-	25	Output	FIFO transmitter buffer empty output
RD#	11	-	-	26	Input	FIFO read enable input
WR#	12	-	-	27	Input	FIFO write enable input
OE#	13	-	-	28	Input	FIFO output enable – synchronous FIFO only
3.3V(30)	14	-	-	-	-	3.3V power rail.
GND	15	-	-	-	-	Ground pin
5V(31)	16	-	-	-	-	5V power rail.

Notes:

(29) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels. The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(30) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(31) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.9 FIFO Interface Connector CN11.

5.6 Prototyping area

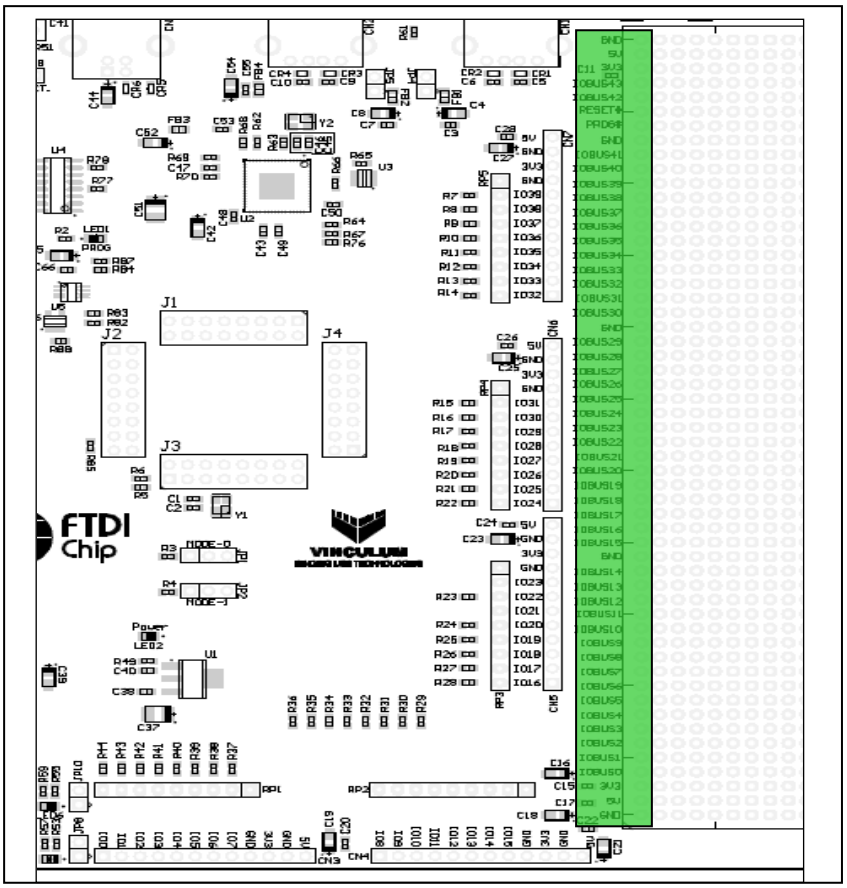


Figure 5.11 Prototyping area P1.

A prototype area consisting of an array of 1100, 0.1-inch pitch holes is provided. The area can be used to create custom circuitry and connect components to the V2-EVAL board. The prototyping area includes connections to the 5V, 3.3 V planes and ground planes. The silk-screen text on the board indicates which holes are connected to which signals. Only the first column is connected to VNC2 IO ports, power and ground planes. All the other holes are not connected to anything on the board.

Signal pins are shared between other IO connectors on the board. For more information refer to the V2-Eval Board schematics.

Connector pin number	Silk Screen Signal Label	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
1	GND	-	-	-	-	Ground pin
2	5V [32]	-	-	-	-	5V power rail. Can be used to power external devices
3	3.3V[33]	-	-	-	-	3.3V power rail. Can be used to power external devices
4	IOBUS0[34]	11	11	11	IO	IOBUS port Data Bit 0. Debug port – default configuration.
5	IOBUS1[34]	12	12	12	IO	IOBUS port Data Bit 1.
6	IOBUS2[34]	14	13	13	IO	IOBUS port Data Bit 2.
7	IOBUS3[34]	15	14	14	IO	IOBUS port Data Bit 3.
8	IOBUS4[34]	-	-	15	IO	IOBUS port Data Bit 4.
9	IOBUS5[34]	-	-	16	IO	IOBUS port Data Bit 5.
10	IOBUS6[34]	-	-	17	IO	IOBUS port Data Bit 6.
11	IOBUS7[34]	-	-	18	IO	IOBUS port Data Bit 7.
12	IOBUS8[34]	-	-	19	IO	IOBUS port Data Bit 8.
13	IOBUS9[34]	-	-	20	IO	IOBUS port Data Bit 9.
14	IOBUS10[34]	-	-	22	IO	IOBUS port Data Bit 10.
15	IOBUS11[34]	-	-	23	IO	IOBUS port Data Bit 11.
16	IOBUS12[34]	-	-	24	IO	IOBUS port Data Bit 12.
17	IOBUS13[34]	-	-	25	IO	IOBUS port Data Bit 13.
18	IOBUS14[34]	-	-	26	IO	IOBUS port Data Bit 14.
19	GND	-	-	-	-	Ground pin
20	IOBUS15[34]	-	-	27	IO	IOBUS port Data Bit 15.
21	IOBUS16[34]	-	-	27	IO	IOBUS port Data Bit 16.
22	IOBUS17[34]	-	46	28	IO	IOBUS port Data Bit 17.
23	IOBUS18[34]	-	45	29	IO	IOBUS port Data Bit 18.
24	IOBUS19[34]	-	48	31	IO	IOBUS port Data Bit 19.
25	IOBUS20[34]	23	31	32	IO	IOBUS port Data Bit 20.
26	IOBUS21[34]	24[35]	32[35]	39	IO	IOBUS port Data Bit 21.
27	IOBUS22[34]	25	33	40	IO	IOBUS port Data Bit 22.
28	IOBUS23[34]	26[35]	34[35]	41	IO	IOBUS port Data Bit 23.
29	IOBUS24[34]	-	35	43	IO	IOBUS port Data Bit 24.
30	IOBUS25[34]	-	36	44	IO	IOBUS port Data Bit 25.
31	IOBUS26[34]	-	37	45	IO	IOBUS port Data Bit 26.
32	IOBUS27[34]	-	38	46	IO	IOBUS port Data Bit 27.
33	IOBUS28[34]	-	41	47	IO	IOBUS port Data Bit 28.
34	IOBUS29[34]	-	42	48	IO	IOBUS port Data Bit 29.
35	GND	-	-	-		
36	IOBUS30[34]	-	43	49	IO	IOBUS port Data Bit 30.
37	IOBUS31[34]	-	44	50	IO	IOBUS port Data Bit 31.
38	IOBUS32[34]	29	15	51	IO	IOBUS port Data Bit 32.
39	IOBUS33[34]	30	16	52	IO	IOBUS port Data Bit 33.
40	IOBUS34[34]	31	18	55	IO	IOBUS port Data Bit 34.
41	IOBUS35[34]	32	19	56	IO	IOBUS port Data Bit 35.

42	IOBUS36(34)	-	-	57	IO	IOBUS port Data Bit 36.
43	IOBUS37(34)	-	-	58	IO	IOBUS port Data Bit 37.
44	IOBUS38(34)	-	-	59	IO	IOBUS port Data Bit 38.
45	IOBUS39(34)	-	-	60	IO	IOBUS port Data Bit 39.
46	IOBUS40(34)	-	20	61	IO	IOBUS port Data Bit 40.
47	IOBUS41(34)	-	21	62	IO	IOBUS port Data Bit 41.
48	GND	-	-	-	-	Ground pin
49	PROG#	9	10	10	I	VNC2 PROG# pin
50	RESET#	10	9	9	I	VNC2 RESET# pin
51	IOBUS42(35)	-	22	63	-	IOBUS port Data Bit 42.
52	IOBUS43(35)	-	23	64	-	IOBUS port Data Bit 43.
53	3.3V(33)	-	-	-	-	3.3V power rail. Can be used to power external devices
54	5V(32)	-	-	-	-	5V power rail. Can be used to power external devices
55	GND	-	-	-	-	Ground pin

Notes:

(32) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

(33) This pin is connected to 3.3V regulator output.

(34) The IOBUS signal labels on the PCB silk screen do directly relate to the IOBUS signal names for the VNC2 device on the daughterboard. See VNC2 pin number for signal mapping on the device.

(35) The following pins are only accessible when the onboard multiplexer select input is high. See section 6.4 for details.

Table 5.10 Prototyping Area Pinout.

5.7 USB1 interface CN1

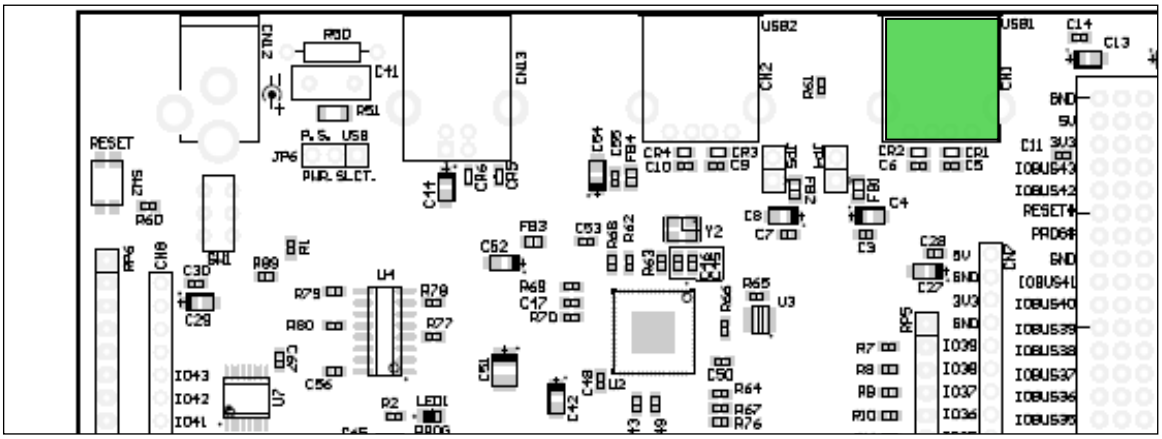


Figure 5.12 USB1 Interface CN1.

VNC2 USB1 transceiver pins are brought on this connector. Depending on the firmware version this port can be configured as host or slave port.

Signal name	Connector pin number	VCN2 pin name	VCN2 pin number			IO type	Description
			32-PIN	48-PIN	64-PIN		
5V (36)	1	-	-			-	5V power rail. Can be used to power external devices
USB1-DM	2	USB1 DM	17	25	33	IO	USB1 transceiver, data line Minus
USB1-DP	3	USB1 DP	18	26	34	IO	USB1 transceiver, data line Plus
GND	4	-	-			-	Ground pin
Shield	5, 6	-	-			-	Connector shield. Connected to ground.

Notes:
(36) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

Table 5.11 USB1 Host/Slave Connector CN1.

5.8 USB2 interface CN2.

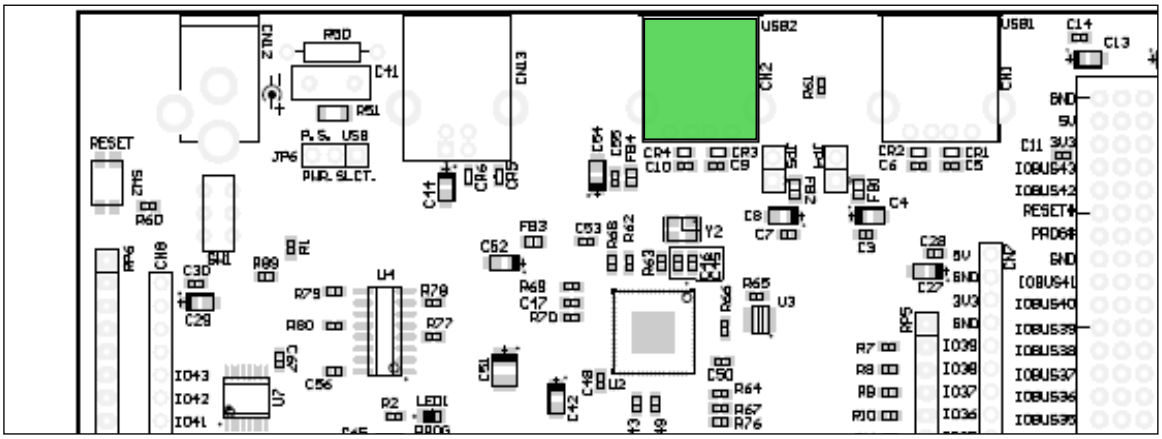


Figure 5.13 USB2 Interface CN2.

VNC2 USB2 transceiver pins are brought on this connector. Depending on the version of the firmware running on the device, the port can be configured as host or slave port.

Signal name	Connector pin number	VCN2 pin name	VCN2 pin number			IO type	Description
			32-PIN	48-PIN	64-PIN		
5V (37)	1	-	-			-	5V power rail. Can be used to power external devices
USB2-DM	2	USB2 DM	20	28	36	IO	USB2 transceiver, data line Minus
USB2-DP	3	USB2 DP	21	29	37	IO	USB2 transceiver, data line Plus
GND	4	-	-			-	Ground pin
Shield	5, 6	-	-			-	Connector shield. Connected to ground.

Notes:
(37) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

Table 5.12 USB2 Host / Slave connector CN2.

5.9 GPIO Jumpers JP1, JP2

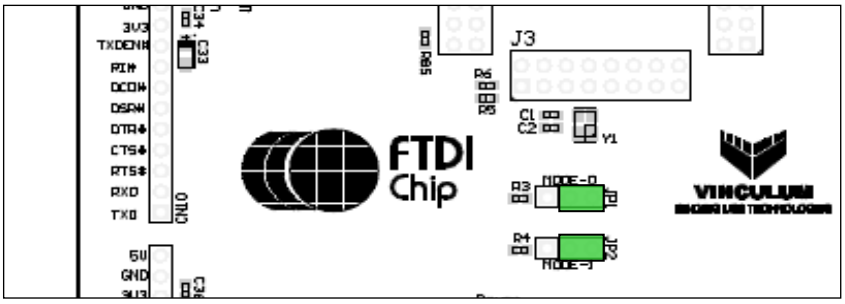


Figure 5.14 GPIO Jumper pins, JP1, JP2.

JP1 and JP2 jumpers are available for use as jumper select inputs to the VNC2.

Jumper	VNC2 Pin Number / Signal Name		VNC2 Signal Name Comments
	48-PIN	64-PIN	
JP1	46 / IOBUS25	29 / IOBUS18	Signal also connected to LED5
JP2	47 / IOBUS26	-	
Notes: (38) The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.			

Table 5.13 GPIO jumpers JP1, JP2.

5.10 User LEDs. LED3 – LED6.

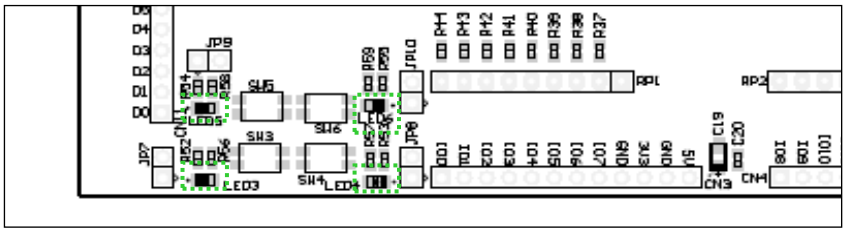


Figure 5.15 User LEDs.

Four LEDs is provided on board. The LEDs enabled or disabled via jumpers JP7 – JP10. The LEDs are controlled by the IOBUS signals on the VNC2.

Note - LED5 is also connected to jumper JP1 on the board. Care should be taken to ensure that LED is not being driven by JP1 when controlling the LED from the VNC2.

Designator	VCN2 pin number		
	32-PIN	48-PIN	64-PIN
LED3	12	12	12
LED4	14	13	13
LED5[39]	-	46	29
LED6	-	45	31

Notes:
(39) LED5 is also connected to jumper JP1 on the board. Care should be taken to ensure that LED is not being driven by JP1 when controlling the LED from the VNC2.

Table 5.14 User LEDs connections.

5.11 LED enable/disable jumpers JP10 – JP14.

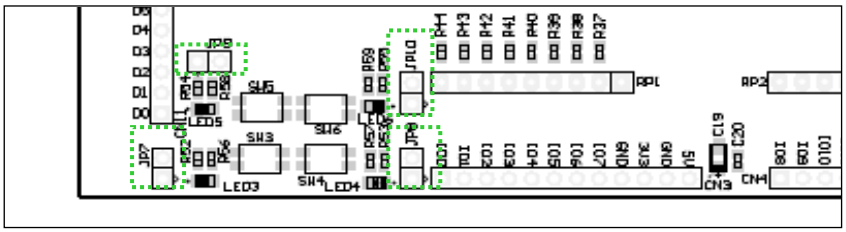


Figure 5.16 LED Enable/Disable jumpers.

Every user-defined LED have an enable/disable jumper. When jumper is closed LED will be illuminate when driven low by one of the VNC2 pins. When jumper is opened LED is disconnected from the VCN2 pin.

Designator	LED affected
JP7	LED3
JP8	LED4
JP9	LED5
JP10	LED6

Table 5.15 LED Enable/Disable Jumpers.

5.12 User push button switches

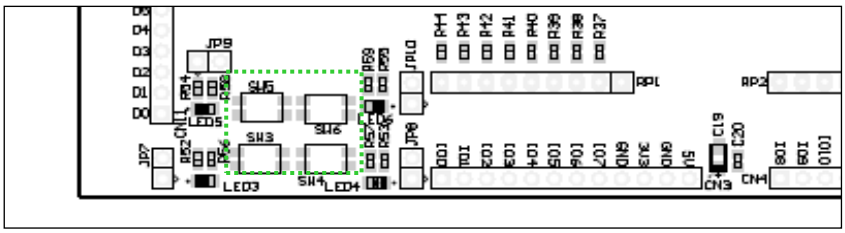


Figure 5.17 User Push Button Switches.

Push button switches connected straight to VNC2 pins. When the switch is pressed down, a logic LOW appears on the corresponding VNC2 pin.

Designator	VNC2 Pin Number		
	32-PIN	48-PIN	64-PIN
SW3(40)	15	14	14
SW4(40)	-	48	32
SW5(40)	-	42	48
SW6(40)	-	43	49

Notes:
(40) The IOBUS pins are shared by other connectors on the board. Care should be taken to ensure that operation of the switches does not interfere with pins used by other headers on the board.

Table 5.16 User Switches

5.13 Host USB power jumpers JP4, JP5.

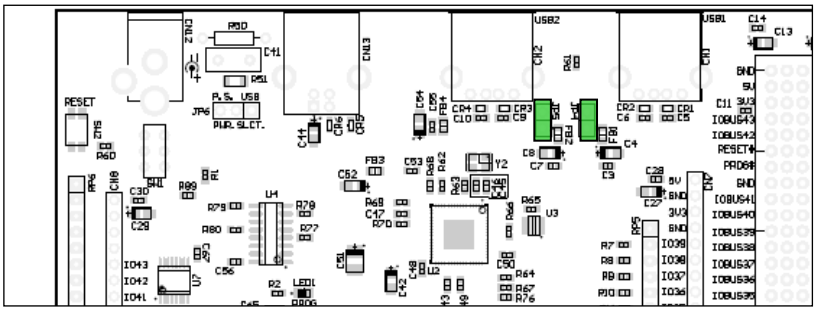


Figure 5.18 USB Power Enable Jumpers JP4 and JP5.

When either USB1 and/or USB2 ports are used as a host ports, the jumpers JP4 and/or JP5 accordingly should be closed to allow peripheral devices to draw power from board's +5V power rail.

Warning!

When using USB1 and USB2 ports as a USB slave ports, remove the shunts from jumpers JP4 and JP5. Failure to do so could cause damage to the USB host or to the V2-EVAL board.

5.14 Remote Wakeup jumper JP3.

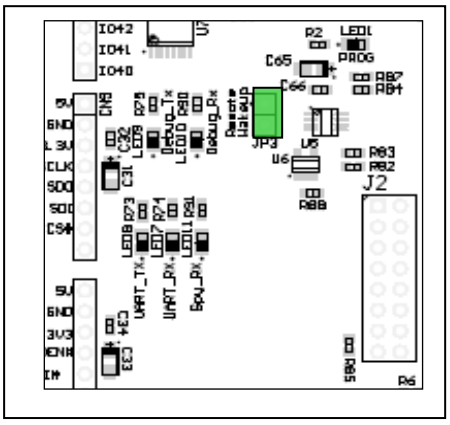


Figure 5.19 Remote Wakeup Jumper.

The remote wakeup jumper enables any firmware running on the VNC2 to support Suspend Monitor (SUM) mode, allowing the device to reduce power consumption when idle. The VNC2 device can be configured to wakeup when any data arrives on the receive data (RXD) pin, by connecting the RXD pin to ring indicator (RI#) input via jumper JP3. When RI# pin is driven low, VNC2 will resume from the SUM mode immediately. The remote wakeup feature is only available when using the UART interface on the VNC2. The feature can be enabled when a jumper is present on jumper JP3.

5.15 Reset Push-button Switch

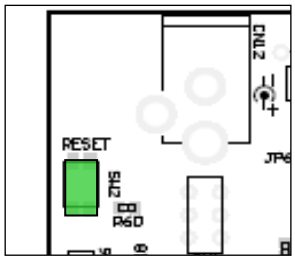


Figure 5.20 Reset Switch

A 'RESET' push button switch is provided on switch SW2, to enable manual resetting of the VNC2 device.

5.16 'PROG' LED

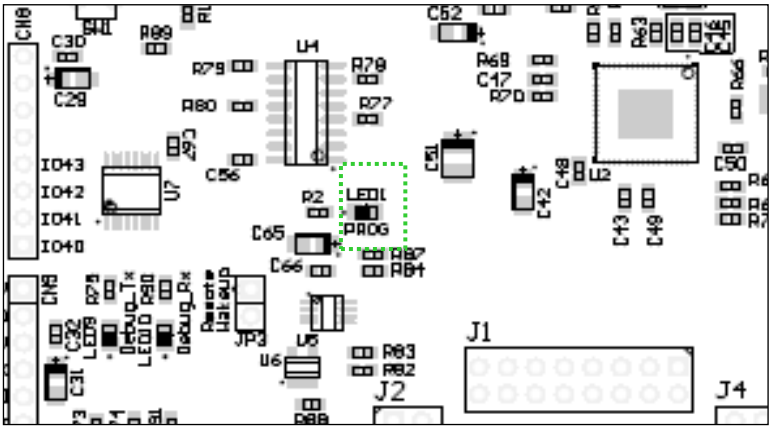


Figure 5.21 'PROG' LED

LED1 (red) is provided to indicate when VNC2 device is in Flash programming mode.

5.17 VNC2 Daughterboard Connector – J1

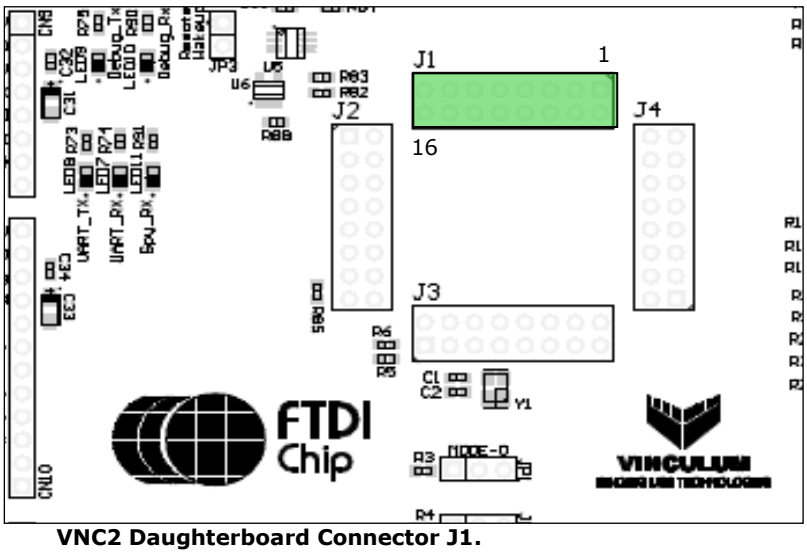


Figure 5.22 VNC2 Daughterboard Connector J1.

Schematic Signal Name(41)	Connector Pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
3.3V	1	-	-	-	-	3.3V power rail.
3.3V	2	-	-	-	-	3.3V power rail.
GND	3	-	-	-	-	Ground pin.
USB1DP	4	17	25	33	IO	USB1 transceiver, data line positive connected to CN1.
USB1DM	5	18	26	34	IO	USB1 transceiver, data line minus connected to CN1.
SPI_S0_CLK	6	29	15	51	IO	Connected to P1 pin 38 / CN7 pin 1.
SPI_S0_MOSI	7	30	16	52	IO	Connected to P1 pin 39 / CN7 pin 2.
SPI_S0_MISO	8	31	18	55	IO	Connected to P1 pin 40 / CN7 pin 3.
SPI_S0_CS#	9	32	19	56	IO	Connected to P1 pin 40 / CN7 pin 4.
USB2DP	10	20	28	36	IO	USB2 transceiver, data line positive connected to CN2.
USB2DM	11	21	29	37	IO	USB2 transceiver, data line minus connected to CN2.
V_TXD	12	23	31	39	IO	Connected to P1 pin 25 / CN10 pin 1 / CN5 pin 5.
V_RXD	13	24	32	40	IO	Connected to P1 pin 26 / CN10 pin 2 / CN5 pin 6.
V_RTS#	14	25	33	41	IO	Connected to P1 pin 27 / CN10 pin 3 / CN5 pin 7.
V_CTS#	15	26	34	42	IO	Connected to P1 pin 28 / CN10 pin 4 / CN5 pin 8.
V_DTR#	16	-	35	43	IO	Connected to P1 pin 29 / CN10 pin 5 / CN6 pin 1.

Notes:
(41) The signal names relate to the labels used on pages 1 & 2 of the V2-EVAL base board schematic. Unless otherwise stated, the function of the IO signals is be set by the user application running on the VNC2.

Table 5.17 Connector J1 Pinout.

5.18 VNC2 Daughterboard Connector – J2

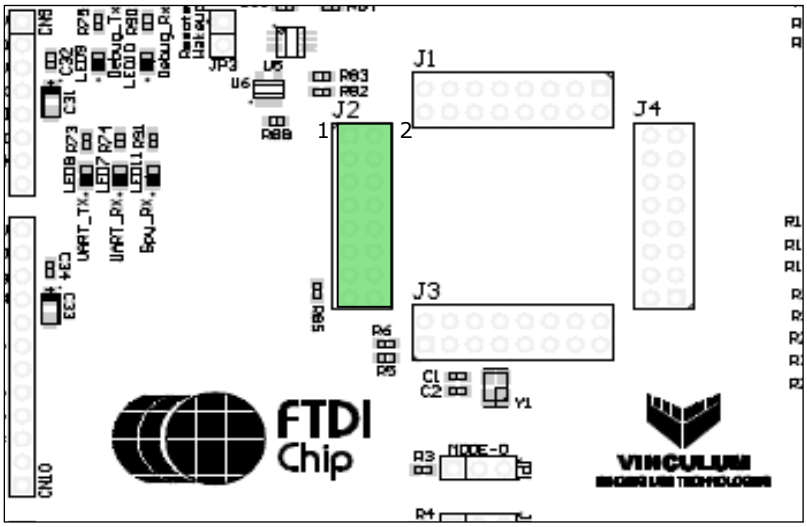


Figure 5.23 VNC2 Daughterboard Connector J2.

Schematic Signal Name[42]	Connector Pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
V_DSR#	1	-	36	44	IO	Connected to P1 pin 30 / CN10 pin 6 / CN6 pin 2.
V_DCD#	2	-	37	45	IO	Connected to P1 pin 31 / CN10 pin 7 / CN6 pin 3.
V_RI#	3	-	38	46	IO	Connected to P1 pin 32 / CN10 pin 8 / CN6 pin 4.
V_TXDEN	4	-	41	47	IO	Connected to P1 pin 33 / CN10 pin 9 / CN6 pin 5.
3.3V	5	-	-	-	-	3.3V power rail.
3.3V	6	-	-	-	-	3.3V power rail.
GPIO7	7	-	42	48	IO	Connected to P1 pin 34 / CN6 pin 6.
GPIO8	8	-	43	49	IO	Connected to P1 pin 36 / CN6 pin 7.
GPIO9	9	-	44	50	IO	Connected to P1 pin 37 / CN6 pin 8.
SPI_S1_CLK	10	-	-	57	IO	Connected to P1 pin 42 / CN7 pin 5.
SPI_S1_MOSI	11	-	-	58	IO	Connected to P1 pin 43 / CN7 pin 6.
SPI_S1_MISO	12	-	-	59	IO	Connected to P1 pin 44 / CN7 pin 7.
GND	13	-	-	-	-	Ground pin.
SPI_S1_CS#	14	-	-	60	IO	Connected to P1 pin 45 / CN7 pin 8.
DEBUG_IF	15	11	11	11	IO	Debug pin. Connected to P1 pin 4 / CN3 pin 1.
GND	16	-	-	-	-	Ground pin.

Notes:
(42) The signal names relate to the labels used on pages 1 & 2 of the V2-EVAL base board schematic. Unless otherwise stated, the function of the IO signals is set by the user application running on the VNC2.

Table 5.18 Connector J2 Pinout.

5.19 VNC2 Daughterboard Connector – J3

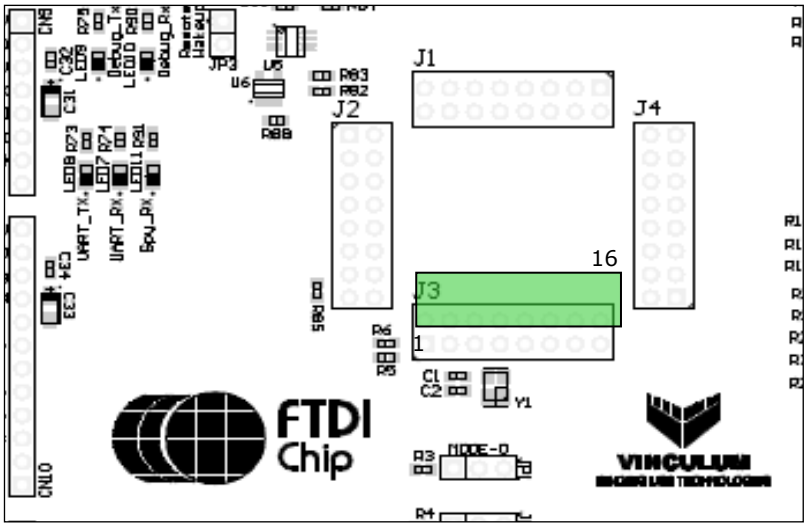


Figure 5.24 VNC2 Daughterboard Connector J3.

Schematic Signal Name(43)	Connector Pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
PROG#	1	9	10	10	Input	PROG# input to VNC2. Connected via multiplexer U4.
RESET#	2	10	9	9	Input	RESET# input to VNC2. Connected via multiplexer U4.
SPI_M_CS#	3	-	23	64	IO	Connected to P1 pin 52 / CN9 pin 7/ CN8 pin 4.
SPI_M_MISO	4	-	22	63	IO	Connected to P1 pin 51 / CN9 pin 6/ CN8 pin 3.
SPI_M_MOSI	5	-	21	62	IO	Connected to P1 pin 47 / CN9 pin 5/ CN8 pin 2.
SPI_M_CLK	6	-	20	61	IO	Connected to P1 pin 46 / CN9 pin 4/ CN8 pin 1.
XTOUT	7	5	5	5	Output	Output from 12MHz oscillator cell on VNC2.
XTIN	8	4	4	4	Input	Input to 12MHz oscillator cell on VNC2.
GPIO2	9	14	13	13	IO	Connected to P1 pin 6 / CN3 pin 3.
GPIO1	10	12	12	12	IO	Connected to P1 pin 5 / CN3 pin 2.
FIFO_DATA0	11	-	-	15	IO	Connected to P1 pin 8/CN3 pin 5 /CN11 pin 1.
GPIO3	12	15	14	14	IO	Connected to P1 pin 7 / CN3 pin 4.
FIFO_DATA2	13	-	-	17	IO	Connected to P1 pin 10/CN3 pin 7 /CN11 pin 3.
FIFO_DATA1	14	-	-	16	IO	Connected to P1 pin 9/CN3 pin 6 /CN11 pin 2.
GND	15	-	-	-	-	Ground pin.
GND	16	-	-	-	-	Ground pin.

Notes:
(43) The signal names relate to the labels used on pages 1 & 2 of the V2-EVAL base board schematic. Unless otherwise stated, the function of the IO signals is set by the user application running on the VNC2.

Table 5.19 Connector J3 Pinout.

5.20 VNC2 Daughterboard Connector – J4

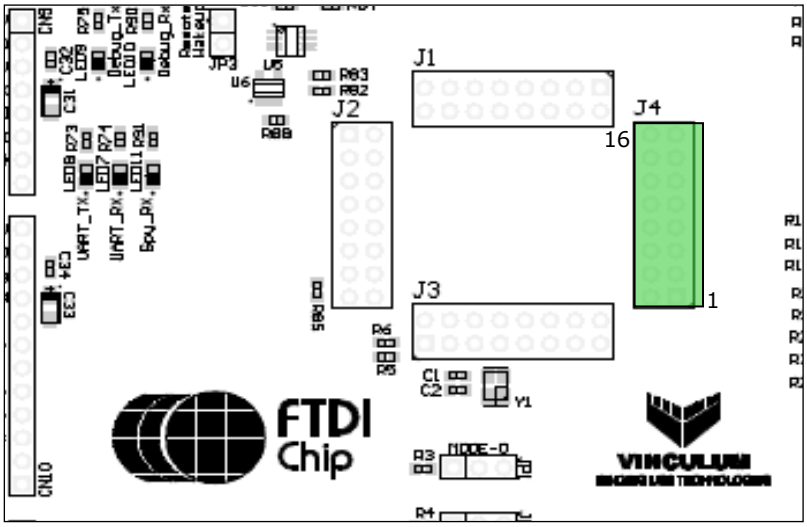


Figure 5.25 VNC2 Daughterboard Connector J4.

Schematic Signal Name(44)	Connector Pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
FIFO_DATA4	1	-	-	19	IO	Connected to P1 pin 12 / CN4 pin 1/ CN11 pin 5.
FIFO_DATA3	2	-	-	18	IO	Connected to P1 pin 11 / CN3 pin 8/ CN11 pin 4.
FIFO_DATA6	3	-	-	22	IO	Connected to P1 pin 14 / CN4 pin 3/ CN11 pin 7.
FIFO_DATA5	4	-	-	20	IO	Connected to P1 pin 13 / CN4 pin 2/ CN11 pin 6.
FIFO_RXF#	5	-	-	24	IO	Connected to P1 pin 16 / CN4 pin 5/ CN11 pin 9.
FIFO_DATA7	6	-	-	23	IO	Connected to P1 pin 15 / CN4 pin 4/ CN11 pin 8.
FIFO_RD#	7	-	-	26	IO	Connected to P1 pin 18 / CN4 pin 7/ CN11 pin 11.
FIFO_TXE#	8	-	-	25	IO	Connected to P1 pin 17 / CN4 pin 6/ CN11 pin 10.
FIFO_OE#	9	-	-	28	IO	Connected to P1 pin 21 / CN5 pin 1 / CN11 pin 13.
FIFO_WR#	10	-	-	27	IO	Connected to P1 pin 20 /CN4 pin 8 / CN11 pin 12.
GPIO5	11	-	45	31	IO	Connected to P1 pin 23 / CN5 pin 3.
INT_SEL0	12	-	46	29	IO	Connected to P1 pin 22 / CN5 pin 2.
INT_SEL1	13	-	47	-	IO	Connected to jumper JP2.
GPIO6	14	-	48	32	IO	Connected to P1 pin 24 / CN5 pin 4.
GND	15	-	-	-	-	-
GND	16	-	-	-	-	-

Notes:
(44) The signal names relate to the labels used on pages 1 & 2 of the V2-EVAL base board schematic. Unless otherwise stated, the function of the IO signals is set by the user application running on the VNC2.

Table 5.20 Connector J4 Pinout.

6 FT4232H Configuration

The V2-EVAL board features a FT4232H, a high speed USB to quad channel UART / serial converter device. The device is primarily featured to provide a connection from the board to a PC host via the onboard USB type B connector. Each of the four channels on the FT4232H device are used to provide a separate functions on the V2-EVAL board.

The functions of the FT4232H include:

- Channel A – UART interface. The FT4232H provides USB to UART conversion to allow a PC / USB host PC to communicate with the VNC2, via the UART interface.
- Channel B – Debug interface control. Enable software tool chain connectivity to the VNC2 debug interface via the the USB type B connector on the board.
- Channel C - Provide a UART data 'sniffer' interface allowing inputs to the VNC2 UART interface to be displayed on the host PC software.
- Channel D – Device control. I/O pins are used to control the onboard multiplexer. The multiplexer allows different interfaces to drive the VNC2 UART interface as well as the VNC2 PROG# and RESET# pins.

Figure 6.1, outlines the configuration circuit for FT4232H I/O ports.

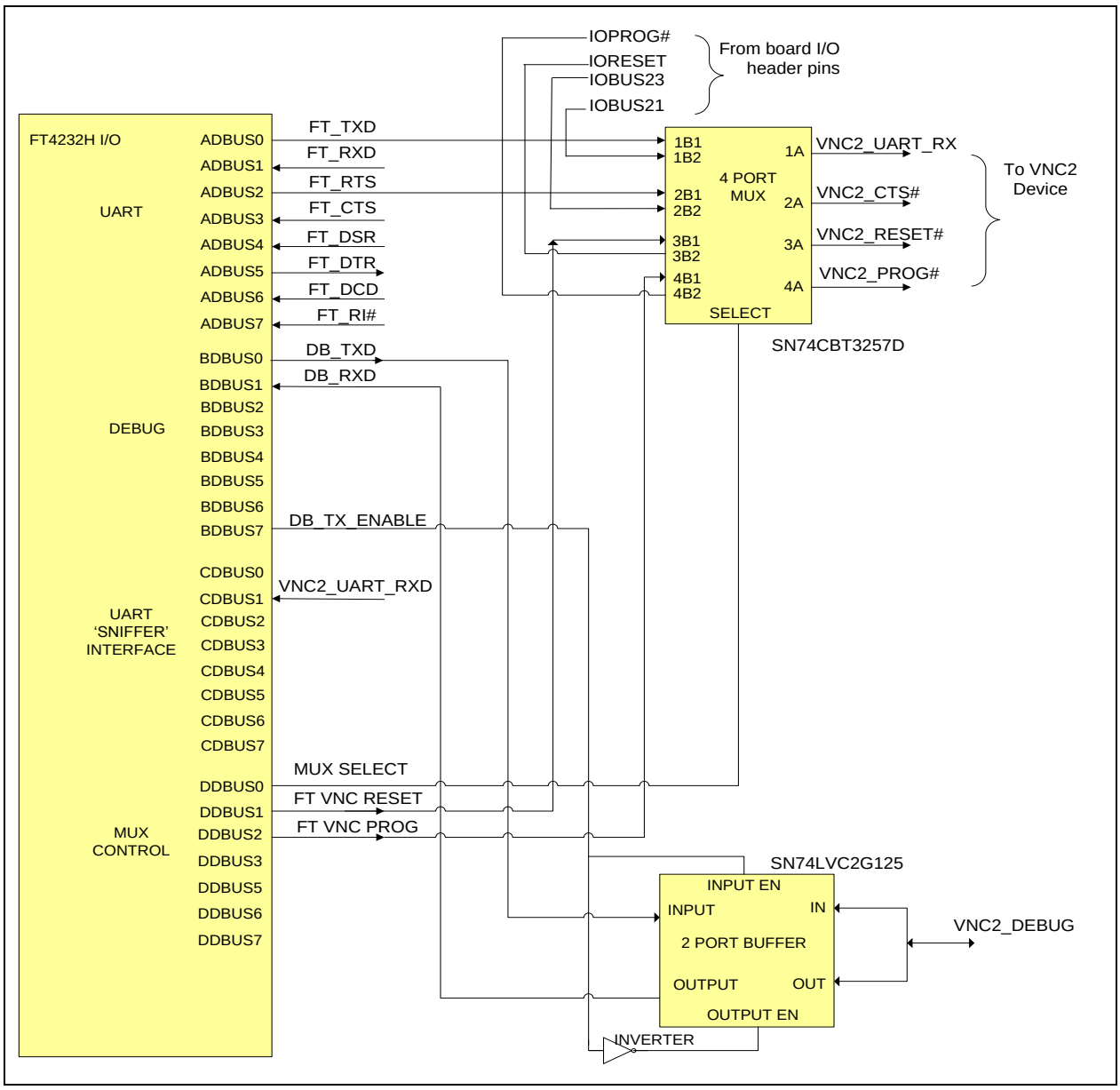


Figure 6.1: FT4232H Configuration

6.1 UART Interface

The FT4232H channel A, ADBUS I/O, pins are used for UART operation with the VNC2. The UART inputs to the FT4232H are supplied directly from the VNC2 device pins, while the UART outputs from the FT4232H, are passed to an external multiplexer. The multiplexer allows the UART interface to the VNC2 to be driven by either by the FT4232H device or by an external UART device, which is connected to the V2-EVAL board via the various board I/O header pins. The multiplexer select pin is controlled by pin DDBUS0 on the FT4232H, where a logic '0' on the select pin will force the FT4232H device to drive the UART interface on the VNC2, while a logic '1' will allow IOBUS21 and IOBUS23 header pins on the board to drive the UART.

6.2 Debug Interface – UART Mode

The FT4232H channel B I/O pins are used to control the debug interface on the VNC2 device. The channel is used to allow the device debug pin to be connected to a software debugger environment running on a PC. The single bit, bi-directional debug signal from VNC2 is converted into a UART style interface, with separate transmit and receive signals, via the 2-port buffer. The signal on the BDBUS0 pin corresponds to the transmit data from the debug software, while BDBUS1 corresponds to the receive output from the VNC2. Pin BDBUS7, DB_TX_ENABLE, on the FT4232H is used for controlling transmit and receive operation on the 2 port buffer.

6.3 UART 'Sniffer' Interface

Channel C on the FT4232H device is configured as a UART interface. The channel is used as a 'data sniffer' to detect any data sent to the VNC2 UART interface. The detected data is passed to software running on the PC for display. The feature is used for detecting and displaying UART data from external sources which are connected to the VNC2 UART interface, via the board I/O headers.

6.4 Device Control – Bit Bang Mode

The I/O signals on FT4232H channel D are used for additional control functions on the board. Pin DDBUS0 is used to control the channel select input on the multiplexer. A logic '0' on the multiplexer select pin will force multiplexer input B1 to drive the multiplexer output A, while a logic '1' will force multiplexer input B2 to drive the multiplexer output.

Pins DDBUS1 and DDBUS2 are used for controlling the PROG# and RESET# inputs on the VNC2 from the software via the FT4232H. Both pins are passed to the onboard multiplexer. A logic '0' on the multiplexer select input will allow the VNC2 PROG# and RESET# pins to be controlled by the FT4232H.

Table 6.1, summarises the V2-EVAL board settings based on the value of the multiplexer select pin.

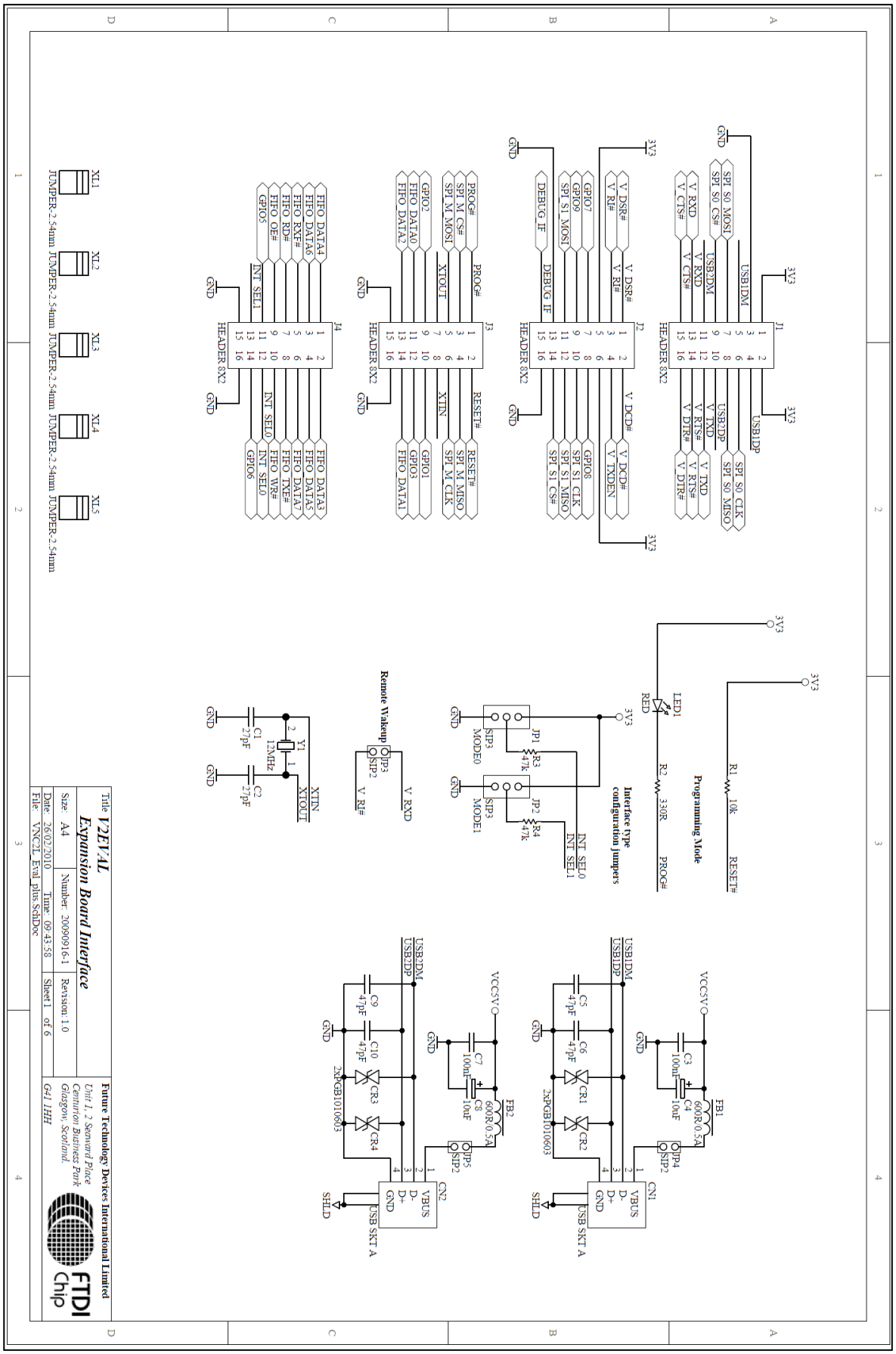
Multiplexer Select Pin Status (Set by FT4232H DDBUS0)	Board Configuration Status
0	VNC2 UART interface connected to FT4232H channel A. VNC2 RESET# connected to FT4232H DDBUS1 output. VNC2 PROG# connected to FT4232H DDBUS2 output.
1	VNC2 UART interface connected to header pins on V2-EVAL board. VNC2 RESET# connected to prototyping area header pin 50. VNC2 PROG# connected to prototyping area header pin 49.

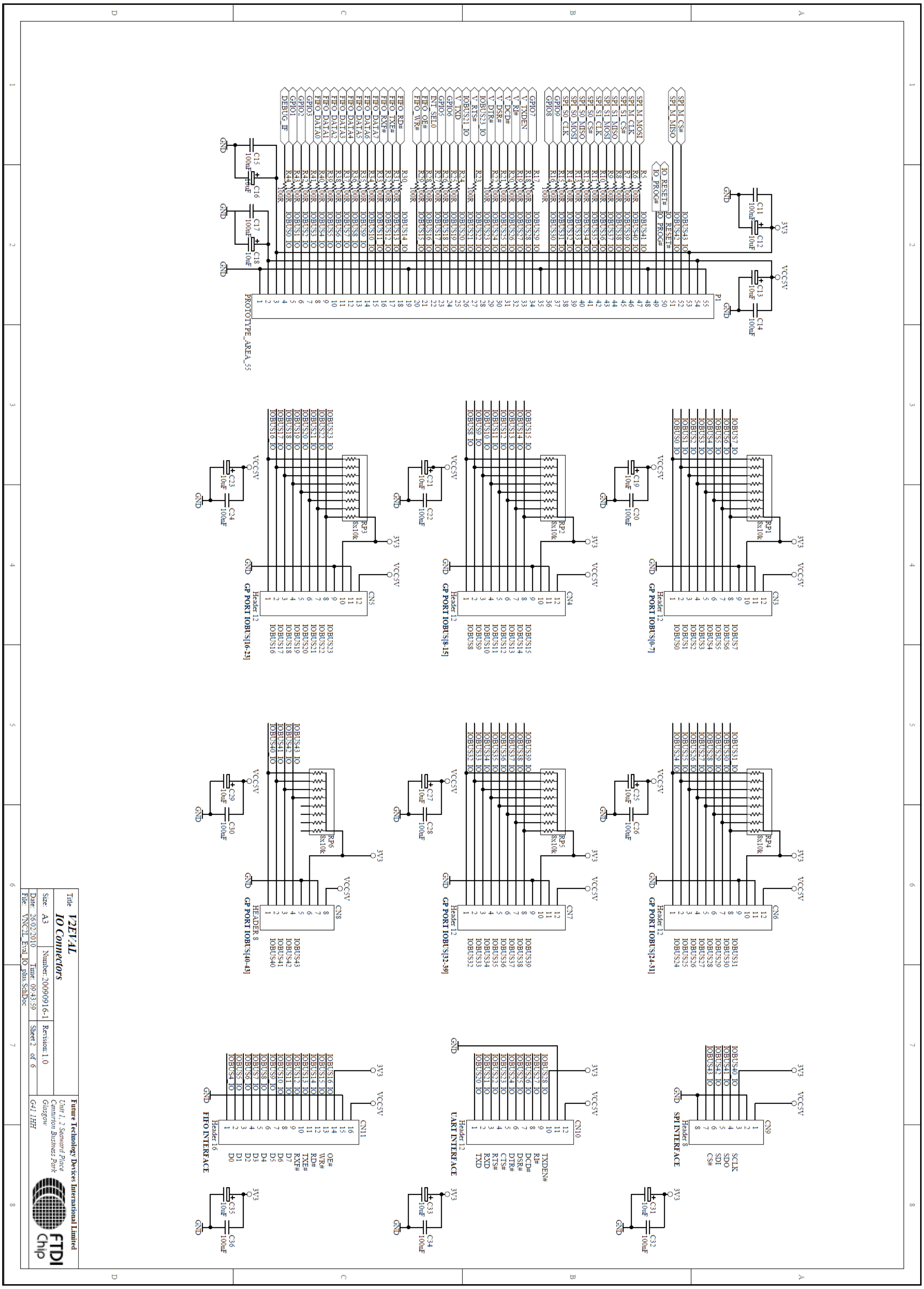
Table 6.1 Multiplexer Configuration Settings

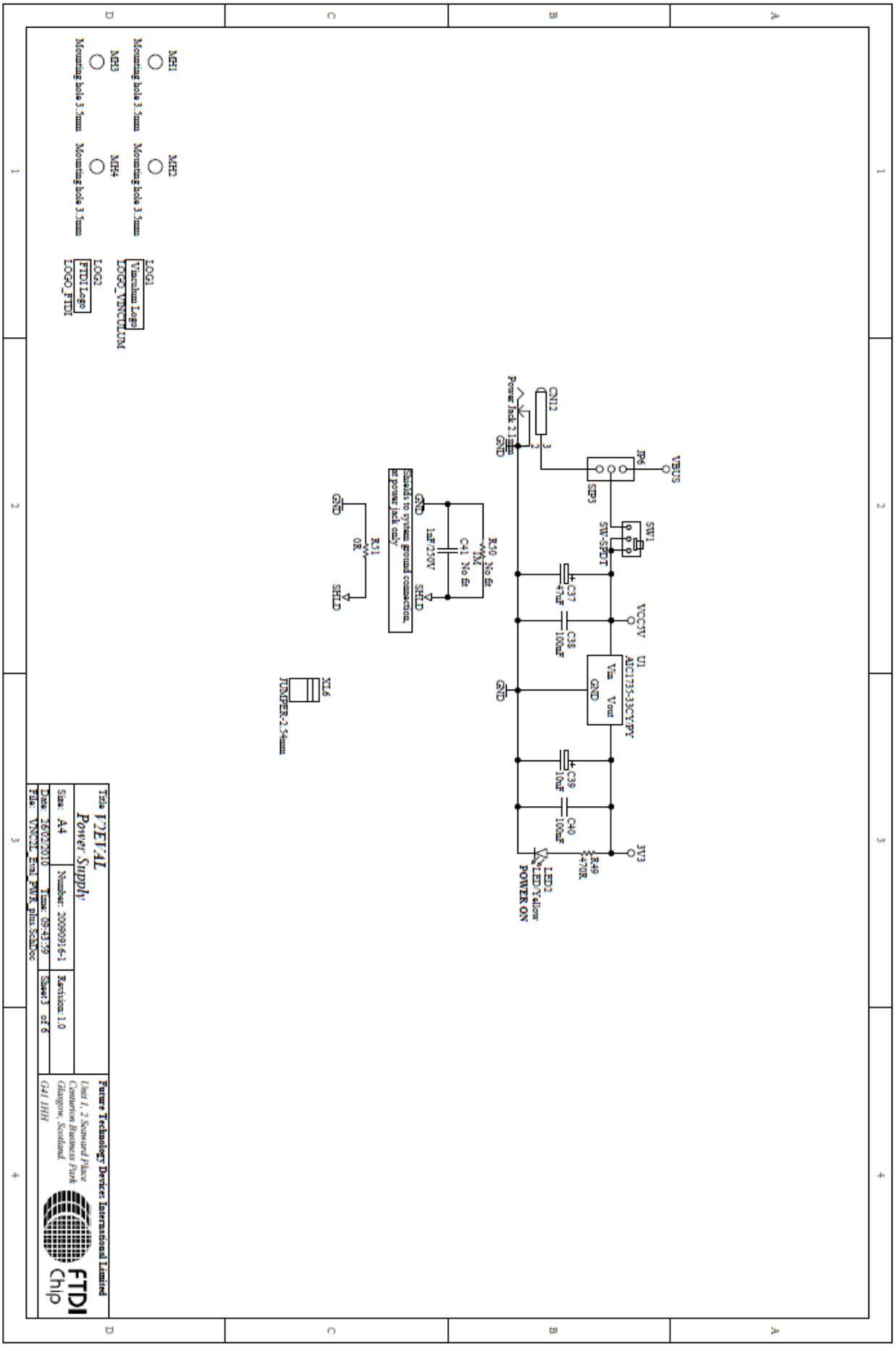
7 Board Schematics.

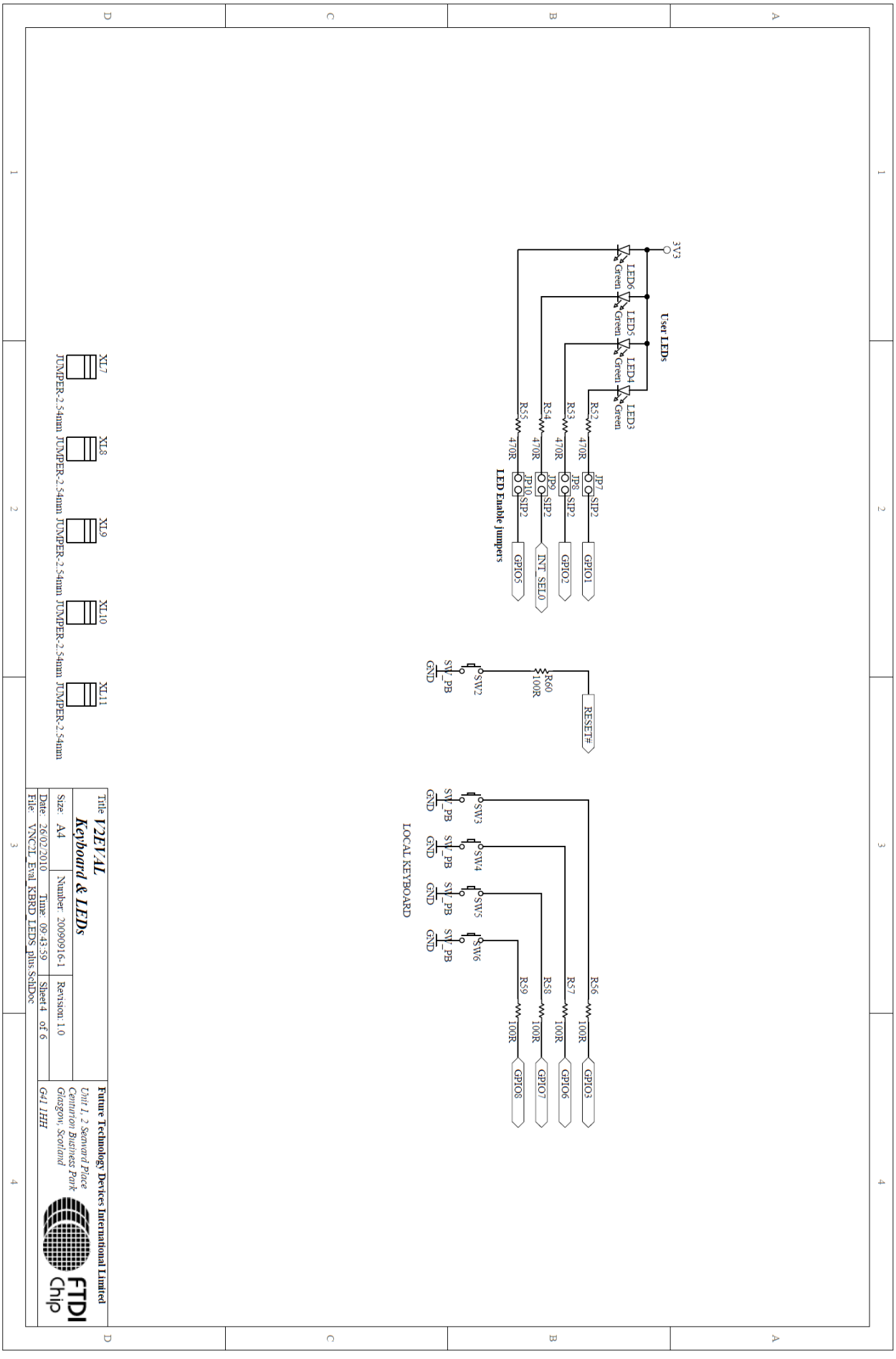
Schematics for the V2-EVAL board and VNC2 daughterboards are found in the following section.

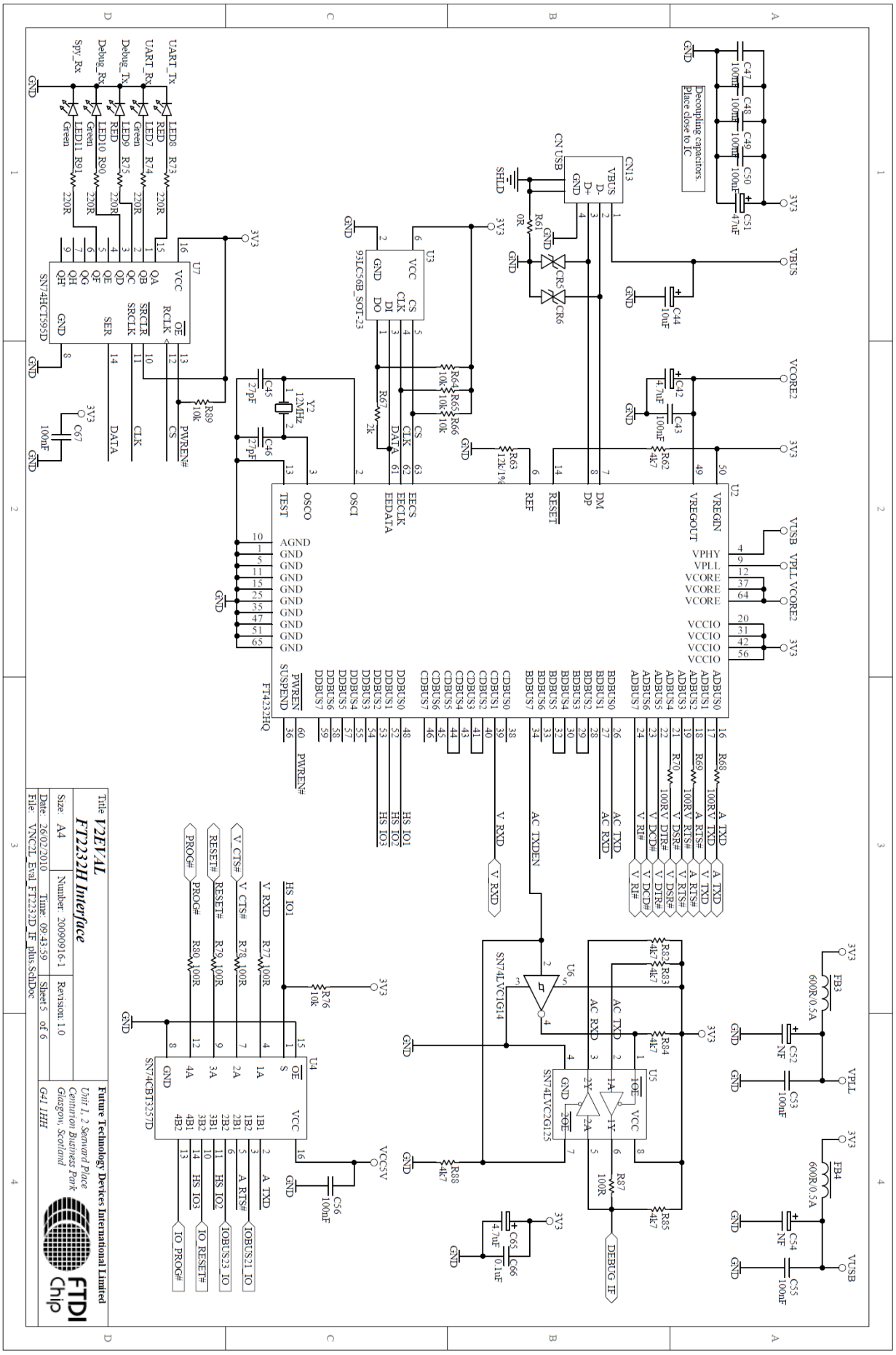
7.1 V2-EVAL Board Schematics



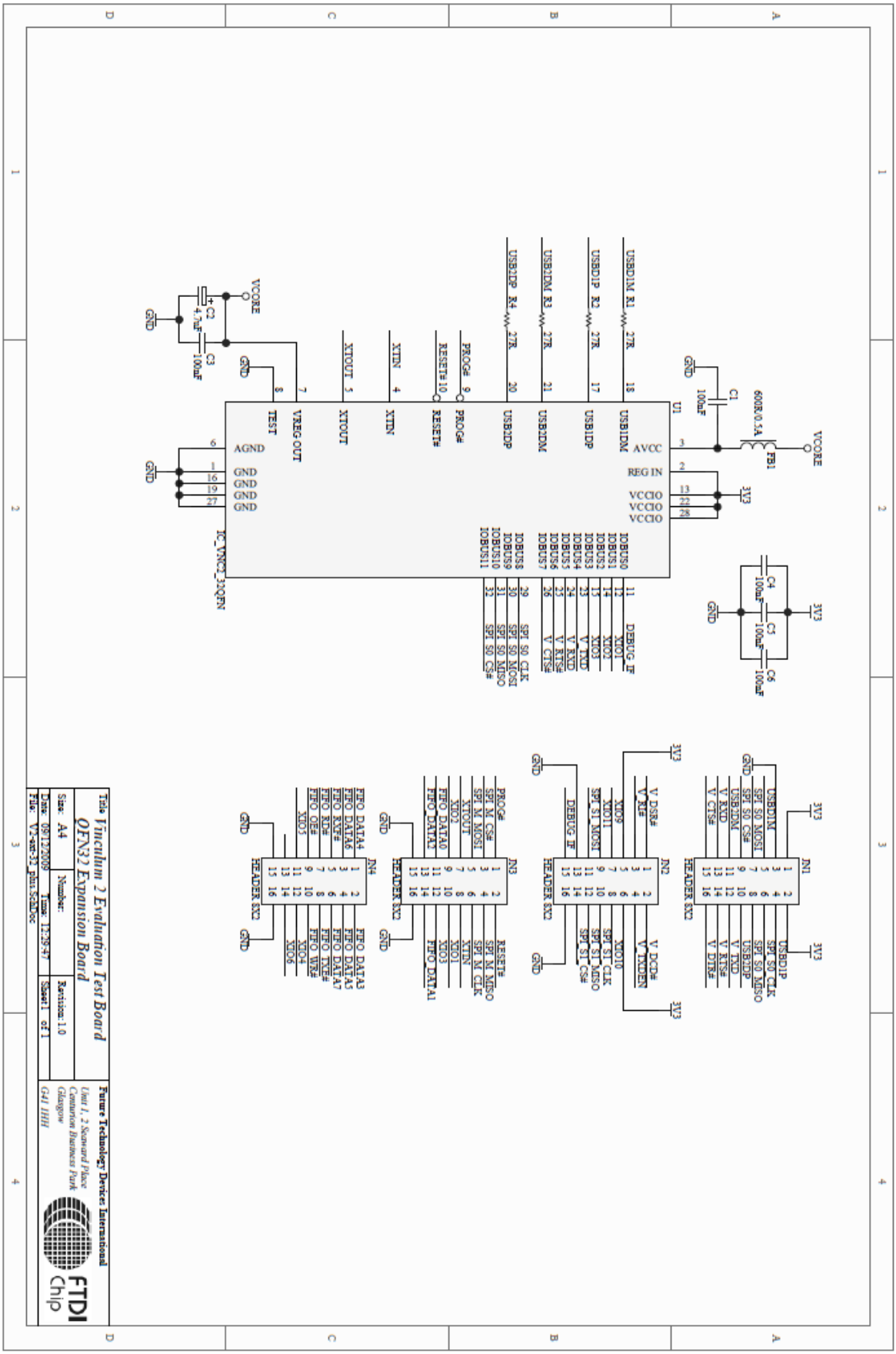




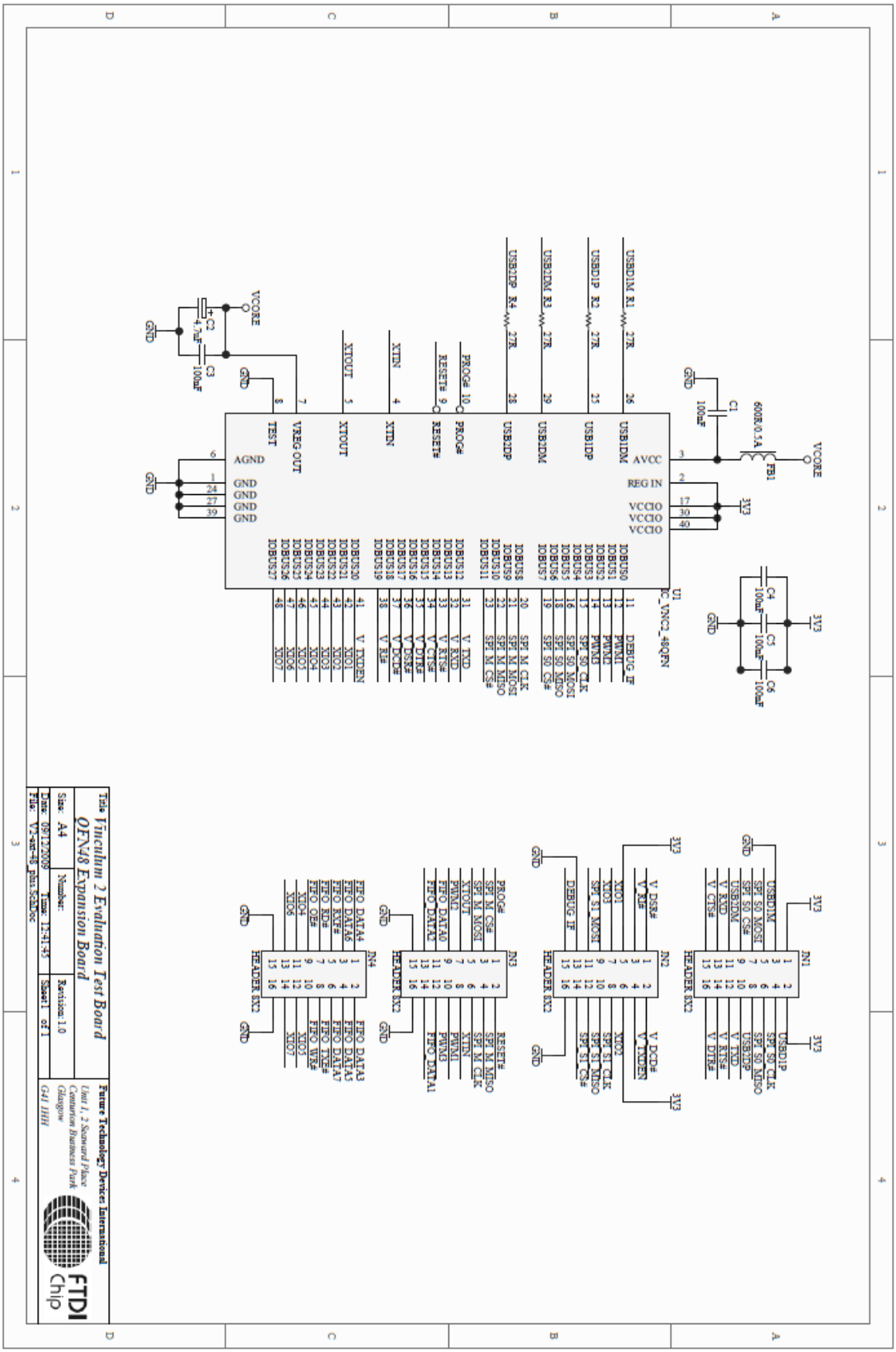

3V3
LED6 Green
LED5 Green
LED4 Green
LED3 Green
User LEDs
R52 470R
R53 470R
R54 470R
R55 470R
JP7 SIP2
JP8 SIP2
JP9 SIP2
JP10 SIP2
LED Enable jumpers
GPIO1
GPIO2
INT_SEL0
GPIO5
SW2
SW_PB
GND
R60 100R
RESET#
SW3
SW4
SW5
SW6
LOCAL KEYBOARD
R56 100R
R57 100R
R58 100R
R59 100R
GPIO3
GPIO6
GPIO7
GPIO8
XL7 JUMPER-2.54mm
XL8 JUMPER-2.54mm
XL9 JUMPER-2.54mm
XL10 JUMPER-2.54mm
XL11 JUMPER-2.54mm
Title V2EVAL Keyboard & LEDs
Size: A4
Number: 20090916-1
Revision: 1.0
Date: 26/02/2010
Time: 09:43:59
Sheet 4 of 6
File: VNC2L_Eval_KBRD_LEDS_plus.SchDoc
Future Technology Devices International Limited
Unit 1, 2 Seaward Place
Centurion Business Park
Glasgow, Scotland
G41 1HH



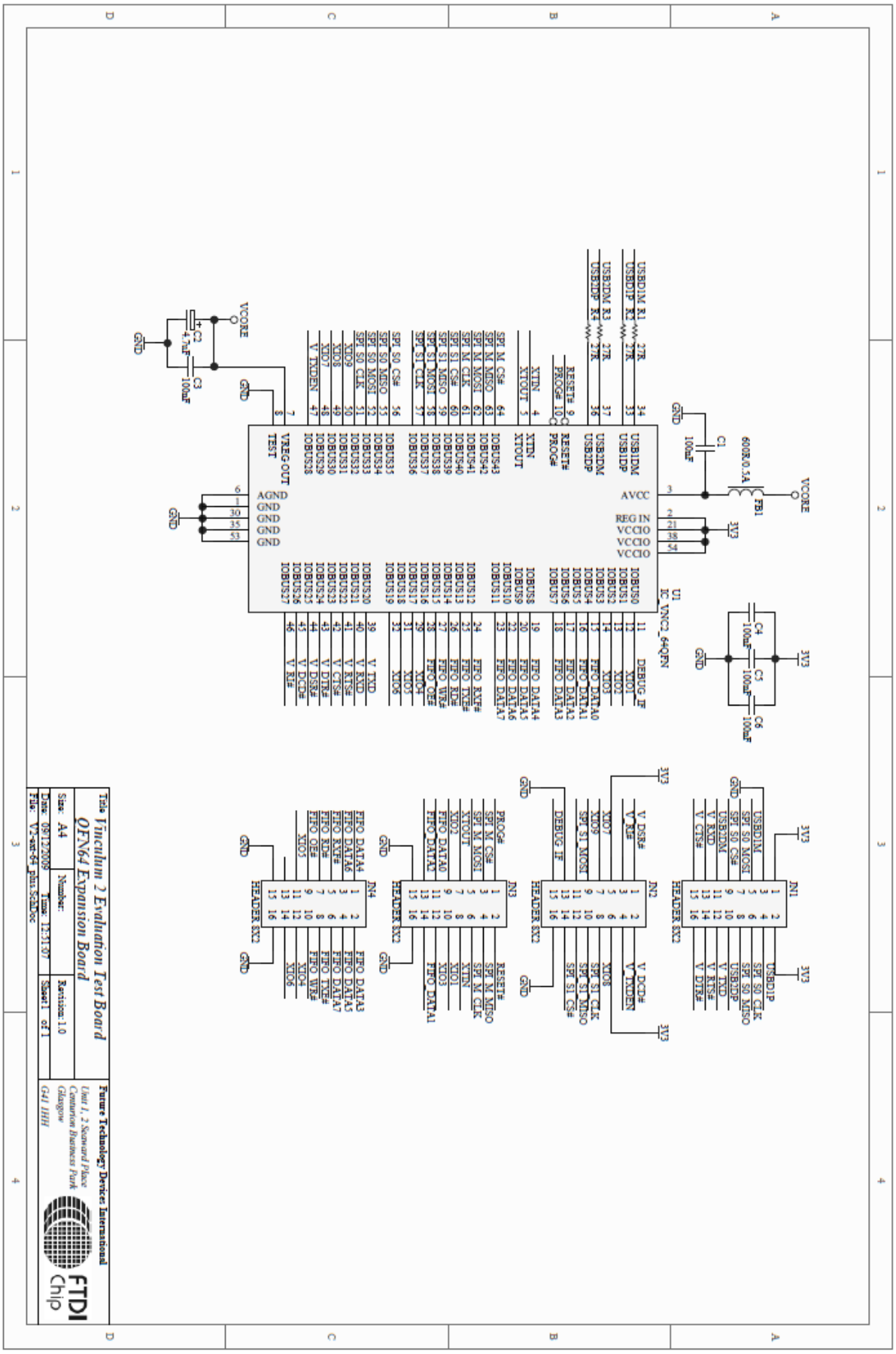
7.2 VNC2 Daughterboard 32-pin QFN Schematic



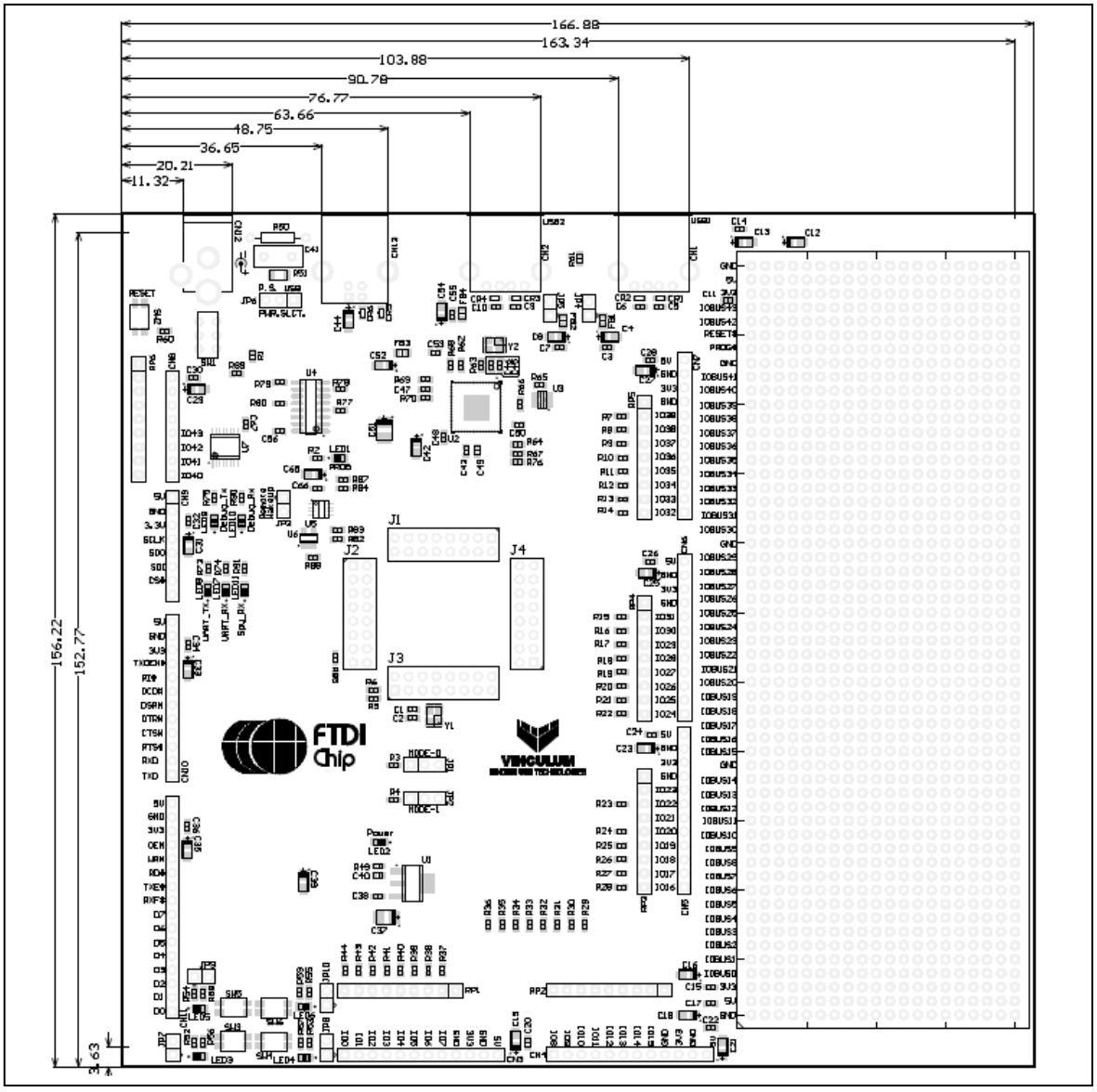
7.3 VNC2 Daughterboard - 48-pin QFN Schematic



7.4 VNC2 Daughterboard - 64-pin QFN Schematic



8 V2-EVAL Board Assembly Drawing



Dimensions in mm.Tolerance is ±0.1mm

Contact Information

Head Office – Glasgow, UK

Future Technology Devices International Limited
Unit 1, 2 Seaward Place,
Centurion Business Park
Glasgow, G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com
Web Site URL http://www.ftdichip.com
Web Shop URL http://www.ftdichip.com

Branch Office – Taipei, Taiwan

Future Technology Devices International Limited (Taiwan)
2F, No 516, Sec. 1 NeiHu RoIOBUS
Taipei 114
Taiwan, R.O.C.
Tel: +886 (0) 2 8791 3570
Fax: +886 (0) 2 8791 3576

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Support) tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com
Web Site URL http://www.ftdichip.com

Branch Office – Hillsboro, Oregon, USA

Future Technology Devices International Limited (USA)
7235 NW Evergreen Parkway, Suite 600
Hillsboro, OR 97123-5803
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales) us.sales@ftdichip.com
E-Mail (Support) us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com
Web Site URL http://www.ftdichip.com

Branch Office – Shanghai, China

Future Technology Devices International Limited (China)
Room 408, 317 Xianxia RoIOBUS,
ChangNing District,
ShangHai, China

Tel: +86 (21) 62351596
Fax: +86(21) 62351595

E-Mail (Sales): cn.sales@ftdichip.com
E-Mail (Support): cn.support@ftdichip.com
E-Mail (General Enquiries): cn.admin1@ftdichip.com
Web Site URL http://www.ftdichip.com

Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – List of Figures and Tables

List of Figures

List of Tables

Appendix B – Revision History

Rev 1.0	First Release	15th April 2010