CYUSB3KIT-001

EZ-USB® FX3 Development Kit Guide

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Contents

1. Introduction

The Cypress EZ-USB FX3 Development Kit (DVK) is a combination of hardware, software, and documentation that enables customers to evaluate the FX3 device. You can use this DVK to start hardware or software integration and then move to the final systems after the integration phase is complete.

This guide only targets the hardware. The software development kit (SDK) documentation comes with the SDK installation. It is located in the folder: `Cypress\FX3 SDK\doc`, where 'FX3 SDK' is the custom installation folder name.

1.1 Kit Contents

The Cypress EZ-USB FX3 DVK includes the following:

- Development kit PCB
- USB3.0 A to Micro B cable
- Quick Start Guide
- Kit CD
- 5-V DC adapter

1.2 Additional Learning Resources

Visit www.cypress.com for additional learning resources in the form of data sheets, technical reference manual and application notes.

1.3 Document History

Revision	PDF Creation Date	Origin of Change	Description of Change
**	06/23/2011	MRKA	Initial version of kit guide
*A	08/11/2011	MRKA	Updated figures and table in GPIF II Connector section. Updated Table 2-3 and Figure 2-11. Added Figure 2-12.

1.4 Documentation Conventions

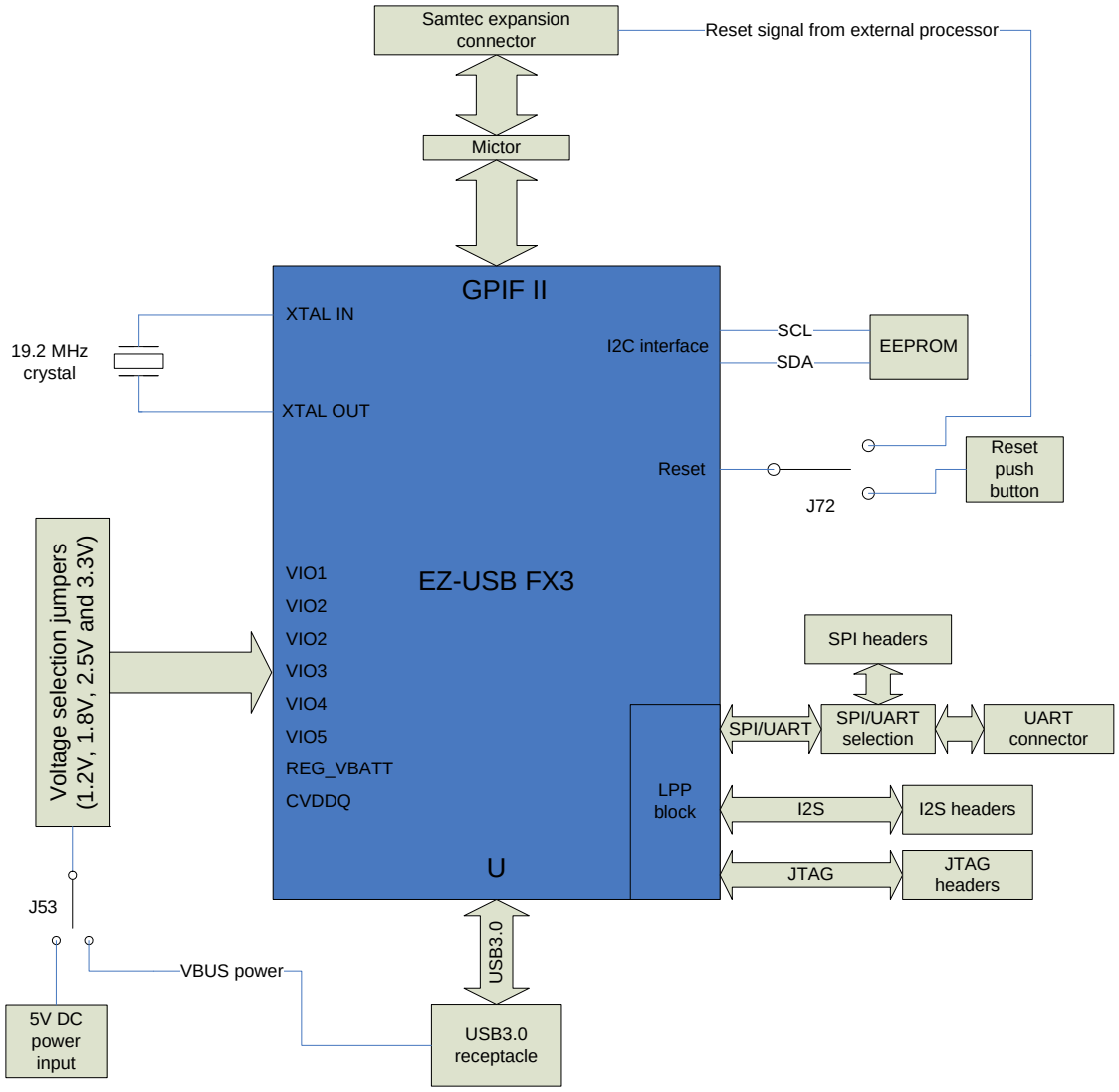
Table 1-1. Document Conventions for Guides

Convention	Usage
`Courier New`	Displays file locations, user entered text, and source code: `C:\ ...cd\icc\`
Italics	Displays file names and reference documentation: Read about the *sourcefile.hex* file in the *PSoC Designer User Guide*.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: 2 + 2 = 4
Text in gray boxes	Describes cautions or unique functionality of the product.

2. Getting Started

2.1 Development Board

Figure 2-1. FX3 DVK Board Block Diagram



2.1.1 Power Supply

The board can be powered either from a 5-V DC external power or from the USB host (VBUS line). Use the SW9 toggle switch on the board to select an option. If VBUS is used to power the board, populate J53 with jumpers. The voltage for FX3 I/O power domains can be selected using on-board selection jumpers. These domains include VIO1, VIO2, VIO3, VIO4, VIO5, REG_VBATT, and CVDDQ. All other power domains are tied to 1.2 V.

The following table shows the power domain selection option through jumpers.

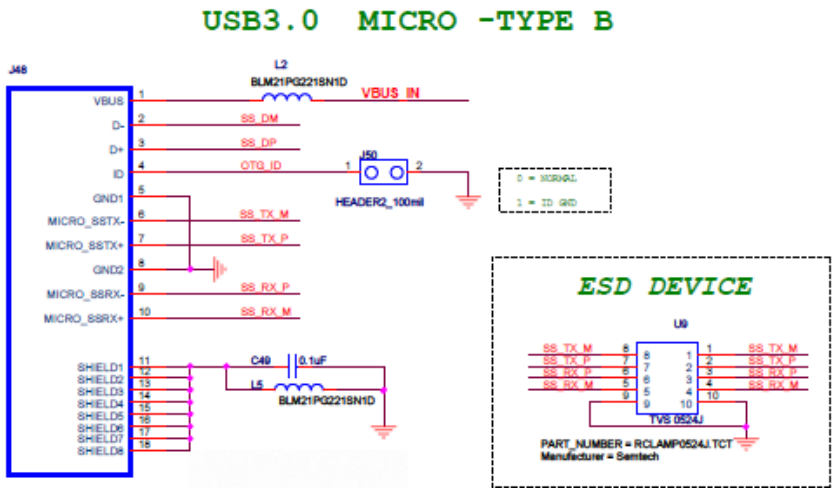
Table 2-1. Power Supply Domains

Power Domain	Description	Headers	Voltage Levels
VIO1	IO1 domain	J136	1.8 V, 2.5 V, 3.3 V
VIO2	IO2 domain	J144	1.8 V, 2.5 V, 3.3 V
VIO3	IO3 domain	J145	1.8 V, 2.5 V, 3.3 V
VIO4	IO4 domain	J146	1.8 V, 2.5 V, 3.3 V
VIO5	IO5 domain	J134	1.2 V, 1.8 V, 2.5 V, 3.3 V
REG_VBATT	VBATT power domain	J143	2.5 V, 3.3 V, 5 V
CVDDQ	Crystal power domain	J135	1.8 V, 3.3 V

2.1.2 USB Receptacle

A standard Micro B receptacle is used on the FX3 DVK board. VBUS power also comes from the host through this connector. The USB3.0 and USB2.0 lines go through an ESD protection device for additional ESD protection.

Figure 2-2. USB3.0 Micro B Connector and ESD Device



2.1.3 Crystal Oscillator

The clock for the FX3 device is provided through an on-board 19.2 MHz crystal that is connected to the XTALIN and XTALOUT pins of FX3. The FSLC[2:0] lines of FX3 are tied to ground; this means that the device is configured to only use the 19.2 MHz crystal for clocking.

Figure 2-3. Crystal Circuit

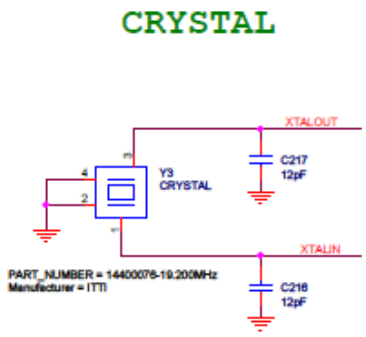
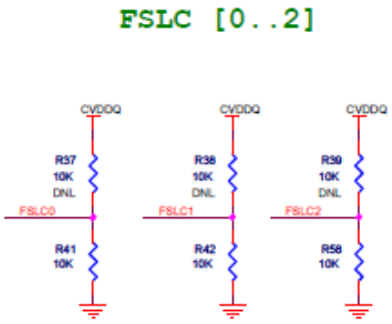


Figure 2-4. FSLC [2:0] Lines Pulled to Ground



Note Pull-up resistors are not loaded on the board.

2.1.4 GPIF II Connector

FX3 offers a high-performance general programmable interface, GPIF II. This interface enables functionality similar to but more advanced than FX2LP's GPIF. The GPIF II is a programmable state machine that enables a flexible interface, which functions either as a master or slave in industry standard or proprietary interfaces. Both parallel and serial interfaces are implemented with GPIF II.

The DVK board consists of a samtec expansion connector to interface with external processors, ASICs, DSPs, or FPGAs. The GPIF II lines going out to the samtec connector also come out on a mictor for probing purposes.

The following figures show the samtec expansion connector with GPIF II signals.

Figure 2-5. Samtec Expansion Connector Circuit 1

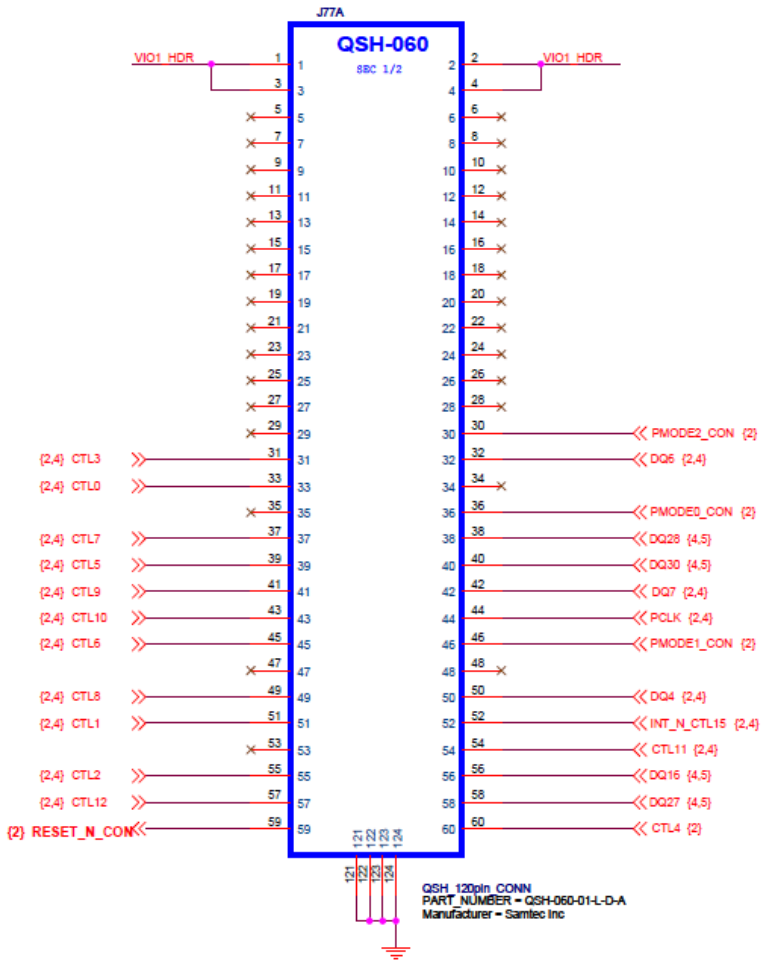
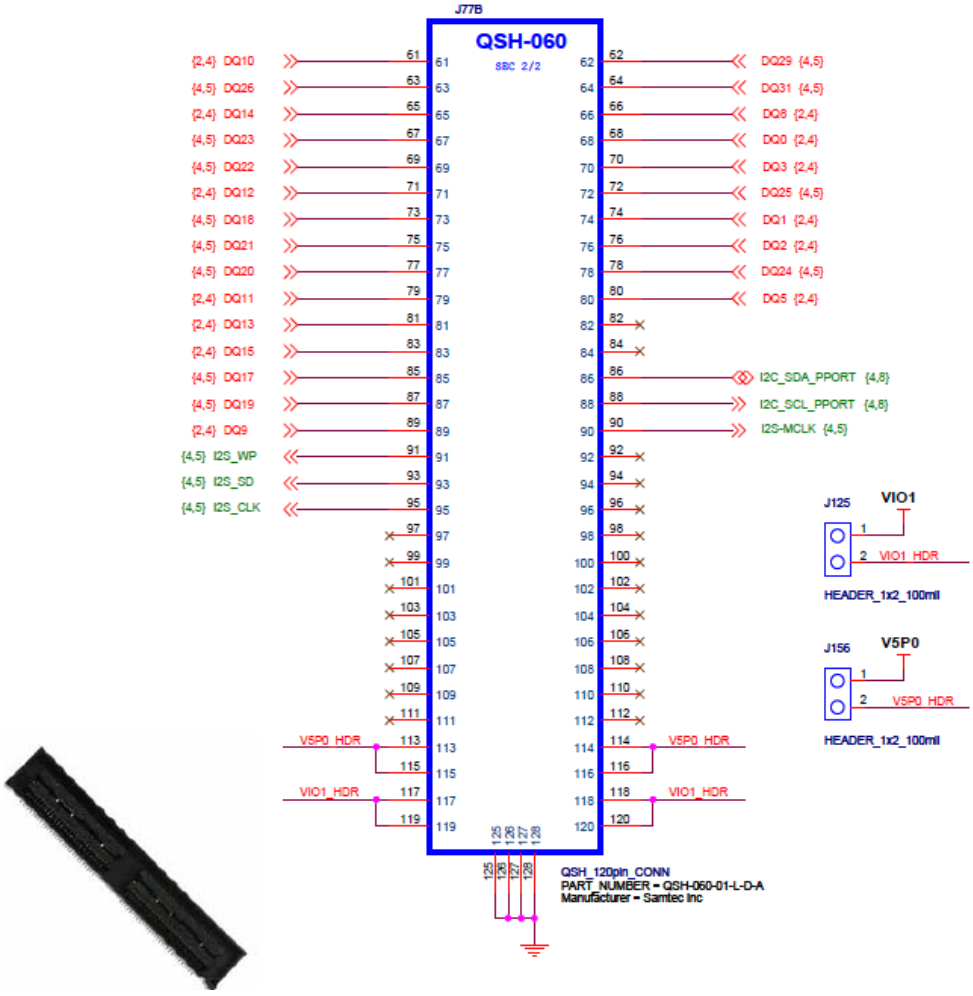


Figure 2-6. Samtec Expansion Connector Circuit 2



The following table shows the pinout of the GPIF II interface on the samtec expansion connector.

Table 2-2. FX3 GPIF II Signal Pinout on Samtec Connector

Connector J77 Pin Nos.	FX3 Signals	GPI/O
68	D0	p_gpio[0]
74	D1	p_gpio[1]
76	D2	p_gpio[2]
70	D3	p_gpio[3]
50	D4	p_gpio[4]
80	D5	p_gpio[5]
32	D6	p_gpio[6]
42	D7	p_gpio[7]
66	D8	p_gpio[8]
89	D9	p_gpio[9]
61	D10	p_gpio[10]
79	D11	p_gpio[11]
71	D12	p_gpio[12]

Connector J77 Pin Nos.	FX3 Signals	GPI/O
81	D13	p_gpio[13]
65	D14	p_gpio[14]
83	D15	p_gpio[15]
44	CLK	p_gpio[16]
33	CTL0	p_gpio[17]
51	CTL1	p_gpio[18]
55	CTL2	p_gpio[19]
31	CTL3	p_gpio[20]
60	CTL4	p_gpio[21]
39	CTL5	p_gpio[22]
45	CTL6	p_gpio[23]
37	CTL7	p_gpio[24]
49	CTL8	p_gpio[25]
41	CTL9	p_gpio[26]
43	CTL10	p_gpio[27]
54	CTL11	p_gpio[28]
57	CTL12	p_gpio[29]
36	PMODE0	p_gpio[30]
46	PMODE1	p_gpio[31]
30	PMODE2	p_gpio[32]
52	INT	int#
59	RESET	reset#
56	D16	s0_gpio[33]
85	D17	s0_gpio[34]
73	D18	s0_gpio[35]
87	D19	s0_gpio[36]
77	D20	s0_gpio[37]
75	D21	s0_gpio[38]
69	D22	s0_gpio[39]
67	D23	s0_gpio[40]
78	D24	s0_gpio[41]
72	D25	s0_gpio[42]
63	D26	s0_gpio[43]
58	D27	s0_gpio[44]
38	D28_UART-RTS	s1_gpio[46]
62	D29_UART-CTS	s1_gpio[47]
40	D30_UART-TX	s1_gpio[48]
64	D31_UART-RX	s1_gpio[49]
95	I2S-CLK	s1_gpio[50]
93	I2S-SD	s1_gpio[51]
91	I2S-WS	s1_gpio[52]
90	I2S-MCLK	L_gpio[57]
88	I2C-SCL	i2c_gpio[58]
86	I2C-SDA	i2c_gpio[59]

As shown in Figure 2-5, J125 can be used to enable the VIO1 power going out on the samtec connector, if populated. Similarly, J156 can be used to enable the 5 V power going out on the samtec connector, if populated.

The CTRL_4 line on the GPIF II interface is also used to enable or disable the on-board USB switch for OTG power. This selection can be made on J100. Figure 2-7 shows how the selection for CTRL_4 is made.

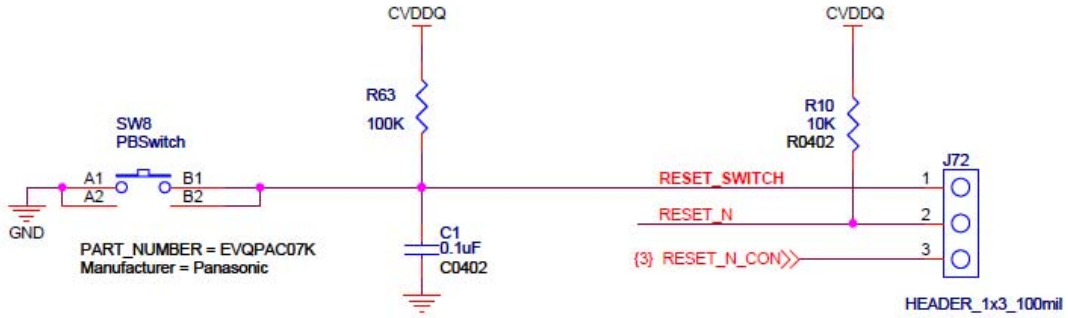
Figure 2-7. CTRL_4 Selection Jumper

As shown in Figure 2-5, if 1 and 2 are connected on J100 through a jumper, the CTRL_4 line goes to the GPIF II interface on the samtec connector. If 2 and 3 are connected, the CTRL_4 line routes to the USB switch for OTG power control.

2.1.5 Reset Circuit

The FX3 device can either be reset from the external processor hooked up to the samtec connector or from an on-board push button. This selection can be made on J72; see Figure 2-8.

Figure 2-8. Reset Circuit and Selection Headers

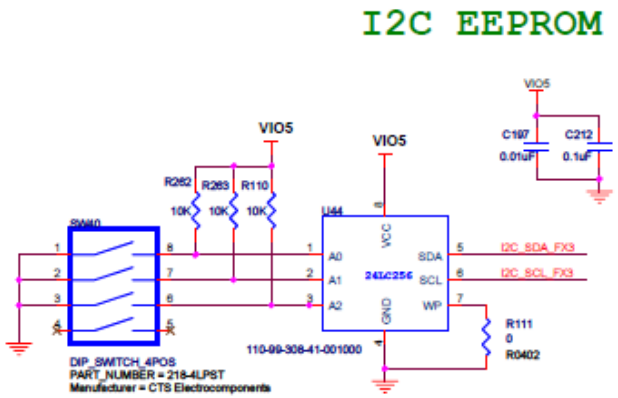


Based on the selection made on J72, either this reset signal goes to the FX3 device (pins 1 and 2 connected on J72) or a signal from the external processor resets the FX3 device (pins 2 and 3 connected on J72).

2.1.6 I2C Interface

The I2C interface lines on the FX3 device come out to headers for probing and expansion, and also connect to an on-board EEPROM device. The EEPROM address bits A2, A1, and A0 can be set using the on-board dip switches on SW40.

Figure 2-9. EEPROM and Address Selection Switches



If the bit is set towards the 'ON' text on SW40, that particular line is connected to ground. This makes the corresponding line to be grounded. If the bit is set towards the numeric text (away from the 'ON' text) on SW40, the corresponding line is pulled high to VIO5.

2.1.7 Booting Options

EZ-USB FX3 can load boot images from various sources selected by the configuration of the PMODE pins. The boot options for FX3 are as follows:

- Boot from USB
- Boot from I2C
- Boot from GPIF II Async ADMUX mode
- Boot from GPIF II Sync ADMUX mode
- Boot from GPIF II Asynch SRAM mode

The following table shows the different booting options for the FX3 device based on the setting of the PMODE pins:

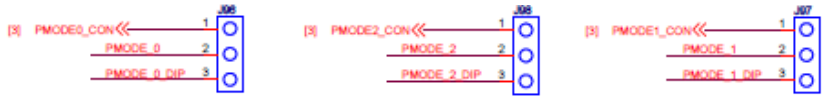
Table 2-3. PMODE Signal Settings for Different FX3 Booting Options

PMODE [2:0]	Boot from
F00	Sync ADMUX (16-bit)
F01	Async ADMUX (16-bit)
F11	USB boot
F0F	Async SRAM (16-bit)
F1F	I2C; on failure, USB boot is enabled
1FF	I2C only
0F1	SPI; on failure, USB boot is enabled

Note F = floating

The FX3 device can boot from the EEPROM connected to its I2C interface. To enable I2C EEPROM boot, the PMODE [2:0] signals need to be set based on Table 2-3. A brief description on how to set the PMODE [2:0] signals is given here.

Figure 2-10. PMODE [2:0] Signal Selection



Headers J96, J97, and J98 are used to select whether the PMODE [2:0] signals are set externally (from the external processor) or on the board. PMODE_0, PMODE_1, and PMODE_2 on the FX3 device are connected to pin 2 of each header, J96, J97, and J98. Place a jumper on 1 and 2 to control the PMODE signals from the external processor, or on 2 and 3 to control the PMODE signals from the dip switch SW25 on the board.

The PMODE [2:0] signals can be set either from the external processor or from the on-board dip switch.

If the PMODE [2:0] signals are set to F1F or 1FF, the FX3 device will boot from the EEPROM connected to the I2C interface. The EEPROM must contain the correct boot data for the FX3 device to boot from it.

The PMODE [2:0] signals can be set on the dip switch SW25 as shown in Figure 2-11.

Figure 2-11. PMODE [2:0] Selection Dip Switches

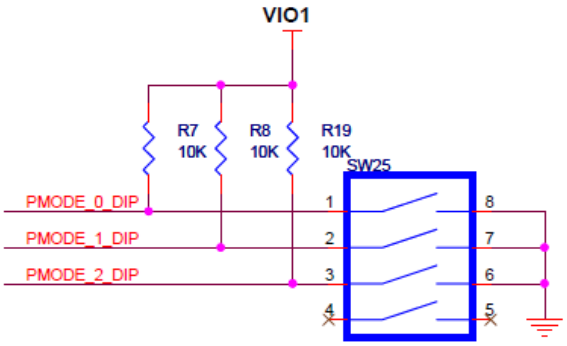


Figure 2-12. Dip Switch

If the bit is set towards the 'ON' text, the corresponding signal line is connected to ground. If the bit is set towards the numeric text (away from the 'ON' text), the corresponding signal line is pulled high to VIO1.

2.1.8 Low Performance Peripherals (LPP)

EZ-USB FX3 consists of the following low performance peripherals:

- JTAG
- I2S
- SPI and UART

2.1.8.1 JTAG

FX3's JTAG interface provides a standard five-pin interface for connecting to a JTAG debugger. This enables to debug the firmware through the CPU core's on-chip debug circuitry. Industry standard debugging tools for the ARM926E-J-S core can be used for FX3 application development. The JTAG pins of FX3 come out on J51. See the SDK documentation for details on the debugger.

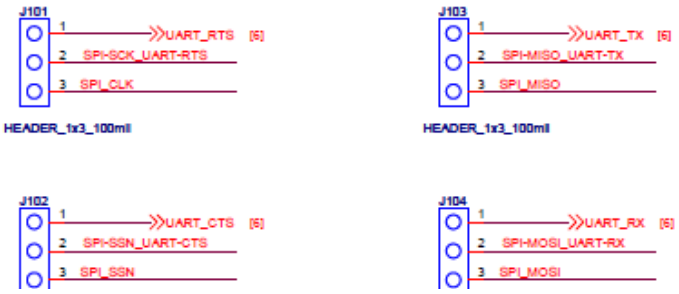
2.1.8.2 I2S

EZ-USB FX3 has an I2S port to support external audio codec devices. FX3 functions as an I2S master (transmitter only). The I2S interface consists of four signals: clock line (I2S_CLK), serial data line (I2S_SD), word select line (I2S_WS), and master system clock (I2S_MCLK). FX3 can generate the system clock as an output on the I2S_MCLK line or accept an external system clock input on the same line. All four I2S lines come out on header J20.

2.1.8.3 SPI and UART

EZ-USB FX3 supports an SPI master interface on the serial peripherals port. The SPI GPIOs are shared with the UART GPIOs on the FX3 device. Even though the data sheet shows that SPI and UART can be used simultaneously in a non 32-bit data path situation, the FX3 DVK design does not allow that. Selection between UART and SPI is made on the board to be able to use either the SPI interface or the UART interface.

Figure 2-13. SPI/UART Selection Headers



If 1 and 2 are shorted on J101, J102, J103, and J104, then the FX3 device will be connected to an RS-232 connector for UART operation. If 2 and 3 are shorted on these four jumpers, the SPI interface of FX3 will come out to J34 only. In this case, the RS-232 connector is disconnected from the FX3 device.