

# SMV512K32-CVAL SRAM Breakout Evaluation Board

This document outlines the basic steps and functions that are required to ensure proper operation of the SMV512K32-CVAL breakout evaluation board. It works in tandem with a customers' pattern generation and capture hardware to demonstrate the memory function features of the 16-Mbit asynchronous SRAM memory.

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### 1 Overview

The SMV512K32-SP 16-Mbit asynchronous SRAM is a QML Class-V Radiation-Hardened memory co-developed with Silicon Space Technology corporation. The HARDSIL<sup>™</sup> radiation hardening technology is an expansion optimization of the radiation performance window by tweaking the processing technology of the circuit design with the layout of the device. The HARDSIL<sup>™</sup> technology provides superior radiation performance with no SWAP (size, weight and power) tradeoffs.

This ultra high performance asynchronous SRAM is functionally com patible with commercial SRAMs and is organized as 512K Words by 32 Bits and has 20ns Read, 13.8ns Write maximum access times. Since it is an Asynchronous Memory, it never needs a clock to refresh the memory and only Reads, Writes, ChipSelect Address, and Data need to be exercised at any given time.

The memory boasts the industries lowest Standby Current ( $I_{SB}$ ) of 200µA which enables the lowest power consumption for Space-grade SRAMs enabling significant system-level power savings.



Figure 1 shows the SMV512K32-SP block diagram of key elements.



The device is pin selectable between Master and Slave modes, and Master-mode provides users with built-in a user defined autonomous Error-Detection-And-Control (or EDAC) for detecting a single bit error from a radiation strike in the device. The built-in "Scrub" engine is included for autonomous cleansing of Single-Event-Errors and avoids multiple errors and a permanent uncorrectable "Multiple-Bit-Error". The combination of the EDAC and Scrub delivers Soft-Error-Rates (SER) < 5e<sup>-17</sup> upsets per bit-day. This is the lowest architecture and power overhead for autonomous Soft-Error mitigation.

The SRAM is Latch up immunity > Linear Energy Transfer (LET) of 110 MeV-cm2/mg which ensures reliable memory data integrity under harshest conditions (T=125°C).

It has a three-state bidirectional data bus and has CMOS compatible Input and Output levels. The Core is powered with a  $1.8V \pm 0.15V$  CORE and the I/O's with a  $3.3V \pm 0.3V$  supply.

The SMV512K32-SP device is offered in a 76-pin Ceramic QFP package, which is shown in Figure 2 below.





Figure 2. SMV512K32-SP 76-Pin QFP (HFG) Package

# 2 Hardware Description

The SMV512K32-CVAL breakout-board utilizes a board utilizes an ENPLAS OTQ-132-0.635-01 socket, which is shown in Figure 3 below.



Figure 3. SMV512K32-CVAL ENPLAS Socket

Access to signals is provided in each quadrant with a three row 100mil standard header. This allows connection to static value, or to a signal generator or capture equipment. The traces are routed with matched length.

Please reference the SMV512K32-SP data sheet (<u>SLVSA21</u>) for proper device operation and power supply connections.



## 3 Device Insertion

For proper SMV512K32-CVAL breakout-board operation, the 76-pin HFG package must be inserted into the socket carefully with the correct orientation. See highlighted red dots in figure 3 for correct orientation. The device has small gold circle embedded into the ceramic in one corner. The socket has an embossed triangle.

To insert the device, place device with correct orientation in the socket. When properly aligned, press down on all four corners of the socket frame to allow cantilever pins to expand and allow device to seat and be captured properly.

## 4 Schematics

## 4.1 Element Schematics

The schematic for the SMV512K32-CVAL breakout-board is shown on the following page in Figure 4.









Schematics

# 4.2 Printed-Circuit-Board Layout Schematics

The layout schematics for the SMV512K32-CVAL breakout-board are shown below for the six-layer PCB in Figure 5 through Figure 10.



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Figure 5. PCB Layout Layer 1





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Figure 6. PCB Layout Layer 2





Figure 7. PCB Layout Layer 3





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Figure 8. PCB Layout Layer 4





Figure 9. PCB Layout Layer 5





Figure 10. PCB Layout Layer 6



EVM Connectors

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## 5 EVM Connectors

## 5.1 Description

The SMV512K3EVM is shown below in Figure 11 below.



Figure 11. SMV512K32-CVAL

To provide the user with simple access and maximum flexibility, the SMV512K32-CVAL has four sets of 3-row 16-pin input/output connectors. These are labeled J1 through J4 and J13 through J20. They provide all of the Input and Output signals for the device.

There are also eight additional Power and Ground banana jack connectors designated as J5 through J12. The power supply is capable of 800 mA for VDD1, and 300 ma for VDD2. Current clamp levels can be greatly reduced with lower operating frequencies. See device datasheet electrical characteristics IDD1, and IDD2 parameters.

The SMV512K32-CVAL connector descriptions are listed in Table 1 below:

REFERENCE DESIGNATOR	FUNCTION
J1	Address Inputs 11 through 16, E1Z, GZ, E2, SCRUBZ, BUSYZ, MBE, MSSEL
J2	DQ0 through DQ15 Data I/O's
J3	Address Inputs A0 through A10, A17, A18, WZ
J4	DQ16 through DQ31 Data I/O's
J5	VDD1 1.8V Power Supply
J6	VDD1 SENSE
J7	GND
J8	GND SENSE
J9	GND SENSE
J10	GND
J11	VDD2 3.3V Power Supply
J12	VDD2 SENSE
J13	GND
J14	VDD2
J15	GND
J16	VDD2
J17	GND
J18	VDD2
J19	GND
J20	VDD2

## Table 1. SMV512K32-CVAL Connector Descriptions

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#### **EVM Warnings and Restrictions**

It is important to operate this EVM within the input voltage range of -0.3 V to 2 V (VDD1), -0.3 V to 3.8 V (VDD2) and the output voltage range of -0.3 V to 3.8 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 40°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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