DS91M047 125 MHz Quad M-LVDS Line Driver



Literature Number: SNLS145D



DS91M047 125 MHz Quad M-LVDS Line Driver

# 125 MHz Quad M-LVDS Line Driver

### **General Description**

The DS91M047 is a high-speed quad M-LVDS line driver designed for driving clock or data signals to up to four multipoint networks.

M-LVDS (Multipoint LVDS) is a new family of bus interface devices based on LVDS technology specifically designed for multipoint and multidrop cable and backplane applications. It differs from standard LVDS in providing increased drive current to handle double terminations that are required in multipoint applications. Controlled transition times minimize reflections that are common in multipoint configurations due to unterminated stubs.

The DS91M047 accepts LVTTL/LVCMOS input levels and translates them to M-LVDS signal levels with transition times of greater than 1 ns. The device provides the DE and  $\overline{DE}$  inputs that are ANDed together and control the TRI-STATE outputs. The DE and  $\overline{DE}$  inputs are common to all four drivers.

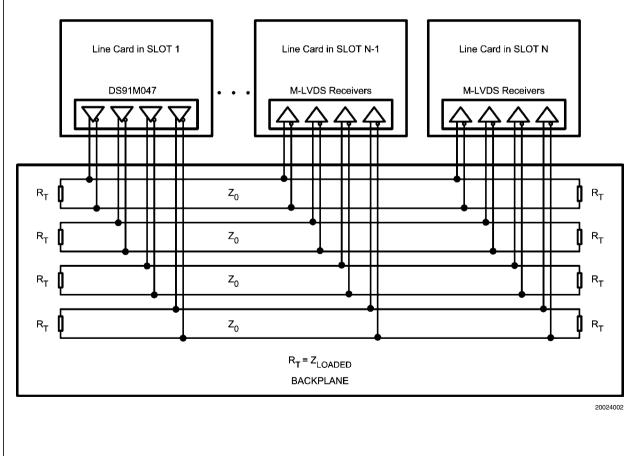
The DS91M047 has a flow-through pinout for easy PCB layout. The DS91M047 provides a new alternative for high speed multipoint interface applications. It is packaged in a space saving SOIC-16 package.

### **Features**

- DC 125 MHz / 250 Mbps low jitter, low skew, low power operation
- Conforms to TIA/EIA-899 M-LVDS Standard
- Controlled transition times (2 ns typ) minimize reflections
- 8 kV ESD on M-LVDS pins protects adjoining components
- Flow-through pinout simplifies PCB layout
- Industrial operating temperature range (-40°C to +85°C)
- Available in a space saving SOIC-16 package

### **Applications**

- Multidrop / Multipoint clock and data distribution
- High-Speed, Low Power, Short-Reach alternative to TIA/EIA-485/422
- Clock distribution in AdvancedTCA (ATCA) and MicroTCA (µTCA, uTCA) backplanes

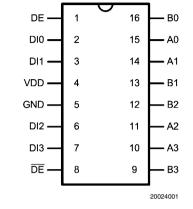


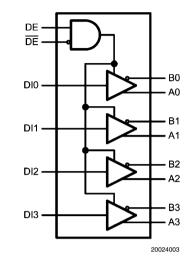
**Typical Application** 

## **Ordering Information**

[	Operating Temperature	Package Type / Number	Order Number
	-40°C to +85°C	SOIC/M16A	DS91M047TMA

## **Connection Diagrams**





## **Pin Descriptions**

Pin No.	Name	Description
2, 3, 6, 7	DI	Driver input pin, LVCMOS compatible.
10, 11, 14, 15	А	Non-inverting driver output pin, M-LVDS levels.
9, 12, 13, 16	В	Inverting driver output pin, M-LVDS levels.
1	DE	Driver enable pin: When DE is low, the driver is disabled. When DE is high and $\overline{DE}$ is low or open, the driver is enabled. If both DE and $\overline{DE}$ are open circuit, then the driver is disabled.
8	DE	Driver enable pin: When $\overline{DE}$ is high, the driver is disabled. When $\overline{DE}$ is low or open and DE is high, the driver is enabled. If both DE and $\overline{DE}$ are open circuit, then the driver is disabled.
4	V <sub>DD</sub>	Power supply pin, $+3.3V \pm 0.3V$
5	GND	Ground pin

### **Truth Table**

Enables		Input	Outputs	
DE	DE	DI	Α	В
Ц	L	L	L	н
		Н	Н	L
All other combinations of ENABLE inputs		Х	Z	Z

### Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage	–0.3V to +4V
LVCMOS Input Voltage	–0.3V to (V <sub>DD</sub> + 0.3V)
M-LVDS Output Voltage	-1.9V to +5.5V
M-LVDS Output Short Circuit Current Duration	Continuous
Junction Temperature	+140°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Diss	ipation @ +25°C
MA Package	2.21W
Derate MA Package	19.2 mW/°C above +25°C
Package Thermal Resistance (4	-Layer, 2 oz. Cu, JEDEC)
$\theta_{JA}$	+52°C/W
θ <sub>JC</sub>	+19°C/W

ESD Susceptibility	
HBM	≥8 kV
MM	≥250V
CDM	≥1250V

Note 1: Human Body Model, applicable std. JESD22-A114C Note 2: Machine Model, applicable std. JESD22-A115-A Note 3: Field Induced Charge Device Model, applicable std. JESD22-C101-C

### Recommended OperatingConditions

	Min	Тур	Max	Units
Supply Voltage (VDD)	+3.0	+3.3	+3.6	V
Voltage at Any Bus Terminal	-1.4		+3.8	V
(Separate or Common-Mode)				
High Level Input Voltage (V <sub>IH</sub> )	2.0		$V_{DD}$	V
Low Level Input Voltage (V <sub>IL</sub> )	0		0.8	V
Operating Free Air				
Temperature (T <sub>A</sub> )	-40	+25	+85	°C

### DC Electrical Characteristics (Note 5, Note 6, Note 7, Note 9)

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
LVCMOS D	OC Specifications					
V <sub>IH</sub>	High-Level Input Voltage		2.0		V <sub>DD</sub>	V
V <sub>IL</sub>	Low-Level Input Voltage		GND		0.8	V
I <sub>IH</sub>	High-Level Input Current	V <sub>IH</sub> = 3.6V	-15	±1	15	μA
I <sub>IL</sub>	Low-Level Input Current	$V_{IL} = 0V$	-15	±1	15	μA
V <sub>CL</sub>	Input Clamp Voltage	I <sub>IN</sub> = -18 mA	-1.5			V
M-LVDS D	C Specifications					
IV <sub>AB</sub> I	Differential Output Voltage Magnitude	- R <sub>1</sub> = 50Ω, C <sub>1</sub> = 5 pF	480		650	mV
$\Delta V_{AB}$	Change in Differential Output Voltage Magnitude Between Logic States	Figures 1, 3	-50		50	mV
V <sub>OS(SS)</sub>	Steady-State Common-Mode Output Voltage	- Figures 1, 2	0.30	1.6	2.10	V
ΔV <sub>OS(SS)</sub>	Change in Steady-State Common-Mode Output Voltage Between Logic States	$R_L = 50\Omega$	0		50	mV
V <sub>A(OC)</sub>	Maximum Steady-State Open-Circuit Output Voltage	Einung (	0		2.4	V
V <sub>B(OC)</sub>	Maximum Steady-State Open-Circuit Output Voltage	- Figure 4	0		2.4	V
V <sub>P(H)</sub>	Voltage Overshoot, Low-to-High Level Output (Note 10)	$R_L = 50\Omega, C_L = 5 \text{ pF}$ $C_D = 0.5 \text{ pF}, \text{ Figures 6, 7}$			1.2V <sub>SS</sub>	V
V <sub>P(L)</sub>	Voltage Overshoot, High-to-Low Level Output (Note 10)		-0.2V <sub>SS</sub>			V
I <sub>os</sub>	Output Short-Circuit Current (Note 8)	Figure 5	-43		43	mA
		$V_{A} = 3.8V, V_{B} = 1.2V$	0		32	μA
I <sub>A</sub>	Driver High-Impedance Output Current	$V_{\rm A} = 0$ V or 2.4V, $V_{\rm B} = 1.2$ V	-20		20	μA
		$V_{A} = -1.4V, V_{B} = 1.2V$	-32		0	μA
		V <sub>A</sub> = 3.8V, V <sub>B</sub> = 1.2V	0		32	μA
B	Driver High-Impedance Output Current	$V_{\rm A} = 0$ V or 2.4V, $V_{\rm B} = 1.2$ V	-20		20	μA
		$V_{A} = -1.4V, V_{B} = 1.2V$	-32		0	μA
I <sub>AB</sub>	Driver High-Impedance Output Differential Curent $(I_A - I_B)$	$V_{A} = V_{B}, -1.4V \le V \le 3.8V$	-4		4	μA

Symbol	Parameter	Conditions	Min	Тур	Max	Units
I <sub>A(OFF)</sub>	Driver High-Impedance Output Power-Off Current	V <sub>A</sub> = 3.8V, V <sub>B</sub> = 1.2V				μA
		DE = 0V	0		32	
		$0V \le V_{DD} \le 1.5V$				
		$V_{A} = 0V \text{ or } 2.4V, V_{B} = 1.2V$				μA
		DE = 0V	-20		20	
		$0V \le V_{DD} \le 1.5V$				
		$V_{A} = -1.4V, V_{B} = 1.2V$				μA
		DE = 0V	-32		0	
		$0V \le V_{DD} \le 1.5V$				
I <sub>B(OFF)</sub>	Driver High-Impedance Output Power-Off Current	$V_{A} = 3.8V, V_{B} = 1.2V$				μA
		DE = OV	0		32	
		$0V \le V_{DD} \le 1.5V$				
		$V_{A} = 0V \text{ or } 2.4V, V_{B} = 1.2V$				μA
		DE = 0V	-20		20	
		$0V \le V_{DD} \le 1.5V$				
		$V_{A} = -1.4V, V_{B} = 1.2V$				μA
		DE = 0V	-32		0	
		$0V \le V_{DD} \le 1.5V$				
I <sub>AB(OFF)</sub>	Driver High-Impedance Output Power-Off Current	$V_{A} = V_{B}, -1.4V \le V \le 3.8V$				μA
	$(I_{A(OFF)} - I_{B(OFF)})$	DE = 0V	-4		4	
		$0V \le V_{DD} \le 1.5V$				<u> </u>
C <sub>A</sub>	Driver Output Capacitance			7.8		pF
C <sub>B</sub>	Driver Output Capacitance	$-V_{DD} = 0V$		7.8		pF
C <sub>AB</sub>	Driver Output Differential Capacitance			3		pF
C <sub>A/B</sub>	Driver Output Capacitance Balance (C <sub>A</sub> /C <sub>B</sub> )			1		
I <sub>CC</sub>	Power Supply Current	$R_L = 50\Omega$ (All Outputs)				
		$DI = V_{DD}$ or GND (All Inputs)		65	75	mA
		$DE = V_{DD}, \overline{DE} = GND$				
		f = 125 MHz				
I <sub>CCZ</sub>	TRI-STATE Power Supply Current	$R_{L} = 50\Omega$ (All Outputs)				
		$DI = V_{DD}$ or GND (All Inputs)		19	24	mA
		$DE = GND, \overline{DE} = V_{DD}$				

Note 4: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 5: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 6: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except  $V_{OD}$  and  $\Delta V_{OD}$ .

Note 7: Typical values represent most likely parametric norms for  $V_{DD}$  = +3.3V and  $T_A$  = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 8: Output short circuit current ( $I_{OS}$ ) is specified as magnitude only, minus sign indicates direction only.

Note 9:  $C_L$  includes fixture capacitance and  $C_D$  includes probe capacitance.

Note 10: Specification is guaranteed by characterization and is not tested in production.

### Switching Characteristics (Note 11, Note 12, Note 18)

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
t <sub>PHL</sub>	Differential Propagation Delay High to Low		1.5	3.1	5.0	ns
t <sub>PLH</sub>	Differential Propagation Delay Low to High		1.5	3.1	5.0	ns
t <sub>SKD1</sub>	Differential Pulse Skew It <sub>PHL</sub> - t <sub>PLH</sub> I (Note 13, Note 14)		0	70	140	ps
t <sub>SKD2</sub>	Channel-to-Channel Skew (Note 13, Note 15)	$R_{L} = 50\Omega$	0	70	200	ps
t <sub>SKD3</sub>	Differential Part-to-Part Skew ( <i>Note 13, Note 16</i> ) (Constant $T_A$ and $V_{DD}$ )	$-C_L = 5 \text{ pF},$ $C_D = 0.5 \text{ pF}$	0	0.8	1.5	ns
t <sub>SKD4</sub>	Differential Part-to-Part Skew (Note 17)	– Figures 6, 7	0		3.5	ns
t <sub>TLH</sub>	Rise Time ( <i>Note 13</i> )		1.1	2.0	3.0	ns
t <sub>THL</sub>	Fall Time ( <i>Note 13</i> )		1.1	2.0	3.0	ns
t <sub>PHZ</sub>	Disable Time High to Z	R <sub>1</sub> = 50Ω		7	12.5	ns
t <sub>PLZ</sub>	Disable Time Low to Z	$C_{L} = 5 \text{ pF},$		7	12.5	ns
t <sub>PZH</sub>	Enable Time Z to High	C <sub>D</sub> = 0.5 pF		7	12.5	ns
t <sub>PZL</sub>	Enable Time Z to Low	Figures 8, 9		7	12.5	ns
f <sub>MAX</sub>	Maximum Operating Frequency	(Note 13)	125			MHz

Note 11: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 12: Typical values represent most likely parametric norms for  $V_{DD}$  = +3.3V and  $T_A$  = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 13: Specification is guaranteed by characterization and is not tested in production.

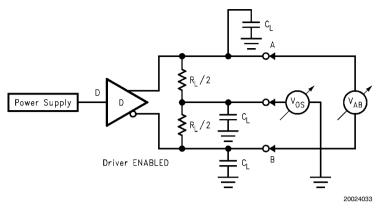
Note 14:  $t_{SKD1}$ ,  $lt_{PLHD} - t_{PHLD}$ , Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

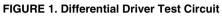
Note 15:  $t_{SKD2}$ , Channel-to-Channel Skew, is the difference in propagation delay ( $t_{PLHD}$  or  $t_{PHLD}$ ) among all output channels.

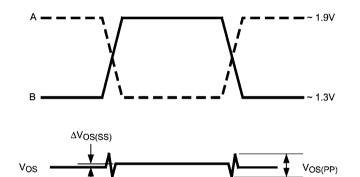
Note 16: t<sub>SKD3</sub>, Part-to-Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V<sub>DD</sub> and within 5°C of each other within the operating temperature range.

**Note 17:**  $t_{SKD4}$ , Part-to-Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution.  $t_{SKD4}$  is defined as IMax – Minl differential propagation delay. **Note 18:**  $C_1$  includes fixture capacitance and  $C_n$  includes probe capacitance.

### **Parameter Measurement Information**









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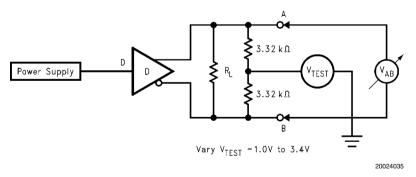


FIGURE 3. Differential Driver Full Load Test Circuit

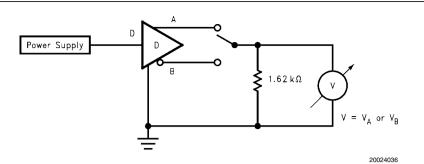
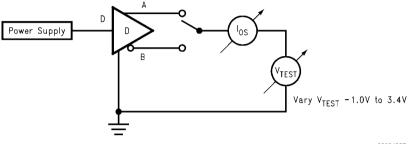


FIGURE 4. Differential Driver DC Open Test Circuit



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FIGURE 5. Differential Driver Short-Circuit Test Circuit

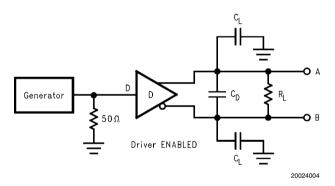


FIGURE 6. Driver Propagation Delay and Transition Time Test Circuit

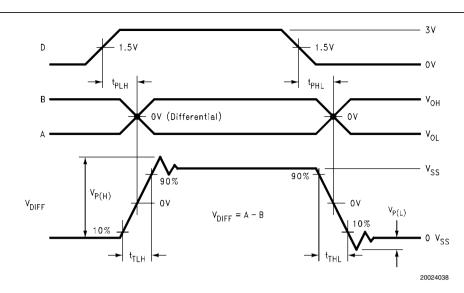
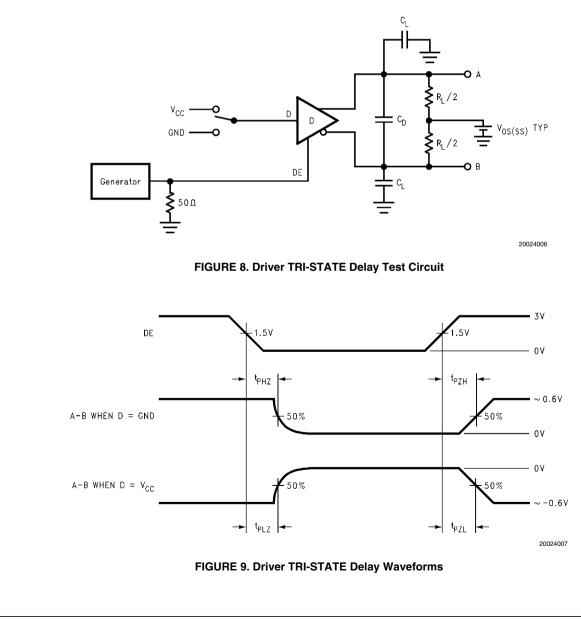
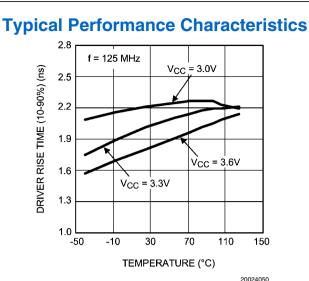
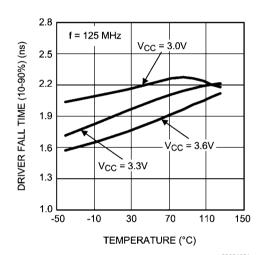


FIGURE 7. Driver Propagation Delay and Transition Time Waveforms

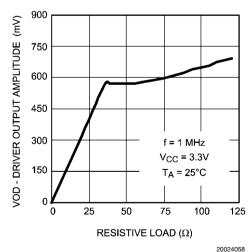




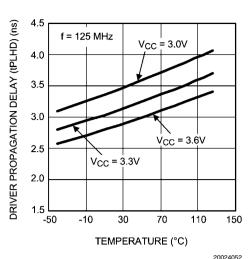
Driver Rise Time as a Function of Temperature



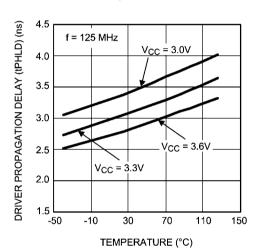
Driver Fall Time as a Function of Temperature



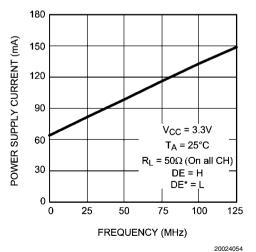
Driver Output Signal Amplitude as a Function of Resistive Load



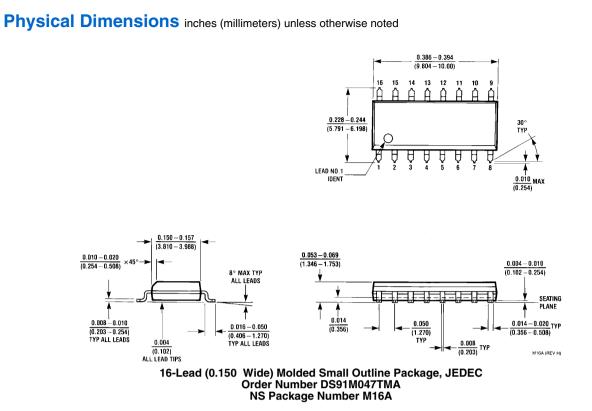
Driver Propagation Delay (tPLHD) as a Function of Temperature



Driver Propagation Delay (tPHLD) as a Function of Temperature



Driver Power Supply Current as a Function of Frequency



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# Notes

DS91M047

# Notes

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Ŋ	Amplifiers
	Audio
Σ	Clock and Tim
ad	Data Converte
n a	Interface
Q	LVDS
P	Power Manage
Σ	Switching
2	LDOs
12	LED Light
~	Voltage R
4	PowerWise® \$
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