DS64BR401 Quad Bi-Directional Repeater with Equalization and De-Emphasis



Literature Number: SNLS304F

# Quad Bi-Directional Repeater with Equalization and De-Emphasis

# **General Description**

The DS64BR401 is a quad lane bi-directional signal conditioning repeater for 6.0/3.0/1.5 Gbps SATA/SAS and other high-speed bus applications with data rates up to 6.4 Gbps. The device performs both receive equalization and transmit de-emphasis on each of its 8 channels to compensate for channel loss, allowing maximum flexibility of physical placement within a system. The receiver's continuous time linear equalizer (CTLE) provides a boost of up to +33 dB at 3 GHz and is capable of opening an input eye that is completely closed due to inter-symbol interference (ISI) induced by the interconnect medium. The transmitter features a programmable output de-emphasis driver and allows amplitude voltage levels to be selected from 600 mVp-p to 1200 mVp-p to suit multiple application scenarios. This Low Power Differential Signaling (LPDS) output driver is a power efficient implementation that maintains compatibility with AC coupled CML receiver. The programmable settings can be applied via pin settings or SMBus interface.

To enable seamless upgrade from SAS/SATA 3.0 Gbps to 6.0 Gbps data rates without compromising physical reach, DS64BR401 automatically detects the incoming data rate and selects the optimal de-emphasis pulse width. The device detects the out-of-band (OOB) idle and active signals of the SAS/SATA specification and passes through with minimum signal distortion.

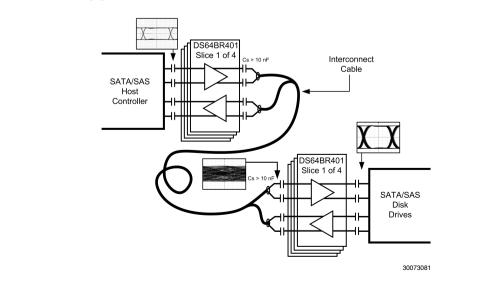
With a typical power consumption of 200 mW/lane (100 mW/ channel) at 6.4 Gbps, and control to turn-off unused channels, the DS64BR401 is part of National's PowerWise family of energy efficient devices.

# **Features**

- Quad lane bi-directional repeater up to 6.4 Gbps rate
- Signal conditioning on input and output for extended reach
- Adjustable receive equalization up to +33 dB gain
- Adjustable transmit de-emphasis up to −12 dB
- Adjustable transmit VOD (600 mVp-p to 1200 mVp-p)
- <0.25 UI of residual DJ at 6.4 Gbps with 40" FR4 trace</p>
- Automatic de-emphasis scaling based on rate detect
- SATA/SAS: OOB signal pass-through,
   <3 ns (typ) envelope distortion</li>
- Adjustable electrical IDLE detect threshold
- Low power (100 mW/channel), per-channel power down
- Programmable via pin selection or SMBus interface
- Single supply operation at 2.5V ±5%
- >6 kV HBM ESD Rating
- 3.3V LVCMOS input tolerant for SMBus interface
- High speed signal flow-thru pinout package: 54-pin LLP (10 mm x 5.5 mm)

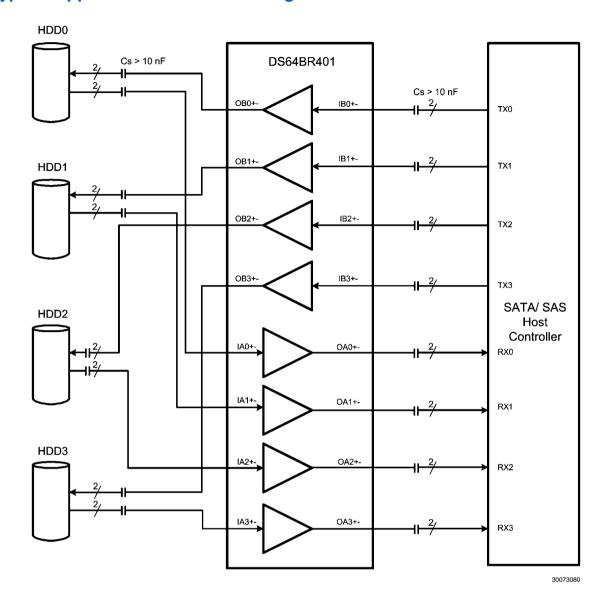
## **Applications**

- SATA (1.5, 3.0 and 6 Gbps)
- SAS (1.5, 3.0 and 6 Gbps)
- XAUI (3.125 Gbps), RXAUI (6.25 Gbps)
- sRIO Serial Rapid I/O
- Fibre Channel (4.25 Gbps)
- 10GBase-CX4, InfiniBand 4x (SDR & DDR)
- QSFP active copper cable modules
- High-speed active cable and FR-4 backplane traces

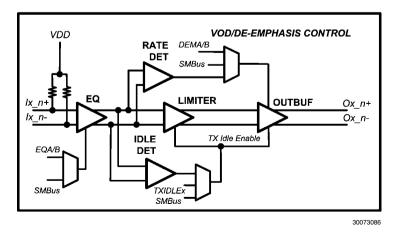


© 2010 National Semiconductor Corporation

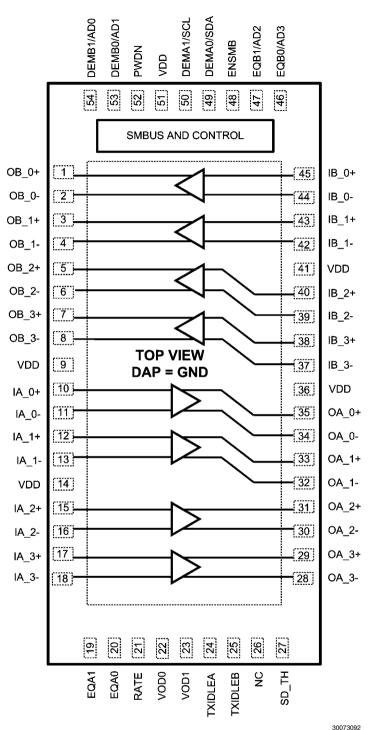
# **Typical Application Connection Diagram**



# Block Diagram - Detail View of the Each Channel (1 of 8)



**Pin Diagram** 



**DS64BR401** 

DS64BR401 Pin Diagram 54L LLP

# **Ordering Information**

NSID	Qty	Spec	Package
DS64BR401SQ	Tape & Reel Supplied As 2,000 Units	NOPB	SQA54A
DS64BR401SQE	Tape & Reel Supplied As 250 Units	NOPB	SQA54A

# **Pin Descriptions**

Pin Name	Pin Number	I/O, Type	Pin Descriptions
Differential High S	peed I/O's		
IA_0+, IA_0- ,	10, 11	I, CML	Inverting and non-inverting CML differential inputs to the
IA_1+, IA_1-,	12, 13		equalizer. A gated on-chip $50\Omega$ termination resistor connects
IA_2+, IA_2-,	15, 16		INA_n+ to VDD and INA_n- to VDD when enabled.
IA_3+, IA_3-	17, 18		
OA_0+, OA_0-,	35, 34	O, LPDS	Inverting and non-inverting low power differential signaling
OA_1+, OA_1-,	33, 32		(LPDS) 50 $\Omega$ outputs with de-emphasis. Compatible with AC
OA_2+, OA_2-,	31, 30		coupled CML inputs.
OA_3+, OA_3-	29, 28		ter
IB_0+, IB_0- ,	45, 44	I, CML	Inverting and non-inverting CML differential inputs to the
IB_1+, IB_1-,	43, 42		equalizer. A gated on-chip $50\Omega$ termination resistor connects
IB_2+, IB_2-,	40, 39		INB_n+ to VDD and INB_n- to VDD when enabled.
IB_3+, IB_3-	38, 37		
OB_0+, OB_0-,	1,2	O, LPDS	Inverting and non-inverting low power differential signaling
OB_1+, OB_1-,	3, 4	-, -	(LPDS) 50 $\Omega$ outputs with de-emphasis. Compatible with AC
OB_2+, OB_2-,	5, 6		coupled CML inputs.
OB_3+, OB_3-	7, 8		
Control Pins — Sh		I	
ENSMB	48	I, LVCMOS w/	System Management Bus (SMBus) enable pin.
	40	internal pull-	When pulled high provide access internal digital registers that
		down	are a means of auxiliary control for such functions as
			equalization, de-emphasis, VOD, rate, and idle detection
			threshold.
			When pulled low, access to the SMBus registers are disabled
			and SMBus function pins are used to control the Equalizer
			and De-Emphasis.
			Please refer to "SMBus configuration Registers" section and
			Electrical Characteristics - Serial Management Bus Interface
			for detail information.
ENSMB = 1 (SMBU			
SCL	50	I, LVCMOS	ENSMB = 1
JOL	50		SMBUS clock input pin is enabled. External pull-up resistor
			maybe needed. Refer to R <sub>TERM</sub> in the SMBus specification.
SDA	49	I, LVCMOS	ENSMB = 1
		O, Open	The SMBus bi-directional SDA pin is enabled. Data input or
		Drain	open drain output. External pull-up resistor is required.
			Refer to R <sub>TERM</sub> in the SMBus specification.
AD0–AD3	54, 53, 47, 46	I, LVCMOS w/	ENSMB = 1
		internal pull-	SMBus Slave Address Inputs. In SMBus mode, these pins are
		down	the user set SMBus slave address inputs. See section —
			System Management Bus (SMBus) and Configuration
			Registers for additional information.
ENSMB = 0 (NORM	IAL PIN MODE)		
EQA0, EQA1	20, 19	I, Float,	EQA/B, 3-level controls the level of equalization of the A/B
EQB0, EQB1	46, 47	LVCMOS	sides. The EQA/B pins are active only when ENSMB is de-
	, í		asserted (Low). Each of the 4 A/B channels have the same
			level unless controlled by the SMBus control registers. When
			ENSMB goes high the SMBus registers provide independent
			control of each lane. See <i>Table 1</i> , <i>Table 2</i> , <i>Table 3</i>

Pin Name	Pin Number	I/O, Type	Pin Descriptions
DEMA0, DEMA1 DEMB0, DEMB1	49, 50 53, 54	I, Float, LVCMOS	DEMA/B, 3–level controls the level of de-emphasis of the A/ B sides. The DEMA/B pins are only active when ENSMB is de-asserted (Low). Each of the 4 A/B channels have the same level unless controlled by the SMBus control registers. When ENSMB goes High the SMBus registers provide independent control of each lane. See <i>Table 4</i>
Control Pins — Both	Modes (LVCM	DS)	
RATE	21	I, Float, LVCMOS	RATE, 3–level controls the pulse width of de-emphasis of the output. RATE = 0 forces 3 Gbps, RATE = 1 forces 6 Gbps, RATE = Float enables auto rate detection and the pulse widt (pull-back) is set appropriately after each exit from IDLE. Thi requires the transition from IDLE to ACTIVE state — OOB signal. See <i>Table 4</i>
TXIDLEA,TXIDLEB	24, 25	I, Float, LVCMOS	<ul> <li>TXIDLEA/B, 3–level controls the driver output.</li> <li>TXIDLEA/B = 0 disables the signal detect/squelch function fo all A/B outputs.</li> <li>TXIDLEA/B = 1 forces the outputs to be muted (electrical idle)</li> <li>TXIDLEA/B = Float enables the signal auto detect/squelch function and the signal detect voltage threshold level can be adjusted using the SD_TH pin. See <i>Table 5</i></li> </ul>
VOD0, VOD1	22, 23	I, LVCMOS w/ internal pull- down	VOD[1:0] adjusts the output differential amplitude voltage level. VOD[1:0] = 00 sets output VOD = 600 mV (Default) VOD[1:0] = 01 sets output VOD = 800 mV VOD[1:0] = 10 sets output VOD = 1000 mV VOD[1:0] = 11 sets output VOD = 1200 mV
PWDN	52	I, LVCMOS	PWDN = 0 enables the device (normal operation). PWDN = 1 disables the device (low power mode). Pin must be driven to a logic low at all times for normal operation
Analog	-1		
SD_TH	27	I, ANALOG	Threshold select pin for electrical idle detect threshold. Floa pin for typical default 130 mVp-p (differential), otherwise connect resistor from SD_TH to GND to set threshold voltage See <i>Table 6, Figure 5</i>
Power	•	•	
VDD	9, 14, 36, 41, 51	Power	Power supply pins. 2.5 V +/-5%
GND	DAP	Power	DAP is the large metal contact at the bottom side, located a the center of the 54 pin LLP package. It should be connected to the GND plane with at least 4 via to lower the ground impedance and improve the thermal performance of the package.
NC	26		No Connect — Leave pin open

1 = HIGH, 0 = LOW, FLOAT = 3rd input state.

Don't drive FLOAT pin; pin is internally biased to mid level with 50 k $\Omega$  pull-up/pull-down.

Internal pulled-down = Internal 30 k $\Omega$  pull-down resistor to GND is present on the input.

Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (VDD)	-0.5V to +3.0V
LVCMOS Input/Output Voltage	-0.5V to +4.0V
CML Input Voltage	-0.5V to (VDD+0.5V)
LPDS Output Voltage	-0.5V to (VDD+0.5V)
Analog (SD_TH)	-0.5V to (VDD+0.5V)
Junction Temperature	+125°C
Storage Temperature	-40°C to +125°C
Maximum Package Power Dissi	pation at 25°C
SQA54A Package	4.21 W
Derate SQA54A Package	52.6mW/°C above +25°C
ESD Rating HBM, STD - JESD22-A114C MM, STD - JESD22-A115-A	≥6 kV ≥250 V

## CDM, STD - JESD22-C101-C ≥1250 V Thermal Resistance

$\theta_{\text{JC}}$	11.5°C/W
$\theta_{JA}$ , No Airflow, 4 layer JEDEC	19.1°C/W

For soldering specifications: see product folder at www.national.com

www.national.com/ms/MS/MS-SOLDERING.pdf

# Recommended Operating Conditions

	Min	Тур	Max	Units	
Supply Voltage					
VDD to GND	2.375	2.5	2.625	V	
Ambient Temperature	-10	25	+85	°C	
SMBus (SDA, SCL)	0		3.6	V	
CML Differential Input Voltage	0		2.0	Vp-р	
Supply Noise Tolerance up to 50 MHz, ( <i>Note 4</i> )		100		mVp-p	

## **Electrical Characteristics**

Over recommended operating supply and temperature ranges with default register settings unless other specified. (Note 3)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
POWER	•			-		
PD	Power Dissipation	PWDN = 0, EQx = 0, DEMx = 0 dB, K28.5 pattern VOD = 1.0 Vp-p		758	950	mW
		PWDN = 1, ENSMB = 0		0.92	1.125	mW
LVCMOS / LV	TTL DC SPECIFICATIONS		Į	. <u>.</u>		
V <sub>IH</sub>	High Level Input Voltage		2.0		3.6	V
V <sub>IL</sub>	Low Level Input Voltage		0		0.8	V
IIH	Input High Current	V <sub>IN</sub> = 3.3V, Inputs OPEN: SDA, SCL, PWDN	-15		+15	μA
		$V_{IN} = 3.3V$ , Inputs with PULL-DOWN and FLOAT — mid level	-15		+120	uA
I <sub>IL</sub>	Input Low Current	V <sub>IN</sub> = 0V, Inputs OPEN: SDA, SCL, PWDN and with PULL-DOWN	-15		+15	μA
		V <sub>IN</sub> = 0V, Inputs with FLOAT — mid level	-80		+15	uA
CML RECEIV	ER INPUTS (IN_n+, IN_n-)					
RL <sub>RX-DIFF</sub>	Rx Differential Return Loss	150 MHz – 1.5 GHz		-20		
	(SDD11),	150 MHz – 3.0 GHz		-13.5		dB
	( <i>Note 2</i> )	150 MHz – 6.0 GHz		-8		
RL <sub>RX-CM</sub>	Rx Common Mode Input Return Loss (SCC11)	150 MHz – 3.0 GHz, ( <i>Note 2</i> )		-10		dB
R <sub>RX-IB</sub>	Rx Impedance Balance (SDC11)	150 MHz – 3.0 GHz, ( <i>Note 2</i> )		-27		dB
I <sub>IN</sub>	Maximum current allowed at IN+ or IN- input pin.		-30		+30	mA

Symbol	Parameter	Conditions	Min	Тур	Max	Units
R <sub>IN</sub>	Input Resistance	Single ended to V <sub>DD</sub> , ( <i>Note 2</i> )		50		Ω
R <sub>ITD</sub>	Input Differential Impedance between IN+ and IN-	DC tested, ( <i>Note 2</i> )	85	100	115	Ω
R <sub>ITIB</sub>	Input Differential Impedance Imbalance	DC tested, (Note 2)			5	Ω
R <sub>ICM</sub>	Input Common Mode Impedance	DC tested, (Note 2)	20	25	35	Ω
V <sub>RX-DIFF</sub>	Differential Rx peak to peak voltage	DC voltage, SD_TH = 20 k $\Omega$ to GND	0.1		1.2	v
V <sub>RX-SD_TH</sub>	Electrical Idle detect threshold (differential)	SD_TH = Float, ( <i>Note 6</i> ), <i>Figure 5</i>	40		175	mVp-p
LPDS OUTPU	TS (OUT_n+, OUT_n-)					
V <sub>OD</sub>	Output Voltage Swing	$R_{L} = 50 \ \Omega \pm 1\% \text{ to GND (AC coupled with 10} \\ nF), 6.4 \text{ Gbps, (Note 5)} \\ DEMx = 0 \text{ dB,} \\ VOD[1:0] = 00$	500	600	700	mV <sub>P-P</sub>
		VOD[1:0] = 11	1100	1265	1450	mV <sub>P-P</sub>
V <sub>OCM</sub>	Output Common-Mode Voltage	Single-ended measurement DC-Coupled with $50\Omega$ termination, ( <i>Note 2</i> )		V <sub>DD</sub> – 1.4		v
T <sub>TX-RF</sub>	Transmitter Rise/ Fall Time	20% to 80% of differential output voltage, measured within 1" from output pins, ( <i>Note 2, Note 5</i> ), <i>Figure 1</i>		67	85	ps
T <sub>RF-DELTA</sub>	Tx rise/fall mismatch	20% to 80% of differential output voltage, ( <i>Note 2, Note 5</i> )			0.1	UI
RL <sub>TX-DIFF</sub>	Tx Differential Return Loss (SDD22), ( <i>Note 2</i> )	Repeating 1100b (D24.3) pattern, VOD = 1.0 Vp-p, 150 MHz – 1.5 GHz		-11		dB
		150 MHz – 3.0 GHz		-10		
		150 MHz – 6.0 GHz		-5		
RL <sub>TX-CM</sub>	Tx Common Mode Return Loss (SCC22)	Repeating 1100b (D24.3) pattern, VOD = 1.0 Vp-p, ( <i>Note 2</i> ) 50 MHz – 3.0 GHz		-10		dB
R <sub>TX-IB</sub>	Tx Impedance Balance (SDC22)	Repeating 1100b (D24.3) pattern, VOD = 1.0 Vp-p, ( <i>Note 2</i> ) 50 MHz – 3.0 GHz		-30		dB
I <sub>TX-SHORT</sub>	Tx Output Short Circuit Current Limit	OA/B_n = GND			90	mA
R <sub>otd</sub>	Output Differential Impedance between OUT+ and OUT-	DC tested, ( <i>Note 2</i> )	85	100	125	Ω
R <sub>OTIB</sub>	Output Differential Impedance Imbalance	DC tested, (Note 2)			5	Ω
R <sub>OCM</sub>	Output Common Mode Impedance	DC tested, (Note 2)	20	25	35	Ω
V <sub>TX-CM-DELTA</sub>	Common Mode Voltage Delta between active burst and electrical Idle of an OOB signal	(Note 7)			±40	mV
T <sub>DI</sub>	Max time to transition to valid electrical idle after leaving active burst in OOB signaling	pattern at 3 Gbps,		6.5	9.5	ns

1
0
4
£
Ω
4
9
S

Symbol	Parameter	Conditions	Min	Тур	Max	Units
T <sub>ID</sub>		VIN = 800 mVp-p, repeating 1100b (D24.3) pattern at 3 Gbps, SD_TH = Float, <i>Figure 3</i>		5.5	8	ns
T <sub>PD</sub>	Differential Propagation Delay (Low to High and High to Low Edge)	Propagation delay measured at midpoint crossing between input to output, <i>Figure 2</i> , EQx[1:0] = 11, $DEMx[1:0] = -6 dB$	150	200	250	ps
		EQx[1:0] = OFF, DEMx[1:0] = 0 dB	120	170	220	ps
T <sub>LSK</sub>	Lane to Lane Skew in a Single Part	V <sub>DD</sub> = 2.5 V, T <sub>A</sub> = 25°C			27	ps
T <sub>PPSK</sub>	Part to Part Propagation Delay Skew	V <sub>DD</sub> = 2.5 V, T <sub>A</sub> = 25°C			35	ps
EQUALIZATIO	ON					-
DJ1	Residual Deterministic Jitter at 6.4 Gbps	Tx Launch Amplitude = 0.8 to 1.2 Vp–p, 40" 4–mil FR4 trace, EQx[1:0] = 0F, DEMx[1:0] = 0 dB, VOD = 1.0 Vp-p, K28.5, SD_TH = float, ( <i>Note 2</i> )		0.12	0.25	UI <sub>P-P</sub>
DJ2	Residual Deterministic Jitter at 6.4 Gbps	Tx Launch Amplitude = 0.8 to 1.2 Vp-p, 12 meters (30 AWG), EQx[1:0] = 1F, DEMx[1:0] = 0 dB, VOD = 1.0 Vp-p, K28.5, SD_TH = float, ( <i>Note 2</i> )		0.05	0.15	UI <sub>P-P</sub>
DJ3	Residual Deterministic Jitter at 3.2 Gbps	Tx Launch Amplitude = $0.8$ to 1.2 Vp-p, 40" 4-mil FR4 trace, EQx[1:0] = 0F, DEMx[1:0] = 0 dB, VOD = $1.0$ Vp-p, K28.5, SD_TH = float, ( <i>Note 2</i> )		0.05	0.12	UI <sub>P-P</sub>
DJ4	Residual Deterministic Jitter at 3.2 Gbps	Tx Launch Amplitude = 0.8 to 1.2 Vp-p, 12 meters (30 AWG), EQx[1:0] = 1F, DEMx[1:0] = 0 dB, VOD = 1.0 Vp-p, K28.5, SD_TH = float, ( <i>Note 2</i> )		0.06	0.16	UI <sub>P-P</sub>
RJ	Random Jitter	Tx Launch Amplitude = 0.8 to 1.2 Vp-p, Repeating 1100b (D24.3) pattern		0.5		psrms

Symbol	Parameter	Conditions	Min	Тур	Max	Units
DE-EMPHASI	S					
DJ5	Residual Deterministic Jitter	Tx Launch amplitude = 0.8 to				
	at 6.4 Gbps	1.2 Vp-p, 10" 4-mil FR4 trace,		0.09	0.20	
		EQx[1:0] = OFF, DEMx[1:0] = -6 dB,		0.09	0.20	UI <sub>P-P</sub>
		VOD = 1.0 Vp-p, K28.5, RATE = 1 ( <i>Note 2</i> )				
DJ6	Residual Deterministic Jitter	Tx Launch amplitude = 0.8 to				
	at 3.2 Gbps	1.2 Vp-p, 20" 4-mil FR4 trace,		0.07	0.18	
		EQx[1:0] = OFF, DEMx[1:0] = -6 dB,		0.07	0.18	UI <sub>P-P</sub>
		VOD = 1.0 Vp-p, K28.5, RATE = 0 ( <i>Note 2</i> )				

**Note 1:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are guaranteed for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

Note 2: Typical values represent most likely parametric norms at V<sub>DD</sub> = 2.5V, T<sub>A</sub> = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 3: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 4: Allowed supply noise (mV<sub>P-P</sub> sine wave) under typical conditions.

Note 5: Measured with clock-like {11111 00000} pattern.

Note 6: Measured at package pins of receiver. The 130 mVp-p is a typical threshold level and does not include hysteresis, thus less than 40 mVp-p is IDLE, greater than 175 mVp-p is ACTIVE. SD\_TH pin connected with resistor to GND overrides this default setting.

Note 7: Common-mode voltage (VCM) is expressed mathematically as the average of the two signal voltages with respect to local ground.

VCM = (A + B) / 2, A = OUT+, B = OUT-.

**DS64BR40**<sup>-</sup>

# Electrical Characteristics — Serial Management Bus Interface

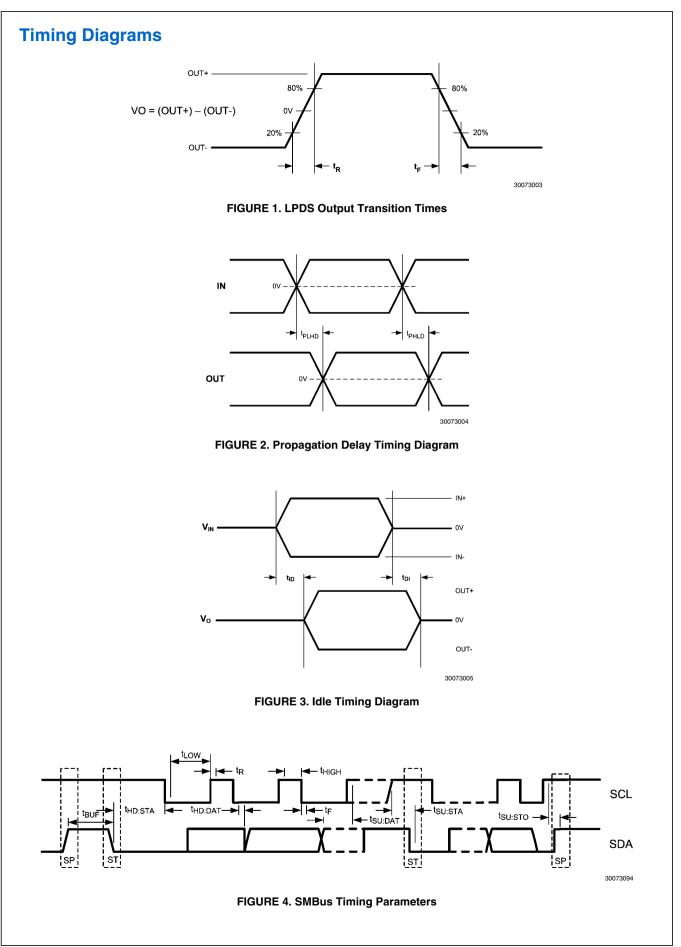
Symbol	Parameter	Conditions	Min	Тур	Max	Units
SERIAL BUS	INTERFACE DC SPECIFICATIONS	5				
V <sub>OL</sub>	Data (SDA) Low Level Output Voltage	I <sub>OL</sub> = 3mA			0.4	V
V <sub>IL</sub>	Data (SDA), Clock (SCL) Input Low Voltage				0.8	v
V <sub>IH</sub>	Data (SDA), Clock (SCL) Input High Voltage		2.1		3.6	v
I <sub>PULLUP</sub>	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V <sub>DD</sub>	Nominal Bus Voltage		2.375		3.6	V
I <sub>LEAK-Bus</sub>	Input Leakage Per Bus Segment	(Note 8)	-200		+200	μA
I <sub>LEAK-Pin</sub>	Input Leakage Per Device Pin			-15		μA
CI	Capacitance for SDA and SCL	(Note 8, Note 9)			10	pF
R <sub>TERM</sub>	External Termination Resistance pull to $V_{DD}$ = 2.5V ± 5% OR 3.3V ±	V <sub>DD3.3</sub> , ( <i>Note 8, Note 9, Note 10</i> )		2000		Ω
	10%	V <sub>DD2.5</sub> , ( <i>Note 8, Note 9, Note 10</i> )		1000		Ω
SERIAL BUS	INTERFACE TIMING SPECIFICAT	ONS. See Figure 4		-	-	-
FSMB	Bus Operating Frequency	(Note 11)	10		100	kHz
TBUF	Bus Free Time Between Stop and Start Condition		4.7			μs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I <sub>PULLUP</sub> , Max	4.0			μs
TSU:STA	Repeated Start Condition Setup Time		4.7			μs
TSU:STO	Stop Condition Setup Time		4.0			μs
THD:DAT	Data Hold Time		300			ns
TSU:DAT	Data Setup Time		250			ns
T <sub>TIMEOUT</sub>	Detect Clock Low Timeout	(Note 11)	25		35	ms
T <sub>LOW</sub>	Clock Low Period		4.7			μs
T <sub>HIGH</sub>	Clock High Period	(Note 11)	4.0		50	μs
T <sub>LOW</sub> :SEXT	Cumulative Clock Low Extend Time (Slave Device)	(Note 11)			2	ms
t <sub>F</sub>	Clock/Data Fall Time	(Note 11)			300	ns
t <sub>R</sub>	Clock/Data Rise Time	(Note 11)			1000	ns
t <sub>POR</sub>	Time in which a device must be operational after power-on reset	(Note 11)			500	ms

Note 8: Recommended value. Parameter not tested in production.

Note 9: Recommended maximum capacitance load per bus segment is 400pF.

Note 10: Maximum termination voltage should be identical to the device supply voltage.

Note 11: Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.



## **Functional Description**

The DS64BR401 is a quad repeater optimized for backplane trace or cable interconnect up to 6.4 Gbps. The DS64BR401 operates in two modes: Pin Control Mode (ENSMB = 0) and SMBus Mode (ENSMB = 1).

### Pin Control Mode:

When in pin mode (ENSMB = 0), the repeater is configurable with external pins. Equalization and de-emphasis can be selected via pin for each side independently. When de-emphasis is asserted VOD is automatically increased per the De-Emphasis table below for improved performance over lossy media. Rate optimization is also pin controllable, with pin selections for 3 Gbps, 6 Gbps, and auto detect. The receiver electrical idle detect threshold is also programmable via an optional external resistor on the SD\_TH pin.

#### SMBUS Mode

When in SMBus mode the equalization, de-emphasis are all programmable on a individual lane basis, instead of grouped

by sides as in the pin mode case. Upon assertion of ENSMB the RATE, EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. The other external control pins remain active unless their respective registers are written to and the appropriate override bit is set, in which case they are ignored until ENSMB is driven low. On powerup and when ENSMB is driven low all registers are reset to their default state. If PWDN = 1 is asserted while ENSMB = 1, the registers retain their current state.

Equalization settings accessible via the pin controls were chosen to meet the needs of most applications. If additional fine tuning or adjustment is needed, additional equalization settings can be accessed via the SMBus registers. Each input has a total of 24 possible equalization settings. The tables show a typical gain for each gain stage (GST[4:3]) and boost level (BST[2:0]) combination. When using SMBus mode, the Equalization and De-Emphasis levels are set using registers. See *Table 8* (register map) for more information.

		EQ S	etting	EQ Ga	in (dB)	
EQ1	EQ0	GST [4:3]	BST [2:0]	1.5 GHz	3.0 GHz	Suggested Use
F	F	00	000	0	0	Bypass - Default Setting
		01	000	2.0	3.8	
		01	001	2.6	4.9	
1	1	01	010	3.3	5.8	8 inch FR4 (4-mil trace) or < 0.7m (30 AWG)
		01	011	3.9	6.8	
		01	100	4.9	8.2	
		01	101	5.5	8.9	
		01	110	6.0	9.4	
		01	111	6.5	10.0	
	F=	=Float (d	don't driv	e pin, each floa	t pin has an inte	rnal 50K Ohm resistor to VDD and GND), 1=High, 0=Low

TABLE 1. Equalization Settings with GST=1 for Pins or SMBus R	legisters
---	-----------

TABLE 2.	Equalization	Settings with	GST=2 for Pins	or SMBus Registers
			•••••••••••••••••••••••••••••••••••••••	•. •

		EQ S	etting	EQ Gain (dB)		
EQ1	EQ0	GST [4:3]	BST [2:0]	1.5 GHz	3.0 GHz	Suggested Use
0	0	10	000	4.8	9.2	12" FR4 (4-mil trace) or 1m (30 AWG)
F	0	10	001	6.3	11.7	20" FR4 (4-mil trace) or 5m (30 AWG)
		10	010	7.6	13.6	
		10	011	9.1	15.6	
F	1	10	100	11.1	18.4	35" FR4 (4-mil trace) or 9m (30 AWG)
0	1	10	101	12.4	20.0	40" FR4 (4-mil trace) or 10m (30 AWG)
		10	110	13.4	20.9	
		10	111	14.5	22.0	
	 F=	=Float (c	don't driv	e pin. each float	pin has an inte	rnal 50K Ohm resistor to VDD and GND), 1=High, 0=Low

## TABLE 3. Equalization Settings with GST=3 for Pins or SMBus Registers

		EQ S	etting	EQ Ga	iin (dB)	
EQ1	EQ0	GST [4:3]	BST [2:0]	1.5 GHz	3.0 GHz	Suggested Use
1	0	11	000	7.7	14.6	25" FR4 (4-mil trace) or 6m (30 AWG)
		11	001	10.1	18.4	
0	F	11	010	12.2	21.2	10m (30 AWG)
		11	011	14.4	24.4	
1	F	11	100	17.5	28.4	12m (30 AWG)
		11	101	19.4	30.6	
		11	110	20.9	32.1	
		11	111	22.6	33.8	
	F=	=Float (c	don't driv	e pin, each floa	t pin has an inte	ernal 50K Ohm resistor to VDD and GND), 1=High, 0=Low

## TABLE 4. De-Emphasis Input Select Pins for A and B ports (3–Level Input)

RATE	DEM1	DEM0	De- Emphasi s Level (typ)	DE Pulse Width (typ)	VOD (typical)	Suggested Use
0/F	0	0	0 dB	0 ps	VOD: 600 to 1200 mVp-p	10 inch FR4 trace or 1 meter (28 AWG)
0/F	0	1	-3.5 dB	330 ps	VOD = 1000 mVp-p	20 inch FR4 trace or 2 meters (28 AWG)
			-2 dB	330 ps	VOD = 1200 mVp-p	15 inch FR4 trace or 2 meters (28 AWG)
0/F	1	0	-6 dB	330 ps	VOD = 1000 mVp-p	25 inch FR4 trace or 3 meters (28 AWG)
			-3 dB	330 ps	VOD = 1200 mVp-p	20 inch FR4 trace or 2 meters (28 AWG)
0/F	1	1	-9 dB	300 ps enhanced	VOD = 1000 mVp-p	5 meters (28 AWG)
			-11 dB	300 ps enhanced	VOD = 1200 mVp-p	7 meters (28 AWG)
0/F	0	F	-6 dB	300 ps enhanced	VOD = 1000 mVp-p	5 meters (26 AWG)
			-8 dB	300 ps enhanced	VOD = 1200 mVp-p	7 meters (26 AWG)
0/F	1	F	-12 dB	300 ps enhanced	VOD = 1000 mVp-p	8 meters (24 AWG)
			-13 dB	300 ps enhanced	VOD = 1200 mVp-p	9 meters (24 AWG)
0/F	F	0	-9 dB	250 ps enhanced	VOD = 1000 + 200 mVp-p	8 meters (26 AWG)
			-10 dB	250 ps enhanced	VOD = 1200 + 200 mVp-p	9 meters (26 AWG)
0/F	F	1	-12 dB	250 ps enhanced	VOD: (1000 to 1200) + 200 mVp-p	10 meters (24 AWG)
0/F	F	F			Reserved, don't	use
1/F	0	0	0 dB	0 ps	VOD: 600 to 1200 mVp-p	5 inch FR4 trace or 0.5 meter (28 AWG)
1/F	0	1	-3.5 dB	200 ps	VOD = 1000 mVp-p	10 inch FR4 trace or 1 meter (28 AWG)
			-2 dB	200 ps	VOD = 1200 mVp-p	10 inch FR4 trace or 1 meters (28 AWG)
1/F	1	0	-6 dB	200 ps	VOD = 1000 mVp-p	20 inch FR4 trace or 2 meters (28 AWG)
			-3 dB	200 ps	VOD = 1200 mVp-p	15 inch FR4 trace or 1 meters (28 AWG)
1/F	1	1	-9 dB	180 ps enhanced	VOD = 1000 mVp-p	3 meters (28 AWG)
			-11 dB	180 ps enhanced	VOD = 1200 mVp-p	4 meters (28 AWG)

RATE	DEM1	DEM0	De- Emphasi s Level (typ)	DE Pulse Width (typ)	VOD (typical)	Suggested Use		
1/F	0	F	-6 dB	180 ps enhanced	VOD = 1000 mVp-p	3 meters (26 AWG)		
			-8 dB	180 ps enhanced	VOD = 1200 mVp-p	4 meters (26 AWG)		
1/F	1	F	-12 dB	180 ps enhanced	VOD = 1000 mVp-p	5 meters (24 AWG)		
			-13 dB	180 ps enhanced	VOD = 1200 mVp-p	6 meters (24 AWG)		
1/F	F	0	-9 dB	160 ps enhanced	VOD = 1000 + 200 mVp-p	5 meters (26 AWG)		
			-10 dB	160 ps enhanced	VOD = 1200 + 200 mVp-p	6 meters (26 AWG)		
1/F	F	1	-12 dB	160 ps enhanced	VOD: (1000 to 1200) + 200 mVp-p	7 meters (24 AWG)		
1/F	F	F	Reserved, don't use					

Note: F = Float (don't drive pin), 1 = High and 0 = Low. Enhanced DE pulse width provides de-empahsis on second bit. When RATE = F (auto rate detection active), the DE level and pulse width settings follow detected rate after exiting IDLE. RATE = 0 is 3 Gbps and RATE = 1 is 6 Gbps. De-emphasis should only be used with VOD = 1000 mVp-p or 1200 mVp-p. VOD less then 1000 mVp-p is not recommended with de-emphasis. Please refer to VOD1 and VOD0 pin description to set the output differential voltage level.

TXIDLEA/B	Function
0	This state is for lossy media, dedicated Idle threshold detect circuit disabled, output follows input based
	on EQ settings. Idle state not guaranteed.
Float	Float enables automatic idle detection. Idle on the input is passed to the output. Internal 50K $\Omega$ resistors
	hold TXIDLEA/B pin at a mid level - don't connect this pin if the automatic idle detect function is desired.
	This is the default state. Output in Idle if differential input signal less than value set by SD_TH pin.
1	Manual override, output in electrical Idle. Differential inputs are ignored.

#### TABLE 6. Receiver Electrical Idle Detect Threshold Adjust

SD_TH resistor value (Ω)	Receiver Electrical Idle Detect Threshold (DIFF p-p)					
Float (no resistor required)	130 mV (default condition)					
0	225 mV					
80k	80k 20 mV					
SD TH resistor value can be set from 0 through 8	0k ohms to achieve desired idle detect threshold, see Figure 5					

# **Typical Performance Curves**

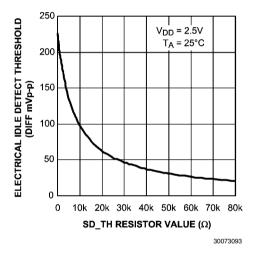
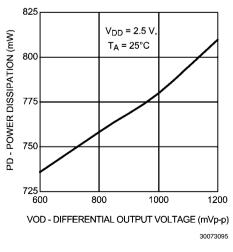


FIGURE 5. Typical Idle Threshold vs. SD\_TH resistor value





# System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SM-Bus 2.0 physical layer specification. ENSMB must be pulled high to enable SMBus mode and allow access to the configuration registers.

The DS64BR401 has the AD[3:0] inputs in SMBus mode. These pins set the SMBus slave address inputs. The AD[3:0] pins have internal pull-down. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is A0'h. Based on the SMBus 2.0 specification, the DS64BR401 has a 7-bit slave address of 1010000'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 1010 0000'b or A0'h. The bold bits indicate the AD[3:0] pin map to the slave address bits [4:1]. The device address byte can be set with the use of the AD[3:0] inputs. Below are some examples.

AD[3:0] = 0001'b, the device address byte is A2'h

AD[3:0] = 0010'b, the device address byte is A4'h

AD[3:0] = 0100'b, the device address byte is A8'h

AD[3:0] = 1000'b, the device address byte is B0'h

The SDA, SCL pins are 3.3V tolerant, but are not 5V tolerant. External pull-up resistor is required on the SDA. The resistor value can be from 1 k $\Omega$  to 5 k $\Omega$  depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

### TRANSFER OF DATA VIA THE SMBUS

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

**START:** A High-to-Low transition on SDA while SCL is High indicates a message START condition.

**STOP:** A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

**IDLE:** If SCL and SDA are both High for a time exceeding  $t_{BUF}$  from the last detected STOP condition or if they are High for a total exceeding the maximum specification for  $t_{HIGH}$  then the bus will transfer to the IDLE state.

#### **SMBUS TRANSACTIONS**

The device supports WRITE and READ transactions. See Register Description table for register address, type (Read/ Write, Read Only), default value and function information.

When SMBus is enabled, the DS64BR401 **must use one of the following De-emphasis settings** (*Table 7*). The driver de-emphasis value is set on a per channel basis using 8 different registers. Each register (0x11, 0x18, 0x1F, 0x26, 0x2E, 0x35, 0x3C, 0x43) requires one of the following De-emphasis settings when in SMBus mode.

#### TABLE 7. De-Emphasis Register Settings (must write one of the following when in SMBus mode)

De-Emphasis Value	Register Setting	3 Gbps Operation	6 Gbps Operation
0.0 dB	0x01	10" trace or 1 meter 28 awg cable	5" trace or 0.5 meter 28 awg cable
-3.5 dB	0x38	20" trace or 2 meters 28 awg cable	10" trace or 1meters 28 awg cable
-6 dB	0x88	25" trace or 3 meters cable	20" trace or 2 meters cable
-9 dB	0x90	5 meters 28 awg cable	3 meters 28 awg cable
-12 dB	0xA0	8 meters 28 awg cable	5 meters 28 awg cable

### WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

- 1. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
- 2. The Device (Slave) drives the ACK bit ("0").
- 3. The Host drives the 8-bit Register Address.
- 4. The Device drives an ACK bit ("0").
- 5. The Host drive the 8-bit data byte.
- 6. The Device drives an ACK bit ("0").
- 7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

#### **READING A REGISTER**

To read a register, the following protocol is used (see SMBus 2.0 specification).

- 1. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
- 2. The Device (Slave) drives the ACK bit ("0").
- 3. The Host drives the 8-bit Register Address.
- 4. The Device drives an ACK bit ("0").
- 5. The Host drives a START condition.
- 6. The Host drives the 7-bit SMBus Address, and a "1" indicating a READ.
- 7. The Device drives an ACK bit "0".

- 8. The Device drives the 8-bit data value (register contents).
- The Host drives a NACK bit "1"indicating end of the READ transfer.
- 10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

#### **RECOMMENDED SMBUS REGISTER SETTINGS**

When SMBus mode is enabled (ENSMB = 1), the default register are not configured to an appropriate settings. Below is the recommended settings to configure the EQ, VOD and DE to a medium level that supports interconnect length of 20 inches FR4 trace or 3 to 5 meters of cable length. Please refer to , *Table 1, Table 2, Table 3, Table 4, Table 7, Table 8* for additional information and recommended settings.

- 1. Reset the SMBus registers to default values: Write 01'h to address 0x00.
- Set de-emphasis to -6 dB enhance for all channels (CH0–CH7):
   Write 88'h to address 0x11, 0x18, 0x1F, 0x26, 0x2E, 0x35, 0x3C, 0x43.
- Set equalization to external pin level EQ[1:0] = 00 (~9 dB at 3 GHz) for all channels (CH0–CH7): Write 30'h to address 0x0F, 0x16, 0x1D, 0x24, 0x2C, 0x33, 0x3A, 0x41.
- 4. Set VOD = 1.0V for all channels (CH0–CH7):

Write 0F'h to address 0x10, 0x17, 0x1E, 0x25, 0x2D, 0x34, 0x3B, 0x42.

# Idle and Rate Detection to External Pins

The functions of IDLE and RATE detection to external pins for monitoring can be supported in SMBus mode. The external GPIO pins of 19, 20, 46 and 47 will be changed and they will serve as outputs for IDLE and RATE detect signals.

The following external pins should be set to auto detection:

RATE = F (FLOAT) – auto RATE detect enabled

TXIDLEA/B = F (FLOAT) - auto IDLE detect enabled

There are 4 GPIO pins that can be configured as outputs with reg\_4E[0].

To disable the external SMBus address pins, so pin 46 and 47 can be used as outputs:

#### Write 01'h to address 0x4E.

Care must be taken to ensure that only the desired status block is enabled and attached to the external pin as the status blocks can be OR'ed together internally. Register bits reg\_47 [5:4] and bits reg\_4C[7:6] are used to enable each of the status block outputs to the external pins. The channel status blocks can be internally OR'ed together to monitor more than one channel at a time. This allows more information to be presented on the status outputs and later if desired, a diagnosis of the channel identity can be made with additional SMBus writes to register bits reg\_47[5:4] and bits reg\_4C[7:6].

Below are examples to configure the device and bring the internal IDLE and RATE status to pins 19, 20, 46, 47.

To monitor the IDLE detect with two channels ORed (CH0 with CH2, CH1 with CH3, CH4 with CH6, CH5 with CH7):

#### Write 32'h to address 0x47.

The following IDLE status should be observable on the external pins:

pin 19 - CH0 with CH2,

pin 20 - CH1 with CH3,

pin 46 - CH4 with CH6,

pin 47 - CH5 with CH7.

Pin = HIGH (VDD) means IDLE is detected (no signal present).

Pin = LOW (GND) means ACTIVE (data signal present). To monitor the RATE detect with two channels ORed (CH0

To monitor the RATE detect with two channels ORed (CH0 with CH2, CH1 with CH3, CH4 with CH6, CH5 with CH7):

#### Write C0'h to address 0x4C.

The following RATE status should be observable on the external pins:

pin 19 - CH0 with CH2,

pin 20 - CH1 with CH3,

pin 46 - CH4 with CH6,

pin 47 – CH5 with CH7.

Pin = HIGH (VDD) means high data rate is detected (6 Gbps). Pin = LOW (GND) means low rate is detected (3 Gbps).

Address	Register Name	Bit (s)	Field	Туре	Default	Description
0x00	Reset	7:1	Reserved	R/W	0x00	Set bits to 0.
		0	Reset			SMBus Reset
						1: Reset registers to default value
0x01	PWDN Channels	7:0	PWDN CHx	R/W	0x00	Power Down per Channel
						[7]: CHA_3
						[6]: CHA_2
						[5]: CHA_1
						[4]: CHA_0
						[3]: CHB_3
						[2]: CHB_2
						[1]: CHB_1
						[0]: CHB_0
						00'h = all channels enabled
						FF'h = all channels disabled
0x02	PWDN Control	7:1	Reserved	R/W	0x00	Set bits to 0.
		0	Override PWDN			0: Allow PWDN pin control
						1: Block PWDN pin control
0x08	Pin Control Override	7:5	Reserved	R/W	0x00	Set bits to 0.
		4	Override IDLE			0: Allow IDLE pin control
						1: Block IDLE pin control
		3	Reserved			Set bit to 0.
		2	Override RATE			0: Allow RATE pin control
						1: Block RATE pin control
		1:0	Reserved		1	Set bits to 0.

Address	Register Name	Bit (s)	Field	Туре	Default	Description
0x0E	CH0 - CHB0	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE RATE Select	5	IDLE auto			0: Allow IDLE_sel control in Bit 4
						1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled)
						1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0
						1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps
a a=						1: 5.0 to 6.4 Gbps
0x0F	CH0 - CHB0 EQ Control	7:6	Reserved	R	0x0	Set bits to 0.
	EQ Control	5:0	CH0 IB0 EQ	R/W	0x20	IB0 EQ Control - total of 24 levels
						(3 gain stages with 8 settings) [5]: Enable EQ
						[4:3]: Gain Stage Control
						[2:0]: Boost Level Control
						Pin [EQ0 EQ1] = Register [EN] [GST] [BST] =
						Hex Value
						FF = 100000 = 20'h = Bypass (Default)
						11 = 101010 = 2A'h
						00 = 110000 = 30'h
						0F = 110001 = 31'h
						01 = 111000 = 38'h 1F = 110100 = 34'h
						10 = 110100 = 35'h
						F0 = 111010 = 3A'h
						F1 = 111100 = 3C'h
0x10	CH0 - CHB0	7:6	Reserved	R	0x00	Set bit to 0.
	VOD Control	5:0	CH0 OB0 VOD	R/W	0x03	OB0 VOD Control
						03'h = 600 mV (Default)
						07'h = 800 mV
						0F'h = 1000 mV
						1F'h = 1200  mV
011		7.0			000	3F'h = 1400 mV
0x11	CH0 - CHB0 DE Control	7:0	CH0 OB0 DEM	R/W	0x03	OB0 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced
						[7]. Dewritten (compatibility = 07 Enhanced $= 1$ )
						[6:0]: DEM Level Control
						Pin [DEM1 DEM0] = Register [TYPE] [Level
						Control] = Hex Value
						00 = 00000001 = 01'h = 0.0 dB
						01 = 00111000 = 38'h = -3.5 dB
						0F = 10001000 = 88'h = -6.0 dB
						01 = 10010000 = 90'h = $-9.0$ dB
						1F = 10100000 = A0'h = -12.0 dB F0 = 10010000 = 90'h = -9.0 dB
						F0 = 10010000 = 90  h = -9.0  dB F1 = 10100000 = A0  h = -12.0  dB
						FF = 11000000 = A011 = -12.0 dB FF = 11000000 = C0'h = Reserved
0x12	CH0 - CHB0	7:4	Reserved		0x00	Set bits to 0.
UN 12	IDLE Threshold	3:0	IDLE threshold			De-assert = [3:2], assert = [1:0]
		13.0				00 = 110  mV, 70  mV (Default)
						01 = 150  mV, 110  mV
						10 = 170  mV, 130  mV
		1				11 = 190 mV, 150 mV

- T-
0
4
ſ
Ω
4
ശ
S

Address	Register Name	Bit (s)	Field	Туре	Default	Description
0x15	CH1 - CHB1	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE RATE Select	5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x16	СН1 - СНВ1	7:6	Reserved	R/W	0x20	Set bits to 0.
	EQ Control	5:0	CH1 IB1 EQ			IB1 EQ Control - total of 24 levels         (3 gain stages with 8 settings)         [5]: Enable EQ         [4:3]: Gain Stage Control         [2:0]: Boost Level Control         Pin [EQ0 EQ1] = Register [EN] [GST] [BST]         Hex Value         FF = 100000 = 20'h = Bypass (Default)         11 = 101010 = 2A'h         00 = 110000 = 30'h         OF = 110001 = 31'h         01 = 111000 = 38'h         1F = 110100 = 34'h         10 = 110101 = 35'h         F0 = 111010 = 3A'h         F1 = 111100 = 3C'h
0x17	СН1 - СНВ1	7:6	Reserved	R	0x00	Set bit to 0.
	VOD Control	5:0	CH1 OB1 VOD	R/W	0x03	OB1 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV
0x18	CH1 - CHB1 DE Control	7:0	CH1 OB1 DEM	R/W	0x03	OB1 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhance = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = $-3.5$ dB 0F = 10011000 = 88'h = $-6.0$ dB 01 = 10010000 = 80'h = $-9.0$ dB 1F = 10100000 = A0'h = $-12.0$ dB F0 = 10010000 = 90'h = $-9.0$ dB F1 = 10100000 = A0'h = $-12.0$ dB FF = 11000000 = C0'h = Reserved
0x19	CH1 - CHB1	7:4	Reserved	R/W	0x00	Set bits to 0.
-	IDLE Threshold	3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV
0x19				R	/W	/W 0x00

Address	Register Name	Bit (s)	Field	Туре	Default	Description
0x1C	CH2 - CHB2	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE RATE Select	5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0
		0	RATE select	_		1: Automatic RATE detect 0: 2.5 to 3.2 Gbps
						1: 5.0 to 6.4 Gbps
0x1D	CH2 - CHB2 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH2 IB2 EQ			IB2 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h 0F = 110001 = 31'h 01 = 111000 = 38'h 1F = 110100 = 34'h 10 = 1110101 = 35'h F0 = 111010 = 3A'h F1 = 111100 = 3C'h
0x1E	CH2 - CHB2	7:6	Reserved	R	0x00	Set bit to 0.
	VOD Control	5:0	CH2 OB2 VOD	R/W	0x03	OB2 VOD Control 03'h = 600  mV  (Default) 07'h = 800  mV 0F'h = 1000  mV 1F'h = 1200  mV 3F'h = 1400  mV
0x1F	CH2 - CHB2 DE Control	7:0	CH2 OB2 DEM	R/W	0x03	OB2 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = $-3.5$ dB 0F = 10001000 = 88'h = $-6.0$ dB 01 = 10010000 = 90'h = $-9.0$ dB 1F = 10100000 = 40'h = $-12.0$ dB F0 = 10010000 = 90'h = $-9.0$ dB F1 = 10100000 = A0'h = $-12.0$ dB F1 = 11000000 = A0'h = $-12.0$ dB FF = 11000000 = C0'h = Reserved
0x20	CH2 - CHB2	7:4	Reserved	R/W	0x00	Set bits to 0.
	IDLE Threshold	3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV
						10 = 170 mV, 130 mV

- T-
0
4
ſ
Ω
4
ဖ
S

Address	Register Name	Bit (s)	Field	Туре	Default	Description
0x23	СНЗ - СНВЗ	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE RATE Select	5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved	-		Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0
				_		1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x24	СНЗ - СНВЗ	7:6	Reserved	R/W	0x20	Set bits to 0.
	EQ Control	5:0	CH3 IB3 EQ			IB3 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h 0F = 110001 = 31'h 01 = 111000 = 38'h 1F = 110100 = 34'h 10 = 110101 = 35'h F0 = 111010 = 3A'h F1 = 111100 = 3C'h
0x25	СНЗ - СНВЗ	7:6	Reserved	R	0x00	Set bit to 0.
	VOD Control	5:0	CH3 OB3 VOD	R/W	0x03	OB3 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV
0x26	CH3 - CHB3 DE Control	7:0	CH3 OB3 DEM	R/W	0x03	OB3 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = $-3.5$ dB 0F = 1001000 = 88'h = $-6.0$ dB 01 = 10010000 = 90'h = $-9.0$ dB 1F = 10100000 = A0'h = $-12.0$ dB F0 = 10010000 = 90'h = $-9.0$ dB F1 = 10100000 = A0'h = $-12.0$ dB FF = 11000000 = C0'h = Reserved
0x27	СНЗ - СНВЗ	7:4	Reserved	R/W	0x00	Set bits to 0.
	IDLE Threshold	3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV

Address	Register Name	Bit (s)	Field	Туре	Default	Description
0x2B	CH4 - CHA0	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE RATE Select	5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto	_		0: Allow RATE_sel control in Bit 0
						1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps
						1: 5.0 to 6.4 Gbps
0x2C	CH4 - CHA0 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
0x2D	CH4 - CHA0 VOD Control	5:0 7:6 5:0	CH4 IA0 EQ Reserved CH4 OA0 VOD	R B/W	0x00 0x03	IA0 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h 0F = 110001 = 31'h 01 = 111000 = 38'h 1F = 110100 = 38'h 1F = 110101 = 35'h F0 = 111010 = 3A'h F1 = 111100 = 3C'h Set bit to 0.
			CH4 OA0 VOD		0x03	OA0 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV
0x2E	CH4 - CHA0 DE Control	7:0	CH4 OA0 DEM	R/W	0x03	OA0 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = $-3.5$ dB 0F = 1001000 = 88'h = $-6.0$ dB 01 = 10010000 = 80'h = $-9.0$ dB 1F = 10100000 = A0'h = $-12.0$ dB F0 = 10010000 = 90'h = $-9.0$ dB F1 = 10100000 = A0'h = $-12.0$ dB FF = 11000000 = C0'h = Reserved
0x2F	CH4 - CHA0	7:4	Reserved	R/W	0x00	Set bits to 0.
	IDLE Threshold	3:0	IDLE threshold			De-assert = [3:2], assert = [1:0]
						00 = 110 mV, 70 mV (Default)
						01 = 150 mV, 110 mV
						10 = 170 mV, 130 mV
	1		1		1	11 = 190 mV, 150 mV

- T-
0
4
ſ
Ω
4
ശ
S

Address	Register Name	Bit (s)	Field	Туре	Default	Description
0x32	CH5 - CHA1	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE RATE Select	5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x33	CH5 - CHA1	7:6	Reserved	R/W	0x20	Set bits to 0.
	EQ Control	5:0	CH5 IA1 EQ			IA1 EQ Control - total of 24 levels         (3 gain stages with 8 settings)         [5]: Enable EQ         [4:3]: Gain Stage Control         [2:0]: Boost Level Control         Pin [EQ0 EQ1] = Register [EN] [GST] [BST] =         Hex Value         FF = 100000 = 20'h = Bypass (Default)         11 = 101010 = 2A'h         00 = 110000 = 30'h         OF = 110001 = 31'h         01 = 111000 = 38'h         1F = 110100 = 34'h         10 = 110101 = 35'h         F0 = 111010 = 3A'h         F1 = 111100 = 3C'h
0x34	CH5 - CHA1	7:6	Reserved	R	0x00	Set bit to 0.
	VOD Control	5:0	CH5 OA1 VOD	R/W	0x03	OA1 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV
0x35	CH5 - CHA1 DE Control	7:0	CH5 OA1 DEM	R/W	0x03	OA1 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhance = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = $-3.5$ dB 0F = 1001000 = 88'h = $-6.0$ dB 01 = 10010000 = 80'h = $-9.0$ dB 1F = 10100000 = A0'h = $-12.0$ dB F0 = 10010000 = 90'h = $-9.0$ dB F1 = 10100000 = A0'h = $-12.0$ dB FF = 11000000 = C0'h = Reserved
0x36	CH5 - CHA1	7:4	Reserved	R/W	0x00	Set bits to 0.
	IDLE Threshold	3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV

Address	Register Name	Bit (s)	Field	Туре	Default	Description
0x39	CH6 - CHA2	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE RATE Select	5	IDLE auto			0: Allow IDLE_sel control in Bit 4
						1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled)
						1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0
						1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps
						1: 5.0 to 6.4 Gbps
0x3A	CH6 - CHA2	7:6	Reserved	R/W	0x20	Set bits to 0.
	EQ Control	5:0	CH6 IA2 EQ			IA2 EQ Control - total of 24 levels
						(3 gain stages with 8 settings)
						[5]: Enable EQ
						[4:3]: Gain Stage Control
						[2:0]: Boost Level Control
						Pin [EQ0 EQ1] = Register [EN] [GST] [BST] =
						Hex Value
						FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h
						100 = 110000 = 30'h
						0F = 110001 = 31'h
						01 = 111000 = 38'h
						1F = 110100 = 34'h
						10 = 110101 = 35'h
						F0 = 111010 = 3A'h
						F1 = 111100 = 3C'h
0x3B	CH6 - CHA2	7:6	Reserved	R	0x00	Set bit to 0.
	VOD Control	5:0	CH6 OA2 VOD	R/W	0x03	OA2 VOD Control
						03'h = 600 mV (Default)
						07'h = 800 mV
						0F'h = 1000 mV
						1F'h = 1200 mV
						3F'h = 1400 mV
0x3C	CH6 - CHA2	7:0	CH6 OA2 DEM	R/W	0x03	OA2 DEM Control
	DE Control					[7]: DEM TYPE (Compatibility = 0 / Enhanced
						[6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level
						Control] = Hex Value
						00 = 00000001 = 01'h = 0.0 dB
						01 = 00111000 = 38'h = -3.5 dB
						0F = 10001000 = 88'h = -6.0 dB
						01 = 10010000 = 90'h = -9.0 dB
						1F = 10100000 = A0'h = -12.0 dB
						F0 = 10010000 = 90'h = -9.0 dB
						F1 = 10100000 = A0'h = -12.0 dB
						FF = 11000000 = C0'h = Reserved
0x3D	CH6 - CHA2	7:4	Reserved	R/W	0x00	Set bits to 0.
	IDLE Threshold	3:0	IDLE threshold			De-assert = [3:2], assert = [1:0]
						00 = 110 mV, 70 mV (Default)
						01 = 150 mV, 110 mV
						10 = 170 mV, 130 mV
	1				1	11 = 190 mV, 150 mV

- T-
0
4
ſ
Ω
4
ဖ
S

Address	Register Name	Bit (s)	Field	Туре	Default	Description
0x40	CH7 - CHA3	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE RATE Select	5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved	-		Set bits to 0.
		1	RATE auto	-		0: Allow RATE_sel control in Bit 0
						1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x41	CH7 - CHA3	7:6	Reserved	R/W	0x20	Set bits to 0.
0x42	EQ Control CH7 - CHA3 VOD Control	5:0 7:6 5:0	CH7 IA3 EQ Reserved CH7 OA3 VOD	R	0x00 0x03	IA3 EQ Control - total of 24 levels         (3 gain stages with 8 settings)         [5]: Enable EQ         [4:3]: Gain Stage Control         [2:0]: Boost Level Control         Pin [EQ0 EQ1] = Register [EN] [GST] [BST]         Hex Value         FF = 100000 = 20'h = Bypass (Default)         11 = 101010 = 2A'h         00 = 110000 = 30'h         OF = 110001 = 31'h         01 = 111000 = 38'h         1F = 110100 = 34'h         10 = 110101 = 35'h         F0 = 111010 = 3A'h         F1 = 111100 = 3C'h         Set bit to 0.         OA3 VOD Control
						03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV
0x43	CH7 - CHA3 DE Control	7:0	CH7 OA3 DEM	R/W	0x03	OA3 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhance = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = $-3.5$ dB 0F = 10001000 = 88'h = $-6.0$ dB 01 = 10010000 = 90'h = $-9.0$ dB 1F = 10100000 = A0'h = $-12.0$ dB F0 = $10010000 = A0$ 'h = $-12.0$ dB F1 = $10100000 = A0$ 'h = $-12.0$ dB F1 = $11000000 = C0$ 'h = Reserved
0x44	CH7 - CHA3 IDLE Threshold	7:4 3:0	Reserved IDLE threshold	R/W	0x00	Set bits to 0. De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV

Address	Register Name	Bit (s)	Field	Туре	Default	Description
0x47	EN	7:6	Reserved	R/W	0x02	Set bits to 0.
	Digital Test Point IDLE Detect	5	CH2, CH3 CH6, CH7			0: Disabled IDLE Test Point for CH2, 3, 6, 7. 1: Enable IDLE Test Point for CH2, 3, 6, 7.
		4	CH0, CH1 CH4, CH5			0: Disabled IDLE Test Point for CH0, 1, 4, 5. 1: Enable IDLE Test Point for CH0, 1, 4, 5.
		3:2	Reserved			Set bits to 0.
	Global VOD Adjust	1:0	VOD Adjust			00 = -25% 01 = -12.5% 10 = 0% (Default) 11 = +12.5%
0x4C	EN Digital Test Point	7	CH2, CH3 CH6, CH7	R/W	0x00	0: Disabled RATE Test Point for CH2, 3, 6, 7. 1: Enable RATE Test Point for CH2, 3, 6, 7.
	RATE Detect	6	CH0, CH1 CH4, CH5			0: Disabled RATE Test Point for CH0, 1, 4, 5. 1: Enable RATE Test Point for CH0, 1, 4, 5.
		5:0	Reserved			Set bits to 0.
0x4E	Digital Test	7:1	Reserved	R/W	0x00	Set bits to 0.
		0	Block AD[3:0] pins			1: Configure GPIO pin 46, 47, 53, 54 to be

outputs.

# **Applications Information**

#### **GENERAL RECOMMENDATIONS**

The DS64BR401 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

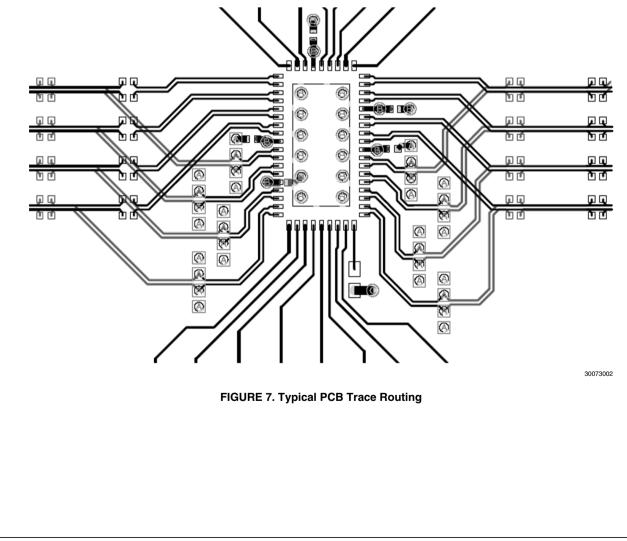
# PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

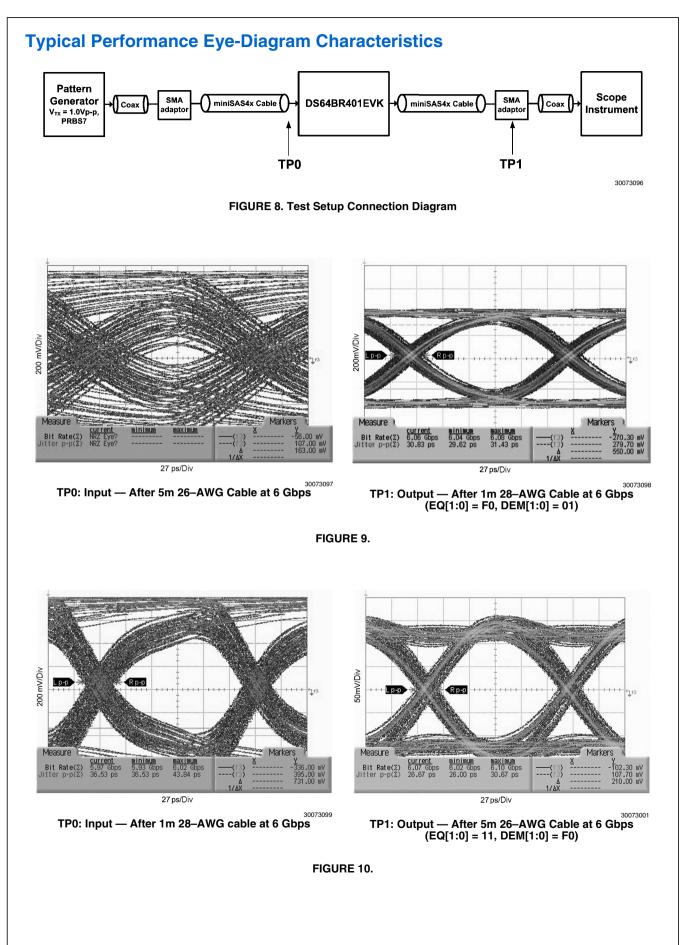
The CML inputs and LPDS outputs must have a controlled differential impedance of  $100\Omega$ . It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187 for additional information on LLP packages.

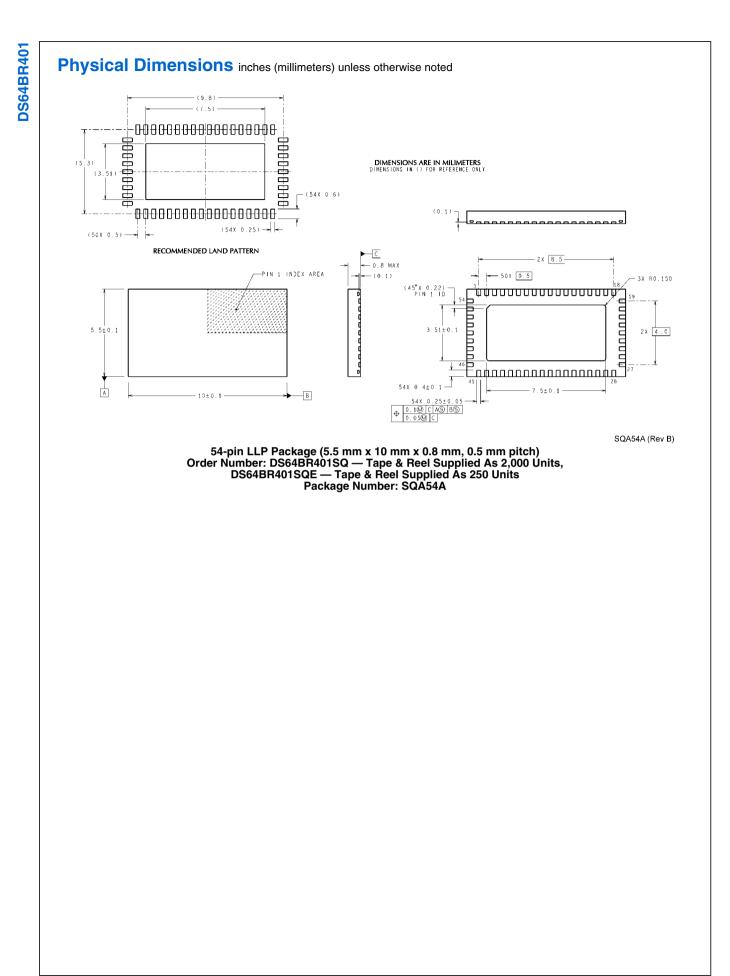
The graphic shown below depicts a typical microstrip trace routing design of the top and bottom layers. This should be used as a reference to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each via hole. To further improve the signal quality, a ground via placed close to the signal via for a low inductance return current path is recommended. When the via structure is associated with stripline trace and a thick board, further optimization such as back drilling is often used to reduce the high frequency effects of via stubs on the signal path. To minimize cross-talk coupling, it is recommended to have >3X gap spacing between the differential pairs. For example, if the trace width is 5 mils with 5 mils spacing – 100 $\Omega$  differential impedance (closely coupled). The gap spacing between the differential pairs should be >15 mils.

#### POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS64BR401 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.01 µF bypass capacitor should be connected to each V<sub>DD</sub> pin such that the capacitor is placed as close as possible to the DS64BR401. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of 2.2  $\mu F$  to 10  $\mu F$  should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.







# Notes

# Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at: www.national.com

Pr	oducts	Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

#### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

#### Copyright© 2010 National Semiconductor Corporation

For the most current product information visit us at www.national.com



National Semiconductor Americas Technical Support Center Email: support@nsc.com Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center Email: europe.support@nsc.com National Semiconductor Asia Pacific Technical Support Center Email: ap.support@nsc.com National Semiconductor Japan Technical Support Center Email: jpn.feedback@nsc.com

#### **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	a O a Al a a m		

**TI E2E Community Home Page** 

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated