SLLS544H-SEPTEMBER 2002-REVISED JUNE 2007







LOW-POWER DISSIPATION ADSL LINE DRIVER

FEATURES

- Low-Power Dissipation Increases ADSL Line Card Density
- Low THD of -88 dBc (100 Ω, 1 MHz)
- Low MTPR Driving +20 dBm on the Line
 - -76 dBc With High Bias Setting
 - -74 dBc With Low Bias Setting
- Wide Output Swing of 44 V_{PP} Differential Into a 200-Ω Differential Load (V_{CC} = ±12 V)
- High Output Current of 600 mA (Typ)
- Wide Supply Voltage Range of ±5 V to ±15 V
- Pin Compatible with EL1503C and EL1508C
 - Multiple Package Options
- Multiple Power Control Modes
 - 11 mA/ch Full Bias Mode
 - 7.5 mA/ch Mid Bias Mode
 - 4 mA/ch Low Bias Mode
 - 0.25 mA/ch Shutdown Mode
 - IAD. Pin for User Controlled Bias Current
 - Stable Operation Down to 1.8 mA/ch
- Low Noise for Increased Receiver Sensitivity
 - 3.2 nV/√Hz Voltage Noise
 - 1.5 pA/√Hz Noninverting Current Noise
 - 10 pA/√Hz Inverting Current Noise

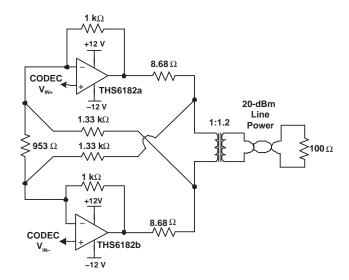
APPLICATIONS

Ideal for Full Rate ADSL Applications

DESCRIPTION

The THS6182 is a current feedback differential line driver ideal for full rate ADSL systems. Its extremely low-power dissipation is ideal for ADSL systems that must achieve high densities in ADSL central office rack applications. The unique architecture of the THS6182 allows the quiescent current to be much lower than existing line drivers while still achieving high linearity without the need for excess open loop gain. Fixed multiple bias settings of the amplifiers allow for enhanced power savings for line lengths where the full performance of the amplifier is not required. To allow for even more flexibility and power savings, an I_{ADI} pin is available to further lower the bias currents while maintaining stable operation with as little as 1.8 mA per channel. The wide output swing of 44 V_{PP} differentially with ±12-V power supplies allows for more dynamic headroom, keeping distortion at a minimum. With a low 3.2 nV/ $\sqrt{\text{Hz}}$ voltage noise coupled with a low 10 pA/ \sqrt{Hz} inverting current noise, the THS6182 increases the sensitivity of the receive signals, allowing for better margins and reach.

TYPICAL ADSL CO-LINE DRIVER CIRCUIT USING ACTIVE IMPEDANCE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PRODUCT	PACKAGE ⁽¹⁾	PACKAGE CODE	SYMBOL	ORDER NUMBER	TRANSPORT MEDIA	
THS6182RHF	Leadless 24-pin	RHF-24	6182	THS6182RHFR	Tape and reel (3000 devices)	
IN30102KHF	4, mm x 5, mm PowerPAD™	КПГ-24	0102	THS6182RHFT	Tape and reel (250 devices)	
				THS6182D	Tube (40 devices)	
THS6182D	SOIC-16	D-16	THS6182	THS6832DR	Tape and reel (2500 devices)	
	SOIC-20			THS6182DW	Tube (25 devices)	
THS6182DW		DW-20	THS6182	THS6182DWR	Tape and reel (2000 devices)	
				THS6182DWP	Tube (25 devices)	
THS6182DWP	SOIC-20 PowerPAD	DWP-20	THS6182	THS6182DWPR	Tape and reel (2000 devices)	

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PACKAGE DISSIPATION RATINGS(1)

PACKAGE	PowerPAD SOLDERED ⁽²⁾ θ _{JA}	PowerPAD NOT SOLDERED ⁽³⁾	θјс
RHF-24 ⁽²⁾	32°C/W	74°C/W	1.7°C/W
D-16		62.9°C/W	25.7°C/W
DW-20		45.4°C/W	16.4°C/W
DWP-20 ⁽²⁾	21.5°C/W	43.9°C/W	0.37°C/W

⁽¹⁾ θ_{JA} values shown are typical for standard test PCBs only.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
\/ to \/	Cumply voltage	Dual supply	±5	±12	±15	V
V _{CC+} to V _{CC-}	Supply voltage	Single supply	10	24	30	V

⁽²⁾ For high-power dissipation applications, use of the PowerPAD package with the PowerPad on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage and/or reduce the lifetime the device. See TI technical brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.

⁽³⁾ Use of packages without the PowerPAD or not soldering the PowerPAD to the PCB, should be limited to low-power dissipation applications.



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1)

ELECTRICAL		THS6132
V _{CC}	Supply voltage	±16.5 V
V _I	Input voltage	±V _{CC}
Io	Output current	1000 mA
V _{IO}	Differential input voltage	±2 V
THERMAL		
т	Maximum junction temperature, any condition	150°C
T _J	Maximum junction temperature, continuous operation, long term reliability (2)	125°C
T _{stg}	Storage temperature	65°C to 150°C
ESD		
	НВМ	2000 V
ESD ratings	CDM	1500 V
	MM	200 V

⁽¹⁾ The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those ispecified is not implied.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ±12 V, R_F = 2 k Ω , Gain = +5, I_{ADJ} = Bias1 = Bias2 = 0 V, R_L = 50 Ω (unless otherwise noted)

	PARAMETE	R	TEST (TEST CONDITIONS				
NOISE/	DISTORTION PERFOR							
MTPR	Multitone power ratio		Gain = +9.5, 163 kHz to 1.1 M +20 dBm Line Power, See Fig		-76		dBc	
Receive band spill-over			Gain =+5, 25 kHz to 138 kHz see Figure 1 for circuit	with MTPR signal applied,	-95		dBc	
			Ond because asia	Differential load = 200 Ω	-88		dBc	
HD	Harmonic distortion, V _{O(PP)} = 2 V		2 nd harmonic	Differential load = 50Ω	-70			
пр	f = 1 MHz		Ord I	Differential load = 200 Ω	-107		-10-	
			3 rd harmonic	Differential load = 50Ω	-84		dBc	
V _n	Input voltage noise		V _{CC} = ±5 V, ±12 V, ±15 V, f =	V _{CC} = ±5 V, ±12 V, ±15 V, f = 100 kHz			nV/√ Hz	
		+Input	V .5V .46V .45V (A / /!	
In	Input current noise	-Input	$V_{CC} = \pm 5 \text{ V}, \pm 12 \text{ V}, \pm 15 \text{ V}, f =$	100 KHZ	10		pA/√ Hz	
		f = 1 MHz, V _{O(PP)} = 2 V,	$R_L = 100 \Omega$	-65		dBc		
1	Crosstalk		$f = 1 \text{ MHz}, V_{O(PP)} = 2 \text{ V}, V_{CC} = \pm 5 \text{ V}, \pm 12 \text{ V}, \pm 15 \text{ V}$	$R_L = 25 \Omega$	-60		dBc	

²⁾ The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.



ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ± 12 V, R_F = 2 k Ω , Gain = +5, I_{ADJ} = Bias1 = Bias2 = 0 V, R_L = 50 Ω (unless otherwise noted)

PARAMETER		TES ⁻	T CONDITIONS	MIN	TYP	MAX	UNIT	
OUTPU	T CHARACTERISTICS							
		V 15.V	R _L = 100 Ω	±3.9	±4.1		V	
		$V_{CC} = \pm 5 \text{ V}$	$R_L = 25 \Omega$	±3.7	±3.9		V	
V	Oin also and ad autout walks as a suite a	V 140 V	R _L = 100 Ω	±10.7	±11		V	
Vo	Single-ended output voltage swing	$V_{CC} = \pm 12 \text{ V}$	$R_L = 25 \Omega$	±10	±10.6		V	
		V 145 V	R _L = 100 Ω	±13.5	±13.9		V	
		$V_{CC} = \pm 15 \text{ V}$	$R_L = 25 \Omega$	±12.7	±13.4		V	
		$R_L = 5 \Omega$	V _{CC} = ±5 V	±350	±400			
lo	Output current (1)	D 40.0	V _{CC} = ±12 V	±450	±600		mA	
		$R_L = 10 \Omega$	V _{CC} = ±15 V	±450	±600			
I _(SC)	Short-circuit current ⁽¹⁾	$R_L = 1 \Omega$	V _{CC} = ±12 V		1000		mA	
	Output resistance	Open-loop			6		Ω	
	Output resistance—terminate mode	f = 1 MHz,	Gain = +10		0.05		Ω	
	Output resistance—shutdown mode	f = 1 MHz,	Open-loop		8.5		kΩ	
POWER	SUPPLY					ų.		
.,	0	Dual supply		±4	±12	±16.5		
V _{CC}	Operating range	Single supply	8	24	33	V		
		V _ + 5 V	T _A = 25°C		9.7	10.7	.7	
	Quiescent current (each driver) $^{(2)}$ Full-bias mode (Bias-1 = 0, Bias-2 = 0) (Trimmed with $V_{CC} = \pm 12 \text{ V}$ at 25°C)	$V_{CC} = \pm 5 \text{ V}$	T _A = full range			11.7	mA	
		V -+12.V	T _A = 25°C		11	12	mA	
		V _{CC} = ± 12 V	T _A = full range			12.5		
Icc		V 145 V	T _A = 25°C		11.5	12.5	A	
		$V_{CC} = \pm 15 \text{ V}$ $T_A = \text{full range}$				13	mA	
		Mid; Bias-1 - 1, Bias-2 = 0		7.5	8.5			
	Quiescent current (each driver) Variable bias modes, V _{CC} = ±12 V	Low; Bias-1 = 0, Bias-2 = 1		4	5	mA		
	variable blackmodes, v _{CC} = ±12 v	Shutdown; Bias-1 = 1, Bias-	Shutdown; Bias-1 = 1, Bias-2 = 1					
		$V_{CC} = \pm 5 \text{ V},$	T _A = 25°C	-50	-56			
PSRR	Dower cumply rejection ratio	$\Delta V_{CC} = \pm 0.5 \text{ V}$	T _A = full range	-47			dB	
FORK	Power supply rejection ratio	$V_{CC} = \pm 12 \text{ V}, \pm 15 \text{ V},$	T _A = 25°C	-56	-60		иБ	
		$\Delta V_{CC} = \pm 1 \text{ V}$	T _A = full range	-53				
DYNAM	IC PERFORMANCE							
			Gain = +1, RF = 1.2 k Ω		100			
		R _L = 100 Ω	Gain = +2, RF = 1 k Ω		80		MHz	
DW		KL = 100 22	Gain = +5, RF = 1 k Ω		35		IVITIZ	
	Single-ended small-signal bandwidth		Gain = +10, RF = 1 k Ω	20				
BW	$(-3 \text{ dB}), V_0 = 0.1 \text{ Vrms}$		Gain = +1, RF = 1.5 kΩ		65			
		P 25 O	Gain = +2, RF = 1 k Ω		60		MHz	
		$R_L = 25 \Omega$	Gain = +5, RF = 1 k Ω		40		IVII IZ	
			Gain = +10, RF = 1 $k\Omega$		22			
SR	Single-ended slew rate (3)	$V_{O} = 10 V_{PP},$	Gain = +5		450		V/µs	

⁽¹⁾ A heatsink is required to keep the junction temperature below absolute maximum rating when an output is heavily loaded or shorted. See Absolute Maximum Ratings section for more information.

 ⁽²⁾ Approximately 0.5 mA (total) flows from V_{CC+} to GND for internal logic control bias.
 (3) Slew rate is defined from the 25% to the 75% output levels.



ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ± 12 V, R_F = 2 k Ω , Gain = +5, I_{ADJ} = Bias1 = Bias2 = 0 V, R_L = 50 Ω (unless otherwise noted)

	PARAMETER	TEST (TEST CONDITIONS				UNIT
DC PER	FORMANCE	<u>'</u>		<u>'</u>		'	
	land offer to the co		T _A = 25°C		1	20	
	Input offset voltage		T _A = full range			25	.,
Vos	Differential effect voltage	V _{CC} = ±5 V, ±12 V, ±15 V	T _A = 25°C		0.5	10	mV
	Differential offset voltage		T _A = full range			15	
	Offset drift		T _A = full range		50		μV/°C
			T _A = 25°C		8	15	
	-Input bias current		T _A = full range			20	
I _{IB}		$V_{CC} = \pm 5 \text{ V}, \pm 12 \text{ V}, \pm 15 \text{ V}$	T _A = 25°C		8	15	μΑ
	+Input bias current		T _A = full range			20	
Z _{OL}	Open loop transimpedance	$R_L = 1 \text{ k}\Omega, V_{CC} = \pm 12 \text{ V}, \pm 15 \text{ V}$	/		900		kΩ
INPUT C	CHARACTERISTICS						
			T _A = 25°C	±2.7	±3		
		$V_{CC} = \pm 5 \text{ V}$	T _A = full range	±2.6			V
.,	Input common-mode voltage range	V 140.V	T _A = 25°C	±9.5	±9.8		
V_{ICR}		$V_{CC} = \pm 12 \text{ V}$	T _A = full range	±±9.3			V
			T _A = 25°C	±12.4	±12.7		
		$V_{CC} = \pm 15 \text{ V}$	T _A = full range	±12.1			V
			T _A = 25°C	48 54			
CMRR	Common-mode rejection ratio	$V_{CC} = \pm 5 \text{ V}, \pm 12 \text{ V}, \pm 15 \text{ V}$ $T_A = \text{full range}$		44			dB
_		+Input					kΩ
R _I	Input resistance	-Input			30		Ω
Ci	Input capacitance				1.7		pF
LOGIC (CONTROL CHARACTERISTICS	<u> </u>					
V _{IH}	Bias pin voltage for logic 1	D. I. II. A. OND. I. II.		2			
V _{IL}	Bias pin voltage for logic 0	Relative to GND pin voltage				0.8	V
I _{IH}	Bias pin current for logic 1	V _{IH} = 3.3 V, GND = 0 V			4	30	μΑ
I _{IL}	Bias pin current for logic 0	V _{IL} = 0.5 V, GND = 0 V			1	10	μΑ
	Transition time, logic 0 to logic 1 ⁽⁴⁾				1		μs
	Transition time, logic 1 to logic 0 ⁽⁴⁾				1		μs

⁽⁴⁾ Transition time is defined as the time from when the logic signal is applied to the time when the supply current has reached half its final

LOGIC TABLE(1)(2)

BIAS-1	BIAS-2	FUNCTION	DESCRIPTION
0	0	Full bias mode	Amplifiers ON with lowest distortion possible (default state)
1	0	Mid bias mode	Amplifiers ON with power savings with a reduction in distortion performance
0	1	Low bias mode	Amplifiers ON with enhanced power savings and a reduction of distortion performance
1	1	Shutdown mode	Amplifiers OFF and output has high impedance

⁽¹⁾ The default state for all logic pins is a logic zero (0). (2) The GND pin useable range is from V_{CC} - to $(V_{CC+}$ - 4 V).



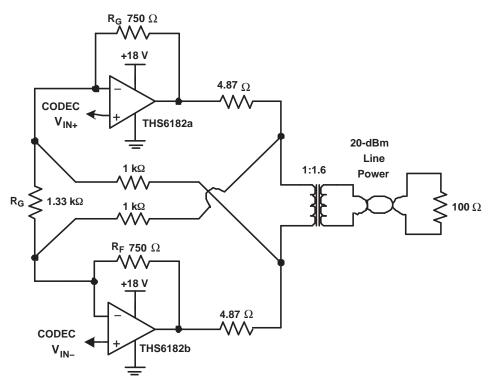
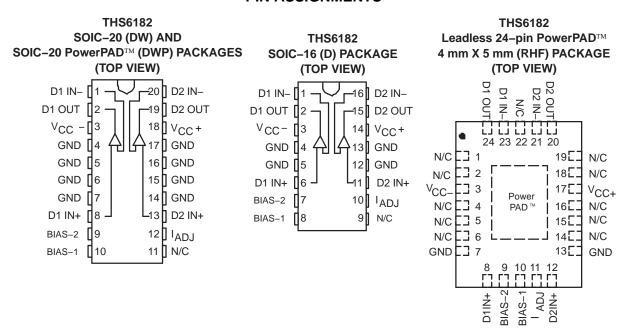


Figure 1. Single-Supply ADSL CO Line Driver Circuit Utilizing Active Impedance (SF = 4)

PIN ASSIGNMENTS



A. The PowerPAD is electrically isolated from all active circuity and pins. Connection of the PowerPAD to the PCB ground plane is highly recommended, although not required, as this plane is typically the largest copper plane on a PCB. The thermal performance will be better with a large copper plane than a small one.



TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Output voltage headroom	vs Output current	2
Common-mode rejection ratio	vs Frequency	3
Crosstalk	vs Frequency	4
Total quiescent current		5
Large signal output amplitude	vs Frequency	6-8
Voltage and current noise	vs Frequency	9
Overdrive recovery		10
Power supply rejection ratio	vs Frequency	11
Output amplitude	vs Frequency	12-37
Slew rate	vs Output voltage	38
Closed-loop output impedance	vs Frequency	39
Quiescent current	vs Supply voltage	40
Quiescent current	vs Temperature	41
Common-mode rejection ratio	vs Common-mode voltage	42
Input bias current	vs Temperature	43
Input offset voltage	vs Temperature	44
2nd Harmonic distribution	vs Frequency	45-52
3rd Harmonic distribution	vs Frequency	53-60
2nd Harmonic distribution	vs Output voltage	61-64
3rd Harmonic distribution	vs Output voltage	65-68

OUTPUT VOLTAGE HEADROOM VS OUTPUT CURRENT

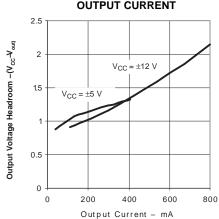


Figure 2.

COMMON-MODE REJECTION RATIO VS FREQUENCY

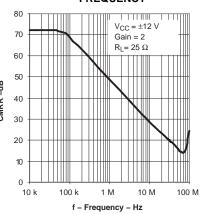


Figure 3.

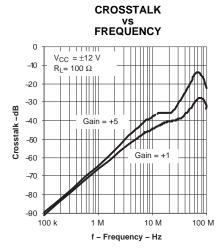


Figure 4.

0

0.01

0.1



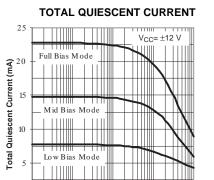


Figure 5.

Rset to $\text{GND-}k\Omega$

100

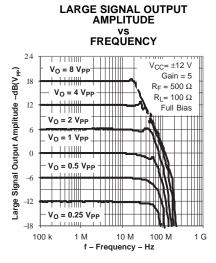
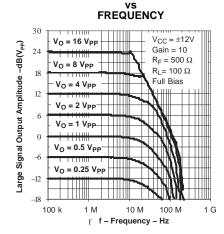


Figure 6.

VOLTAGE AND CURRENT NOISE



LARGE SIGNAL OUTPUT AMPLITUDE

Figure 7.



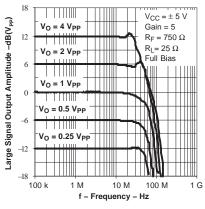


Figure 8.

FOR THE PARTY HE PART

Figure 9.

1 k

f - Frequency - Hz

10 k

100 k

10

100

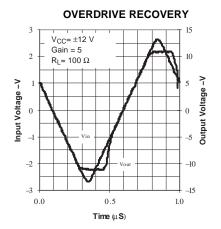


Figure 10.

POWER SUPPLY REJECTION RATIO VS FREQUENCY

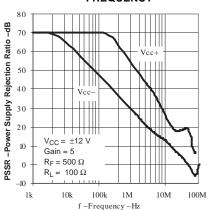


Figure 11.

OUTPUT AMPLITUDE vs FREQUENCY

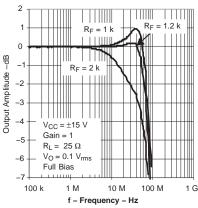


Figure 12.

OUTPUT AMPLITUDE vs FREQUENCY

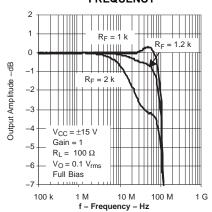


Figure 13.



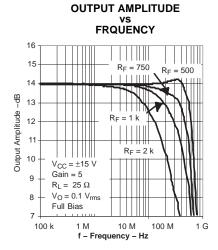


Figure 14.

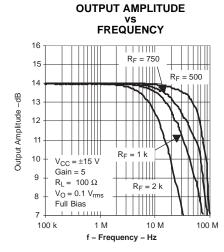


Figure 15.

OUTPUT AMPLITUDE

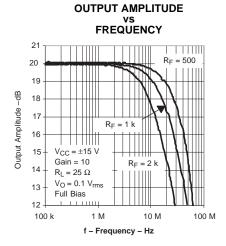


Figure 16.

OUTPUT AMPLITUDE

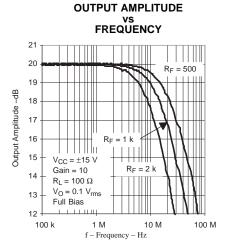


Figure 17.

OUTPUT AMPLITUDE

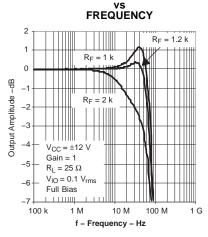


Figure 18.

OUTPUT AMPLITUDE

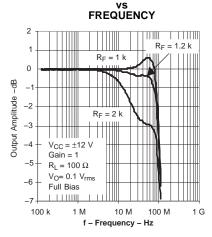


Figure 19.

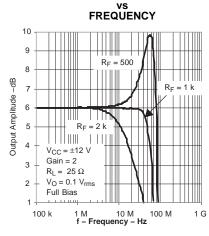


Figure 20.

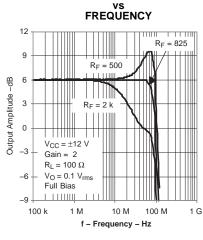


Figure 21.

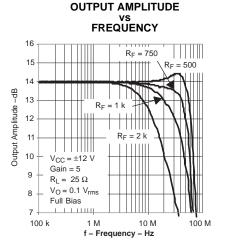


Figure 22.



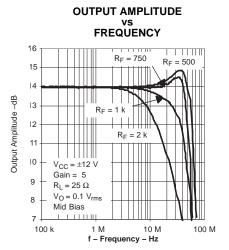
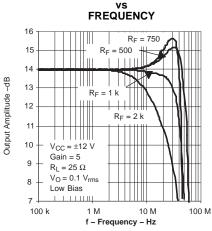


Figure 23.



OUTPUT AMPLITUDE

Figure 24.

OUTPUT AMPLITUDE

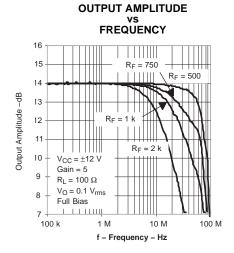


Figure 25.

OUTPUT AMPLITUDE

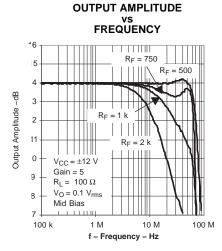


Figure 26.

OUTPUT AMPLITUDE

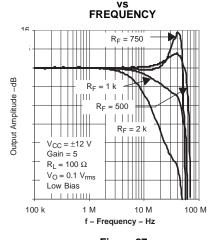


Figure 27.

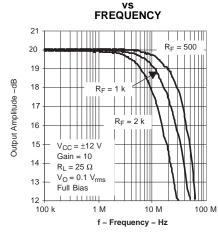


Figure 28.

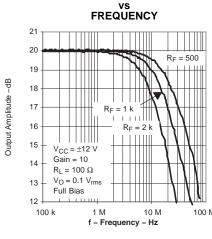


Figure 29.

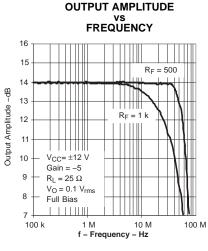


Figure 30.

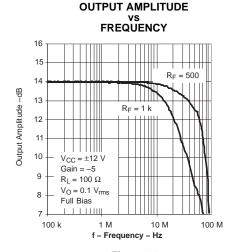


Figure 31.



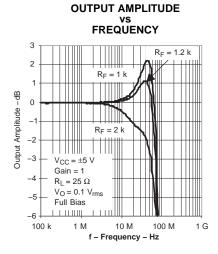


Figure 32.

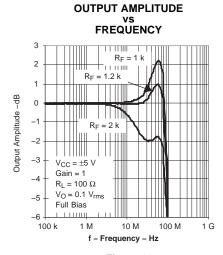


Figure 33.

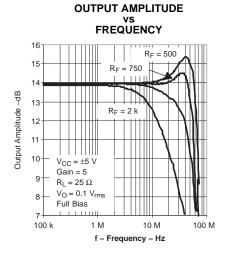


Figure 34.

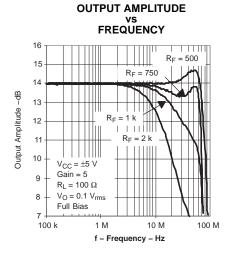


Figure 35.

SLEW RATE

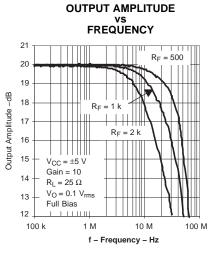


Figure 36.

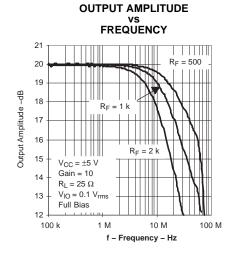


Figure 37.

QUIESCENT CURRENT

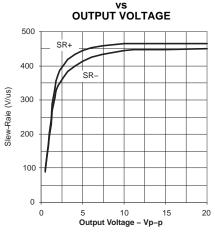


Figure 38.

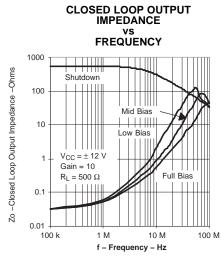


Figure 39.

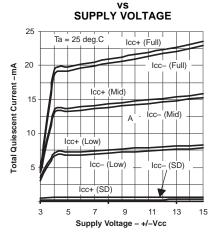
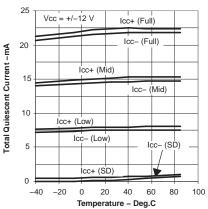


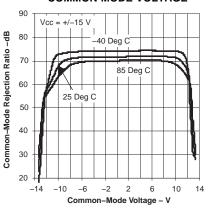
Figure 40.







COMMON-MODE REJECTION RATIO
VS
COMMON-MODE VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE

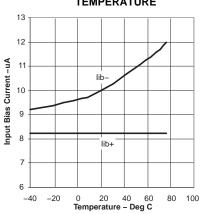
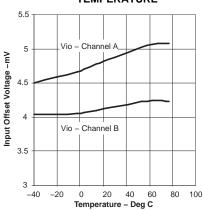


Figure 41.

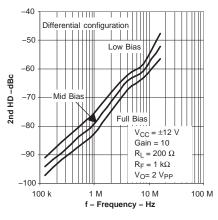
Figure 42.

Figure 43.





2ND HARMONIC DISTORTION VS FREQUENCY



2ND HARMONIC DISTORTION

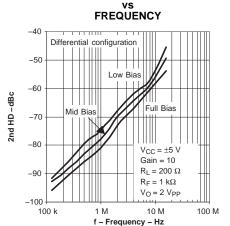
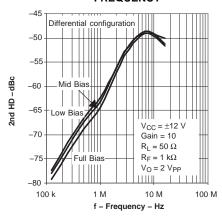


Figure 44.

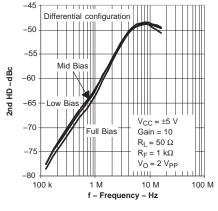
Figure 45.

Figure 46.

2ND HARMONIC DISTORTION VS FREQUENCY



2ND HARMONIC DISTORTION VS FREQUENCY



2ND HARMONIC DISTORTION VS FREQUENCY

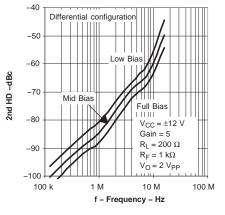
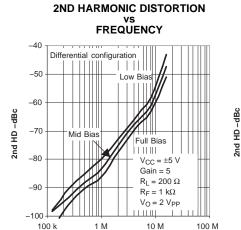


Figure 47. Figure 48.

Figure 49.







FREQUENCY -45 Differential configuration -50 -50 Mid Bias

2ND HARMONIC DISTORTION

-65

Figure 51.

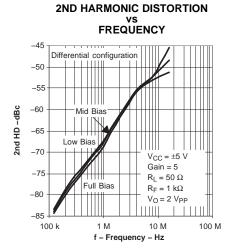


Figure 52.

3RD HARMONIC DISTORTION VS FREQUENCY

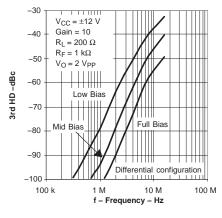


Figure 53.

3RD HARMONIC DISTORTION VS FREQUENCY

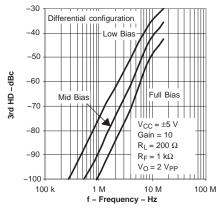


Figure 54.

3RD HARMONIC DISTORTION vs FREQUENCY

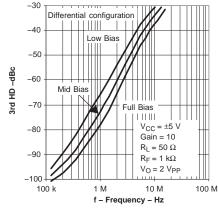


Figure 55.

3RD HARMONIC DISTORTION VS FREQUENCY

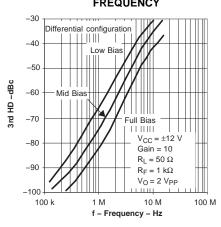


Figure 56.

3RD HARMONIC DISTORTION vs FREQUENCY

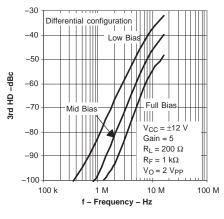


Figure 57.

3RD HARMONIC DISTORTION VS FREQUENCY

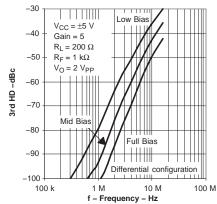
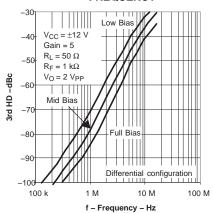


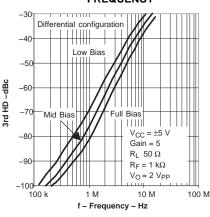
Figure 58.



3RD HARMONIC DISTORTION VS FREQUENCY



3RD HARMONIC DISTORTION
VS
FREQUENCY



2ND HARMONIC DISTORTION
VS
OUTPUT VOLTAGE

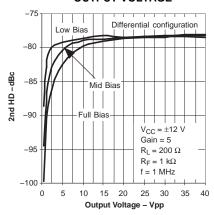
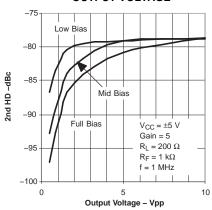


Figure 59.

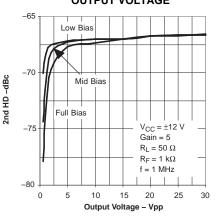
Figure 60.

Figure 61.

2ND HARMONIC DISTORTION VS OUTPUT VOLTAGE



2ND HARMONIC DISTORTION
vs
OUTPUT VOLTAGE



2ND HARMONIC DISTORTION
VS
OUTPUT VOLTAGE

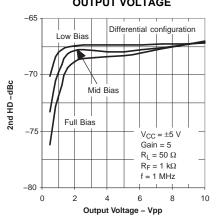
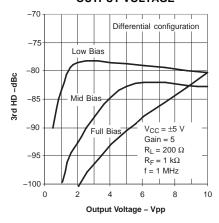


Figure 62.

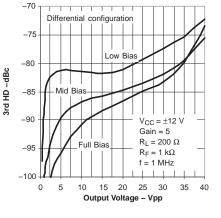
Figure 63.

Figure 64.

3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE



3RD HARMONIC DISTORTION
vs
OUTPUT VOLTAGE



3RD HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

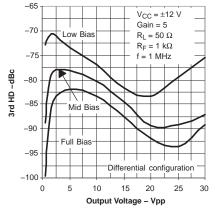


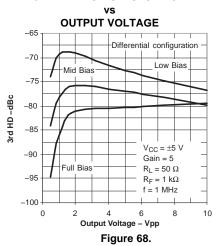
Figure 65.

Figure 66.

Figure 67.



3RD HARMONIC DISTORTION





APPLICATION INFORMATION

The THS6182 contains two independent operational amplifiers. These amplifiers are current feedback topology amplifiers made for high-speed operation. They have been specifically designed to deliver the full power requirements of ADSL and therefore can deliver output currents of at least 400 mA at full output voltage.

The THS6182 is fabricated using Texas Instruments 30-V complementary bipolar process, HVBiCOM. This process provides excellent isolation and high slew rates that result in the device's excellent crosstalk and extremely low distortion.

DEVICE PROTECTION FEATURE

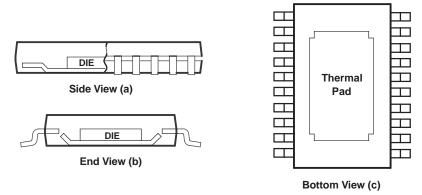
The THS6182 has a built-in thermal protection feature. Should the internal junction temperature rise above approximately 160°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the abnormal condition is fixed, the internal thermal shutdown circuit automatically turns the device back on. This occurs at approximately 145°C, junction temperature. Note that the THS6182 does not have short-circuit protection and care should be taken to minimize the output current below the absolute maximum ratings.

THERMAL INFORMATION

The THS6182 is available in a thermally-enhanced DWP and RHF package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 69(a) and Figure 69(b), for the DWP package example]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 69(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad. Note that the PowerPAD is electronically isolated from the active circuitry and any pins. Thus, the PowerPAD can be connected to any potential voltage within the absolute maximum voltage range. Ideally, connection of the PAD to the ground plane is preferred as the plane typically is the largest copper plane on a PCB.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the *PCB design considerations* section of this document.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



A. The thermal pad is electrically isolated from all terminals in the package.

Figure 69. Views of Thermally Enhanced DWP Package



RECOMMENDED FEEDBACK AND GAIN RESISTOR VALUES

As with all current feedback amplifiers, the bandwidth of the THS6182 is an inversely proportional function of the value of the feedback resistor. The recommended resistors with a ± 12 -V power supply for the optimum frequency response with a 25- Ω load system is 1 k Ω for a gain of 5. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics.

Consistent with current feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independently of the bandwidth constitutes a major advantage of current feedback amplifiers over conventional voltage feedback amplifiers.

It is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third order harmonic distortion increases more than the second order harmonic distortion.

Finally, in a differential configuration as shown in Figure 1, it is important to note that there is a differential gain and a common-mode gain which are different from each other. Differentially, the gain is at $1 + R_F/R_G$. While common-mode gain = 1 due to R_G being connected directly between each amplifier and not to ground. This can lead to potential problems as the stability of the amplifier is determined by R_F . Thus, R_F must be large enough to ensure the common-mode stability, even though a large differential gain may be required.

OFFSET VOLTAGE

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

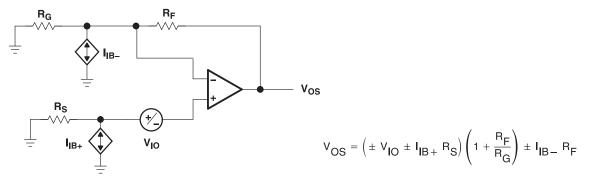


Figure 70. Output Offset Voltage Model

NOISE CALCULATIONS

Noise can cause errors on very small signals. This is especially true for the amplifying small signals. The noise model for current feedback amplifiers (CFB) is the same as voltage feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input while VFB amplifiers usually only specify one noise current parameter. The noise model is shown in Figure 71. This model includes all of the noise sources as follows:

- $e_n = Amplifier internal voltage noise (nV/<math>\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/ $\sqrt{\text{Hz}}$)
- IN- = Inverting current noise (pA/√Hz)
- e_{RX} = Thermal voltage noise associated with each resistor (e_{RX} = 4 kTR_x)



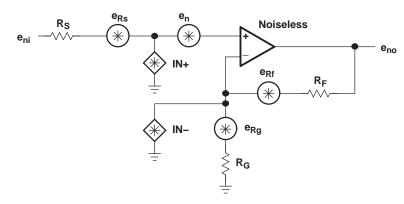


Figure 71. Noise Model

The total equivalent input noise density (eni) is calculated by using the following equation:

$$\mathbf{e}_{ni} = \sqrt{\left(\mathbf{e}_{n}\right)^{2} + \left(\mathsf{IN} + \times \mathsf{R}_{S}\right)^{2} + \left(\mathsf{IN} - \times \left(\mathsf{R}_{F} \, \| \, \mathsf{R}_{G}\right)\right)^{2} + 4 \, \mathsf{kTR}_{S} + 4 \, \mathsf{kT}\left(\mathsf{R}_{F} \, \| \, \mathsf{R}_{G}\right)}$$

Where:

 $k = Boltzmann's constant = 1.380658 \times 10^{-23}$

T = Temperature in degrees Kelvin (273 +°C)

 $R_F \parallel R_G = Parallel resistance of R_F and R_G$

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni} A_{V} = e_{ni} \left(1 + \frac{R_{F}}{R_{G}} \right)$$
 (Noninverting Case)

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing $R_{\rm G}$), the input noise is reduced considerably because of the parallel resistance term.

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6182 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 72. A minimum value of 2 Ω should work well for most applications. For example, in 75- Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.



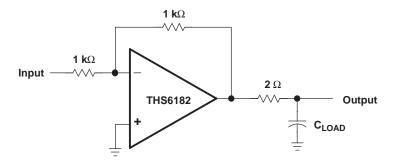


Figure 72. Driving a Capacitive Load

PCB DESIGN CONSIDERATIONS

Proper PCB design techniques in two areas are important to assure proper operation of the THS6182. These areas are high-speed layout techniques and thermal-management techniques. Because the THS6182 is a high-speed part, the following guidelines are recommended.

- Ground plane It is essential that a ground plane be used on the board to provide all components with a low
 inductive ground connection. Although a ground connection directly to a terminal of the THS6012 is not
 necessarily required, it is recommended that the thermal pad of the package be tied to ground. This serves
 two functions. It provides a low inductive ground to the device substrate to minimize internal crosstalk and it
 provides the path for heat removal. Note that the BiCom process is a SOI process and thus, the substrate is
 isolated from the active circuitry.
- Input stray capacitance To minimize potential problems with amplifier oscillation, the capacitance at the
 inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input
 must be as short as possible, the ground plane should be removed under any etch runs connected to the
 inverting input, and external components should be placed as close as possible to the inverting input. This is
 especially true in the noninverting configuration.
- Proper power supply decoupling Use a minimum of a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminal and the ceramic capacitors.
- For a differential configuration as shown in Figure 1, it is recommended that a 0.1-μF or 1-μF capacitor be added across the power supplies (from V_{CC+} to V_{CC-}) as close as possible to the THS6182. This allows for differential currents to flow properly, signficantly reducing even-order harmonic distortion. The 0.1-μF capacitors to ground should also be used as previously stipulated.

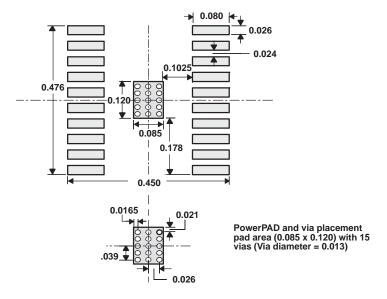
Because of its power dissipation, proper thermal management of the THS6182 is required. Although there are many ways to properly heatsink this device, the following steps illustrate one recommended approach for a multilayer PCB with an internal ground plane utilizing the 20 pin DWP PowerPAD package.

- Prepare the PCB with a top side etch pattern as shown in Figure 73. There should be etch for the leads as well as etch for the thermal pad.
- 2. Place 18 holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
- It is recommended, but not required, to place six more holes under the package, but outside the thermal pad area. These holes are 25 mils in diameter. They may be larger because they are not in the area to be soldered so that wicking is not a problem.
- 4. Connect all 24 holes, the 18 within the thermal pad area and the 6 outside the pad area, to the internal ground plane.
- 5. When connecting these holes to the ground plane, do **not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the



heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6182 package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.

- The top-side solder mask should leave exposed the terminals of the package and the thermal pad area with its five holes. The four larger holes outside the thermal pad area, but still under the package, should be covered with solder mask.
- 7. Apply solder paste to the exposed thermal pad area and all of the operational amplifier terminals.
- With these preparatory steps in place, the THS6182 DWP is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.



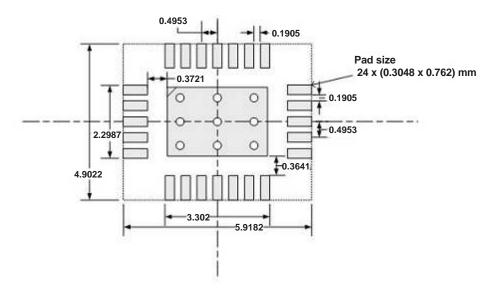
Vias should go through the board connecting the top layer PowerPad to any and all ground planes. (The larger the ground plane, the larger the area to distribute the heat.) Solder resist should be used on the bottom side ground plane in order to prevent wicking of the solder through the vias during the reflow process.

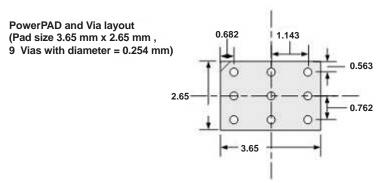
All Units in Inches

Figure 73. 20-Pin DWP PowerPAD PCB Etch and Via Pattern

The RHF package is similar to the DWP package with respect to PCB mounting procedures. The recommended PCB layout is as shown in Figure 74.







Vias should go through the board connecting the top layer PowerPAD to any and all ground planes. The larger the ground plane, the more area to distribute the heat.

Solder resist should be used on the bottom side ground plane to prevent wicking of the solder through the vias during the reflow process.

Figure 74. Suggested PCB Layout

The actual thermal performance achieved with the THS6182 in the 20-pin DWP PowerPAD package depends on the application. In the previous example, if the size of the internal ground plane is approximately 3 inches \times 3 inches, then the expected thermal coefficient, Θ_{JA} , is about 21.5°C/W. (See the Package Dissipation Ratings Table for all other package metrics.) For a given Θ_{JA} , the maximum power dissipation is calculated by the following formula:



$$P_{D} = \left(\frac{T_{MAX}^{-T}A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of THS6182 (watts)

T_{MAX} = Absolute maximum operating junction temperature (125°C)

 T_A = Free-ambient air temperature (°C)

 $\theta_{JA} = \theta_{JC} + \theta_{CA}$

 $\theta_{\text{JC}}\,$ = Thermal coefficient from junction to case. See the Package Dissipation Ratings table.

 θ_{CA} = Thermal coefficient from case to ambient determined by PCB layout and construction.

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package*. This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

GENERAL CONFIGURATIONS

A common error for the first-time CFB user is to create a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration oscillates and is **not** recommended. The THS6182, like all CFB amplifiers, **must** have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 75).

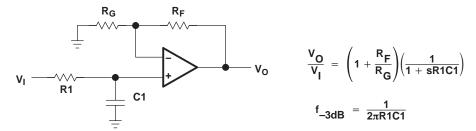


Figure 75. Single-Pole Low-Pass Filter

If a multiple pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 76.



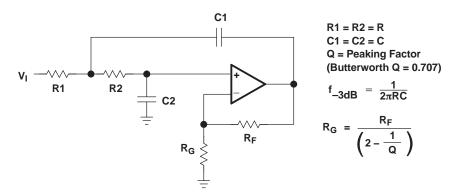


Figure 76. 2-Pole Low-Pass Sallen-Key Filter

EVALUATION BOARD

An evaluation board is available for the THS6182. This board has been configured for proper thermal management of the THS6182. The circuitry has been designed for a typical ADSL application as shown previously in this document. For more detailed information, refer to the *THS6182EVM User's Guide* (literature number SLOU152). To order the evaluation board contact your local TI sales office or distributor.



28-Aug-2010

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
THS6182D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
THS6182DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
THS6182DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
THS6182DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
THS6182DWP	ACTIVE	SO PowerPAD	DWP	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
THS6182DWPG4	ACTIVE	SO PowerPAD	DWP	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
THS6182DWPR	ACTIVE	SO PowerPAD	DWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
THS6182DWPRG4	ACTIVE	SO PowerPAD	DWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
THS6182RHFR	ACTIVE	VQFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
THS6182RHFRG4	ACTIVE	VQFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
THS6182RHFT	ACTIVE	VQFN	RHF	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
THS6182RHFTG4	ACTIVE	VQFN	RHF	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

28-Aug-2010

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL. Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

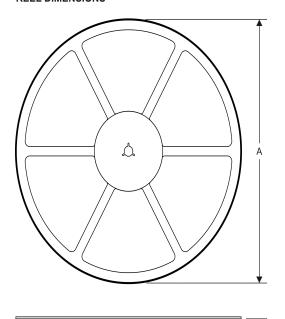
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 16-Feb-2012

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

7 til dillionolollo aro nominar												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6182RHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
THS6182RHFT	VQFN	RHF	24	250	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

www.ti.com 16-Feb-2012



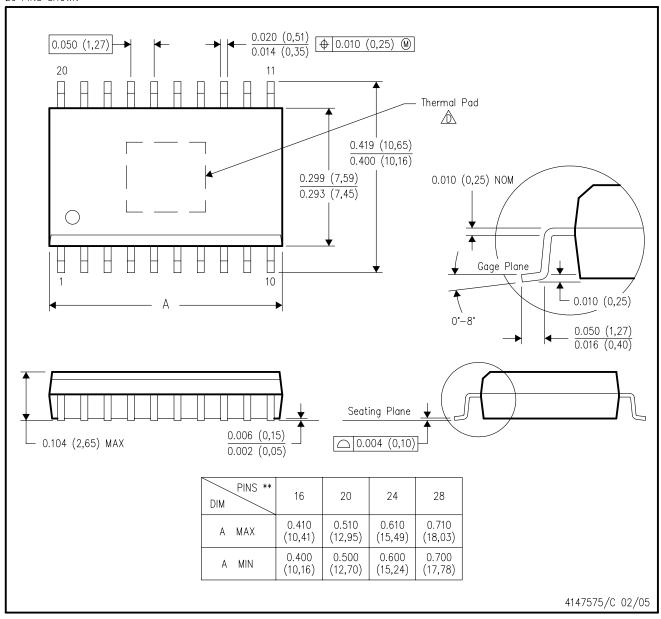
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6182RHFR	VQFN	RHF	24	3000	338.1	338.1	20.6
THS6182RHFT	VQFN	RHF	24	250	338.1	338.1	20.6

DWP (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com http://www.ti.com. See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.



DWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD $^{\mathsf{TM}}$ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

20

11

22

13

14

279

1,91

10

10

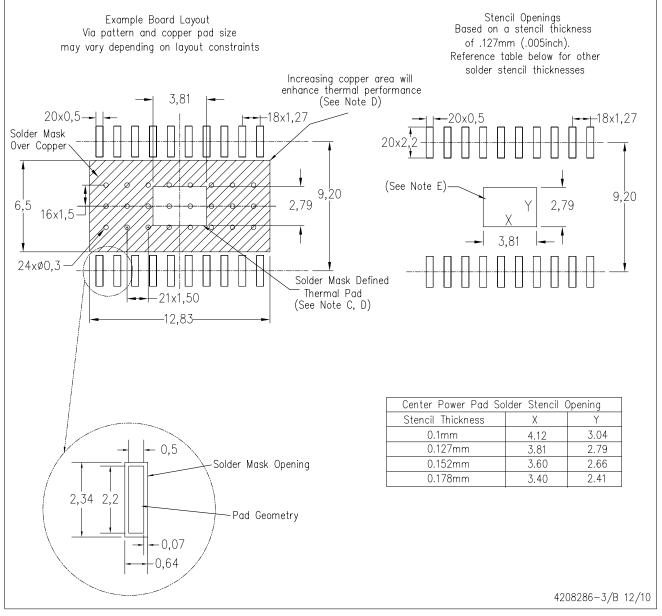
Exposed Thermal Pad Dimensions

4206325–4/E 12/10

NOTE: A. All linear dimensions are in millimeters

DWP (R-PDSO-G20)

PowerPAD™PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste.

PowerPAD is a trademark of Texas Instruments.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



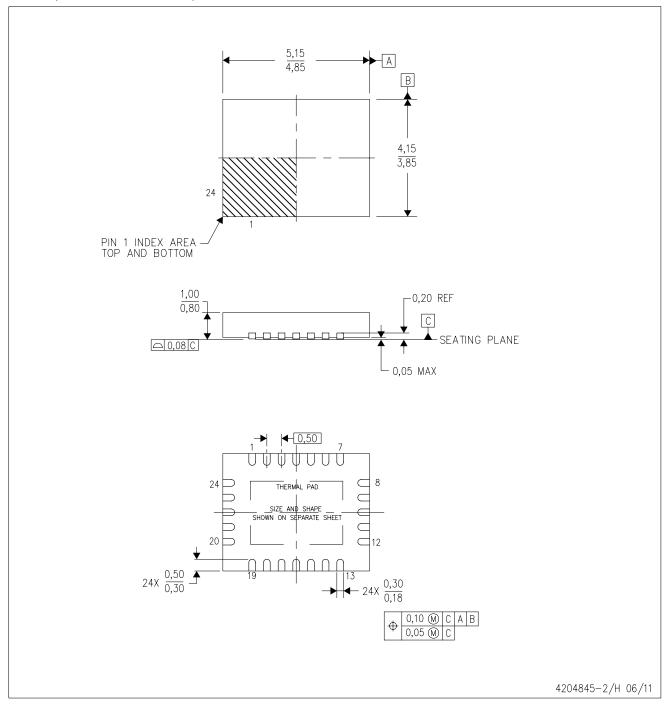
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



RHF (R-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.



RHF(R-PVQFN-N24)

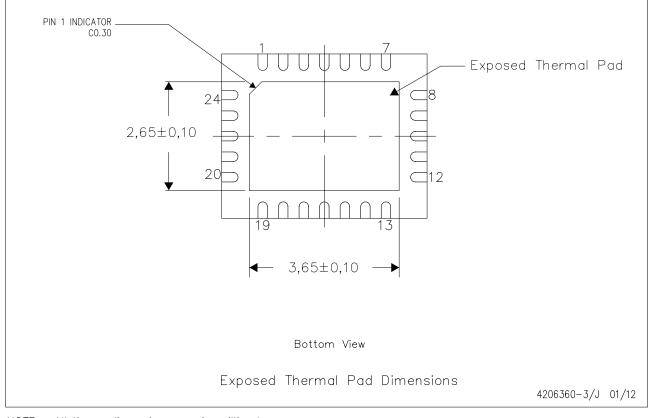
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

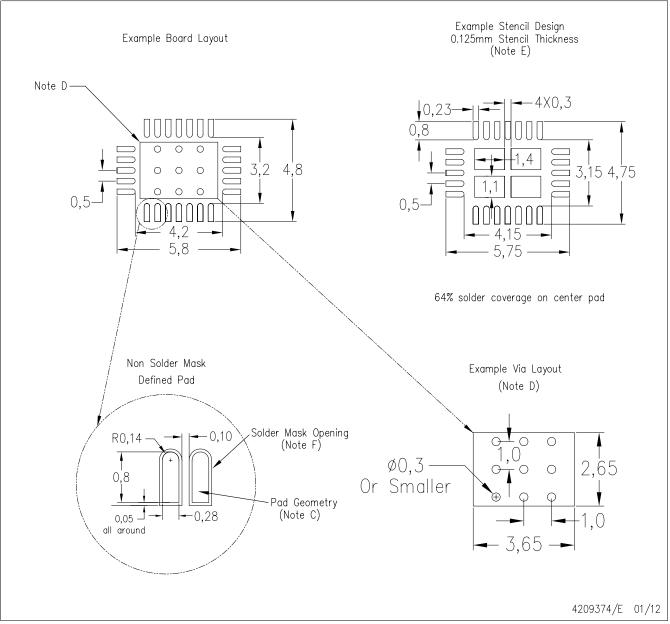


NOTE: All linear dimensions are in millimeters



RHF (R-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

Applications

Automotive and Transportation www.ti.com/automotive

e2e.ti.com

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

		•	
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video

RFID <u>www.ti-rfid.com</u>
OMAP Mobile Processors www.ti.com/omap

Products

Audio

Wireless Connectivity www.ti.com/wirelessconnectivity

www.ti.com/audio

TI E2E Community Home Page

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2012, Texas Instruments Incorporated