

### 2.5 Gbps / 5.0 Gbps / 8.0 Gbps 4 Lane PCI Express **Repeater with Equalization and De-Emphasis**

#### **General Description**

The DS80PCI402 is a low power, 4 lane repeater with 4-stage input equalization, and output de-emphasis driver to enhance the reach of PCI express serial links in board-to-board or cable interconnects. Ideal for x4 (or lower) PCI express configuration, the DS80PCI402 automatically detects and adapts to Gen-1, Gen-2 and Gen-3 data rates for easy system upgrade.

Each channel supports seamless detection and management of the new Gen-3 transmit equalizer coefficients (FIR tap) handshake protocol and PCIe control signals such as transmit idle, beacon etc. without external system intervention. An automatic receive detection circuitry controls the input termination impedance based upon endpoint insertion (hot-plug events). These features guarantee PCIe interoperability at both the electrical and system level, while reducing design complexity.

Powered by National's SiGe BiCMOS process, DS80PCI402 offers programmable transmit de-emphasis (up to 12 dB), transmit VoD (up to 1300 mVp-p) and receive equalization (up to 36 dB) to enable longer distance transmission in lossy copper cables (10m+), or backplanes (40"+) with multiple connectors. The receiver is capable of opening an input eve that is completely closed due to inter-symbol interference (ISI) introduced by the interconnect medium.

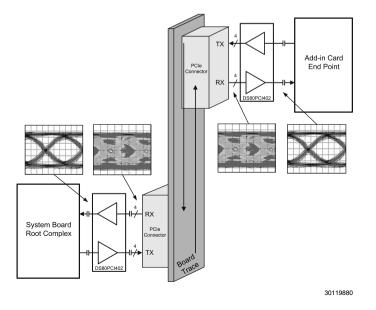
The programmable settings can be applied easily via pins, software (SMBus/I2C) or loaded via an external EEPROM. When operating in the EEPROM mode, the configuration information is automatically loaded on power up, which eliminates the need for an external microprocessor or software driver

With a low power consumption and control to turn-off unused channels, the DS80PCI402 is part of PowerWise family of energy efficient devices.

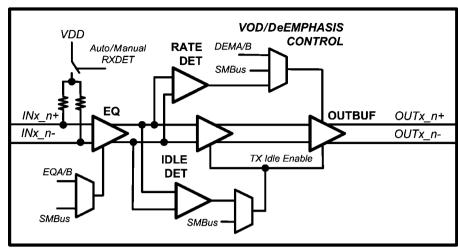
#### Features

- Comprehensive family, proven system inter-operability DS80PCI102 : x1 PCIe Gen-1/2/3 DS80PCI402 : x4 PCIe Gen-1/2/3 DS80PCI800 : x8/x16 PCIe Gen-1/2/3
- Automatic rate detect and adaptation to Gen-1/2/3 speeds
- Seamless support for Gen-3 transmit FIR handshake
- Rate adaptive receive EQ (up to 36 dB), transmit deemphasis (up to 12 dB) only Gen-1/2
- Adjustable Transmit VOD: 0.8 to 1.3 Vp-p (pin mode)
- 0.2 UI of residual deterministic jitter at 8 Gbps after 40" of FR4 or 10m 30awg PCIe Cable
- Low power dissipation with ability to turnoff unused channels: 65 mW/channel
- Automatic receiver detect (hot-plug)
- Multiple configuration modes: Pins/SMbus/Direct-**EEPROM** load
- Flow-thru pinout: 54-pin LLP (10 mm x 5.5 mm, 0.5 mm pitch)
- Single supply voltage: 2.5V or 3.3V (selectable)
- 5 kV HBM ESD rating
- -40 to 85°C operating temperature range

### **Typical Application**



#### Block Diagram - Detail View Of Channel (1 Of 8)



30119886

**Pin Diagram** DEMA0/SDA DEMB1/AD0 DEMA1/SCL DEMB0/AD1 EQB1/AD2 EQB0/AD3 ENSMB PRSNT ٧DD 54 53 49 47 52 50 48 46 51 SMBUS AND CONTROL OUTB\_0+ 1 INB 0+ 45 OUTB\_0-2 44 INB\_0-3 OUTB\_1+ 43 INB 1+ 4 42 OUTB\_1-INB\_1-OUTB 2+ 5 41 VDD OUTB\_2-6 40 INB\_2+ OUTB\_3+ 7 39 INB\_2-OUTB\_3-8 38 INB\_3+ DAP = GND 9 VDD 37 INB\_3-10 36 VDD INA\_0+ 35 [11] OUTA\_0+ INA\_0-34 INA\_1+ 12 OUTA\_0-33 OUTA\_1+ 13 INA\_1-32 OUTA\_1-14 VDD 31 OUTA\_2+ 15 INA 2+ OUTA\_2-INA 2-16 30 17 29 OUTA 3+ INA\_3+ INA\_3-18 28 OUTA\_3-25 26 19 20 21 22 23 24 27 EQA1 EQA0 RATE ALL\_DONE RXDET LPBK N VDD\_SEL SD\_TH/READ\_EN 30119892 DS80PCI402 Pin Diagram 54 lead **Ordering Information** 

### **Pin Descriptions**

Pin Name	Pin Number	I/O, Type	Pin Description
Differential High Spe	ed I/O's		· ·
INB_0+, INB_0- , INB_1+, INB_1-, INB_2+, INB_2-, INB_3+, INB_3-	45, 44, 43, 42 40, 39, 38, 37	1	Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip $50\Omega$ termination resistor connects INB_n+ to VDD and INB_n- to VDD when enabled.
OUTB_0+, OUTB_0-, OUTB_1+, OUTB_1-, OUTB_2+, OUTB_2-, OUTB_3+, OUTB_3-		0	Inverting and non-inverting $50\Omega$ driver outputs with de- emphasis. Compatible with AC coupled CML inputs.
INA_0+, INA_0- , INA_1+, INA_1-, INA_2+, INA_2-, INA_3+, INA_3-	10, 11, 12, 13 15, 16, 17, 18	1	Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip $50\Omega$ termination resistor connects INA_n+ to VDD and INA_n- to VDD when enabled.
OUTA_0+, OUTA_0-, OUTA_1+, OUTA_1-, OUTA_2+, OUTA_2-, OUTA_3+, OUTA_3-		0	Inverting and non-inverting $50\Omega$ driver outputs with de- emphasis. Compatible with AC coupled CML inputs.
Control Pins — Share	ed (LVCMOS)	l	
ENSMB	48	I, LVCMOS	System Management Bus (SMBus) enable pin Tie $1k\Omega$ to VDD = Register Access SMBus Slave mode FLOAT = Read External EEPROM (Master SMBUS Mode) Tie $1k\Omega$ to GND = Pin Mode
ENSMB = 1 (SMBUS I	MODE)		
SCL	50	I, LVCMOS, O, OPEN Drain	ENSMB Master or Slave mode SMBUS clock input pin is enabled (slave mode). Clock output when loading EEPROM configuration (master mode).
SDA	49	I, LVCMOS, O, OPEN Drain	ENSMB Master or Slave mode The SMBus bi-directional SDA pin is enabled. Data input or open drain (pull-down only) output.
AD0-AD3	54, 53, 47, 46	I, LVCMOS	ENSMB Master or Slave mode SMBus Slave Address Inputs. In SMBus mode, these pins are the user set SMBus slave address inputs.
READ_EN	26	I, LVCMOS	When using an External EEPROM, a transition from high to low starts the load from the external EEPROM
ENSMB = 0 (PIN MOD	E)		
EQA0, EQA1 EQB0, EQB1	20, 19 46, 47	I, 4-LEVEL, LVCMOS	EQA[1:0] and EQB[1:0] control the level of equalization of the A/B sides as shown in . The pins are active only when ENSMB is de-asserted (low). Each of the 4 A/B channels have the same level unless controlled by the SMBus control registers. When ENSMB goes high the SMBus registers provide independent control of each lane. The EQB[1:0] pins are converted to SMBUS AD2, AD3 inputs. See <i>Table 2:</i> Equalizer Settings.

Pin Name	Pin Number	I/O, Type	Pin Description
DEMA0, DEMA1	49, 50	I, 4-LEVEL,	DEMA[1:0] and DEMB[1:0] control the level of de-emphasis
DEMB0, DEMB1	53, 54	LVCMOS	of the A/B sides as shown in . The pins are only active wher
			ENSMB is de-asserted (low). Each of the 4 A/B channels have
			the same level unless controlled by the SMBus control
			registers. When ENSMB goes high the SMBus registers
			provide independent control of each lane. The DEMA[1:0]
			pins are converted to SMBUS SCL/SDA and DEMB[1:0] pins
			are converted to AD0, AD1 inputs. See Table 3: Output
			Voltage and De-emphasis Settings
RATE	21	I, 4-LEVEL,	RATE control pin selects GEN 1,2 and GEN 3 operating
		LVCMOS	modes.
			Tie 1k $\Omega$ to GND = GEN 1,2
			Float = Auto Rate select
			Tie $20k\Omega$ to GND = GEN 3 without De-emphasis
			Tie 1k $\Omega$ to VDD = GEN 3 with De-emphasis
	26		Controls the internal Signal Detect Threshold.
SD_TH	20	I, 4-LEVEL, LVCMOS	See Table 5: Signal Detect Threshold Level.
0			
Control Pins — Bo	1	· · · · · · · · · · · · · · · · · · ·	
RXDET	22	I, 4-LEVEL,	The RXDET pin controls the receiver detect function.
		LVCMOS	Depending on the input level, a 50 $\Omega$ or >50K $\Omega$ termination to
			the power rail is enabled.
			See Table 4: RX-Detect Settings.
LPBK	23	I, 4-LEVEL,	Controls the loopback function
		LVCMOS	Tie 1k $\Omega$ to GND = Root Complex Loopback (INA_n to
			OUTB_n
			Float = Normal Operation
			Tie 1k $\Omega$ to VDD = End-point Loopback (INB_n to OUTA_n)
VDD_SEL	25	I, FLOAT	Controls the internal regulator
			Float = 2.5V mode
			Tie GND = 3.3V mode
PRSNT	52	I, LVCMOS	Cable Present Detect input. high when a cable is not present
	-	,	per PCIe Cabling Spec. 1.0. Puts part into low power mode.
			When low (normal operation) part is enabled. See <i>Table 4</i> :
			RX-Detect Settings.
Outputs	Į		
ALL_DONE	27	O, LVCMOS	Valid Register Load Status Output
ALL_DONL	21		HIGH = External EEPROM load failed
			LOW = External EEPROM load passed
Power			
		Daman	
VIN	24	Power	In 3.3V mode, feed 3.3V to VIN
			In 2.5V mode, leave floating.
VDD	9, 14,36, 41,	Power	Power supply pins CML/analog
	51		2.5V mode, connect to 2.5V
			3.3V mode, connect 0.1 uF cap to each VDD pin
GND	DAP	Power	Ground pad (DAP - die attach pad).
Notes:			
LVCMOS inputs with	nout the "Float" c	onditions must b	be driven to a logic low or high at all times or operation is no
guaranteed.			

For 3.3V mode operation, VIN pin = 3.3V and the "VDD" for the 4-level input is 3.3V.

For 2.5V mode operation, VDD pin = 2.5V and the "VDD" for the 4-level input is 2.5V.

Absolute Maximum Ratings (Note 1)	ESD Rating
If Military/Aerospace specified devices are required,	HBM, STD - JESD22-A114F
please contact the Texas Instruments Sales Office/	MM, STD - JESD22-A115-A
Distributors for availability and specifications.	CDM, STD - JESD22-C101-D

Supply Voltage (VDD - 2.5V)	-0.5V to +2.75V	Thermal Resistance				
Supply Voltage (VIN - 3.3V)	-0.5V to +4.0V	θJC				11.5°C/W
LVCMOS Input/Output Voltage	-0.5V to +4.0V	θJA, No Airflow, 4 layer JED	EC		1	19.1°C/W
CML Input Voltage	-0.5V to (VDD+0.5)	For soldering specifications:				
CML Input Current	-30 to +30 mA	www.national.com/ms/MS/MS	S-SOLD	ERIN	G.pdf	
Junction Temperature	125°C		Min	Тур	Max	Units
Storage Temperature	-40°C to +125°C	Supply Voltage (2.5V mode)	2.375	2.5	2.625	V
Lead Temperature Range Soldering	+260°C	Supply Voltgae (3.3V mode)	3.0	3.3	3.6	V
(4 sec.)		Ambient Temperature	-40	25	+85	°C
SQA54A Package		SMBus (SDA, SCL)			3.6	V
Derate SQA54A Package	52.6mW/°C above +25°C	Supply Noise up to 50 MHz ( <i>Note 4</i> )			100	mVp-p

5 kV

150 V

1000 V

Symbol	Parameter	Conditions	Min	Тур	Max	Units
Power	3	•			1	
PD	Power Dissipation	<b>VDD = 2.5 V supply</b> , EQ Enabled, VOD = 1.0 Vp-p, RXDET = 1, PRSNT = 0		500	700	mW
		<b>VIN = 3.3 V supply</b> , EQ Enabled, VOD = 1.0 Vp-p, RXDET = 1, PRSNT = 0		660	900	mW
LVCMOS / I	LVTTL DC Specifications					
V <sub>ih</sub>	High Level Input Voltage		2.0		3.6	V
V <sub>il</sub>	Low Level Input Voltage		0		0.8	V
V <sub>oh</sub>	High Level Output Voltage (ALL_DONE pin)	I <sub>oh</sub> = -4mA	2.0			V
V <sub>ol</sub>	Low Level Output Voltage (ALL_DONE pin)	I <sub>ol</sub> = 4mA			0.4	V
l <sub>ih</sub>	Input High Current (PRSNT pin)	VIN = 3.6 V, LVCMOS = 3.6 V	-15		+15	uA
	Input High Current with internal resistors (4–level input pin)		+20		+150	uA
l <sub>il</sub>	Input Low Current (PRSNT pin)	VIN = 3.6 V, LVCMOS = 0 V	-15		+15	uA
	Input Low Current with internal resistors (4–level input pin)		-160		-40	uA

Symbol	Parameter	Conditions	Min	Тур	Max	Units
CML Receiver	Inputs (IN_n+, IN_n-)			3		
RL <sub>rx-diff</sub>	RX Differential return	0.05 - 1.25 GHz		-16		dB
	loss	1.2 - 2.5 GHz		-16		dB
		2.5 - 4.0 GHz		-14		dB
RLrx-cm	RX Common mode	0.05 - 2.5 GHz		-12		dB
	return loss	2.5 - 4.0 GHz		-8		dB
Zrx-dc	RX DC common mode impedance	Tested at VDD = 2.5 V	40	50	60	Ω
Zrx-diff-dc	RX DC differntial mode impedance	Tested at VDD = 2.5 V	80	100	120	Ω
Vrx-diff-dc	Differential RX peak to peak voltage (VID)	Tested at pins	0.6	1.0	1.2	V
Zrx-high-imp- dc-pos				50		KΩ
Vrx-signal-det- diff-pp Signal detect assert level for active data signal SD_TH = F (float), 0101 pattern at 8 Gbps			180		mVp-p	
Vrx-idle-det- diff-pp	Signal detect de-assert level for electrical idle	SD_TH = F (float), 0101 pattern at 8 Gbps		110		mVp-p

Symbol	Parameter	Conditions	Min	Тур	Max	Units
High Speed Ou	tputs					
V <sub>tx-diff-pp</sub>	Output Voltage Differential Swing	Differential measurement with Out_n+ and OUT_n-, terminated by $50\Omega$ to GND, AC-Coupled, VID = 1.0 Vp-p, DEM0 = 1, DEM1 = 0 ( <i>Note 7</i> )	0.8	1.0	1.2	mVp-p
V <sub>tx-de-ratio_3.5</sub>	TX de-emphasis ratio	VOD = 1.0 Vp-p, DEM0 = 0, DEM1 = R, Gen 1 & 2 modes only		-3.5		dB
V <sub>tx-de-ratio_6</sub>	TX de-emphasis ratio	VOD = 1.0 Vp-p, DEM0 = R, DEM1 = R, Gen 1 & 2 modes only		-6		dB
T <sub>TX-HF-DJ-DD</sub>	TX Dj > 1.5 MHz				0.15	UI
T <sub>TX-HF-DJ-DD</sub>	TX RMS jitter < 1.5 MHz				3.0	ps RMS
T <sub>TX-RISE-FALL</sub>	Transmitter rise/fall time	20% to 80% of differential output voltage	35	45		ps
T <sub>RF-MISMATCH</sub>	Transmitter rise/fall mismatch	20% to 80% of differential output voltage		0.01	0.1	UI
RL <sub>TX-DIFF</sub>	TX Differential return	0.05 - 1.25 GHz		-16		dB
	loss	1.25 - 2.5 GHz		-12		dB
		2.5 - 4 GHz		-11		dB
RL <sub>TX-CM</sub>	TX Common mode	0.05 - 2.5 GHz		-12		dB
_	return loss	2.5 - 4 GHz		-8		dB
Z <sub>TX-DIFF-DC</sub>	DC differential TX impedance			100		Ω
V <sub>TX-CM-AC-PP</sub>	TX AC common mode voltage	VOD = 1.0 Vp-p, DEM0 = 1, DEM1 = 0			100	mVp-p
I <sub>TX-SHORT</sub>	Transmitter short circuit current limit	Total current the transmitter can supply when shorted to VDD or GND		20		mA
V <sub>TX-CM-DC-</sub> ACTIVE-IDLE-DELTA	Absolute delta of DC common mode voltage during L0 and electrical idle				100	mV
V <sub>TX-CM-DC-LINE-</sub> DELTA	Absolute delta of DC common mode voltgae between TX+ and TX-				25	mV
T <sub>TX-IDLE-DATA</sub>	Max time to transition to valid differential signal after idle	VID = 1.0 Vp-p, 8 Gbps		3.5		ns
T <sub>TX-DATA</sub> -IDLE	Max time to transition to idle after differential signal	VID = 1.0 Vp-p, 8 Gbps		6.2		ns
T <sub>PDEQ</sub>	Differential propagation delay	EQ = 00, ( <i>Note 6</i> )		200		ps
T <sub>LSK</sub>	Lane to lane skew	T = 25C, VDD = 2.5V		25		ps
T <sub>PPSK</sub>	Part to part propagation delay skew	T = 25C, VDD = 2.5V		40		ps

Symbol	Parameter	Conditions	Min	Тур	Max	Units
Equalization	n				•	-
DJE1	Residual deterministic jitter at 8 Gbps	35" 4mils FR4, VID = 0.8 Vp-p, PRBS15, <b>EQ = 1F'h,</b> DEM = 0 dB		0.14		UI
DJE2	Residual deterministic jitter at 5 Gbps	35" 4mils FR4, VID = 0.8 Vp-p, PRBS15, <b>EQ = 1F'h,</b> DEM = 0 dB		0.1		UI
DJE3	Residual deterministic jitter at 2.5 Gbps	35" 4mils FR4, VID = 0.8 Vp-p, PRBS15, <b>EQ = 1F'h,</b> DEM = 0 dB	57 4mils FR4, /ID = 0.8 Vp-p, PRBS15, <b>EQ = 1F'h,</b>			UI
DJE4	Residual deterministic jitter at 8 Gbps	10 meters 30 awg cable, VID = 0.8 Vp-p, PRBS15, <b>EQ = 2F'h,</b> DEM = 0 dB		0.16		UI
DJE5	Residual deterministic jitter at 5 Gbps	10 meters 30 awg cable, VID = 0.8 Vp-p, PRBS15, <b>EQ = 2F'h,</b> DEM = 0 dB		0.1		UI
DJE6	Residual deterministic jitter at 2.5 Gbps	10 meters 30 awg cable, VID = 0.8 Vp-p, PRBS15, <b>EQ = 2F'h,</b> DEM = 0 dB		0.05		UI
De-emphasi	is (Gen 1&2 mode only)				-	
DJD1	Residual deterministic jitter at 2.5 Gbps AND 5.0 Gbps	,		0.1		UI
DJD2	Residual deterministic jitter at 2.5 Gbps AND 5.0 Gbps	20" 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 00, VOD = 1.0 Vp-p, <b>DEM = -9 dB,</b>		0.1		UI

**Note 1:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are guaranteed for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

Note 2: Typical values represent most likely parametric norms at VDD = 2.5V, TA = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 3: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 4: Allowed supply noise (mVp-p sine wave) under typical conditions.

Note 5: Guaranteed by device characterization.

Note 6: Propagation Delay measurements will change slightly based on the level of EQ selected. EQ = 00 will result in the shortest propagation delays.

Note 7: In GEN3 mode, the output VOD level is not fixed. It will be adjusted automatically based on the VID input amplitude level. The output VOD level set by DEMA/B[1:0] in GEN3 mode is dependent on the VID level and the frequency content. The DS80PCI800 repeater in GEN3 mode is designed to be transparent, so the TX-FIR (de-emphasis) is passed to the RX to support the PCIe GEN3 handshake negotiation link training.

### Electrical Characteristics — Serial Management Bus Interface

Symbol	Parameter	Conditions	Min	Тур	Max	Units
SERIAL BUS	INTERFACE DC SPECIFICATIONS					•
V <sub>IL</sub>	Data, Clock Input Low Voltage				0.8	V
V <sub>IH</sub>	Data, Clock Input High Voltage		2.1		3.6	V
I <sub>PULLUP</sub>	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V <sub>DD</sub>	Nominal Bus Voltage		2.375		3.6	V
I <sub>LEAK-Bus</sub>	Input Leakage Per Bus Segment	(Note 8)	-200		+200	μA
I <sub>LEAK-Pin</sub>	Input Leakage Per Device Pin			-15		μA
CI	Capacitance for SDA and SCL	(Note 8, Note 9)			10	pF
R <sub>TERM</sub>	External Termination Resistance pull to $V_{DD}$ = 2.5V ± 5% OR 3.3V ±	Pullup V <sub>DD</sub> = 3.3V, ( <i>Note 8, Note 9, Note 10</i> )		2000		Ω
	10%	Pullup V <sub>DD</sub> = 2.5V, ( <i>Note 8, Note 9, Note 10</i> )		1000		Ω
SERIAL BUS	INTERFACE TIMING SPECIFICATI	ONS		<b></b>		•
FSMB	Bus Operating Frequency	ENSMB = VDD (Slave Mode)			400	kHz
		ENSMB = FLOAT (Master Mode)	280	400	520	kHz
TBUF	Bus Free Time Between Stop and Start Condition		1.3			μs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I <sub>PULLUP</sub> , Max	0.6			μs
TSU:STA	Repeated Start Condition Setup Time		0.6			μs
TSU:STO	Stop Condition Setup Time		0.6			μs
THD:DAT	Data Hold Time		0			ns
TSU:DAT	Data Setup Time		100			ns
T <sub>LOW</sub>	Clock Low Period		1.3			μs
T <sub>HIGH</sub>	Clock High Period	(Note 11)	0.6		50	μs
t <sub>F</sub>	Clock/Data Fall Time	(Note 11)			300	ns
t <sub>R</sub>	Clock/Data Rise Time	(Note 11)			300	ns
t <sub>POR</sub>	Time in which a device must be operational after power-on reset	(Note 11, Note 12)			500	ms

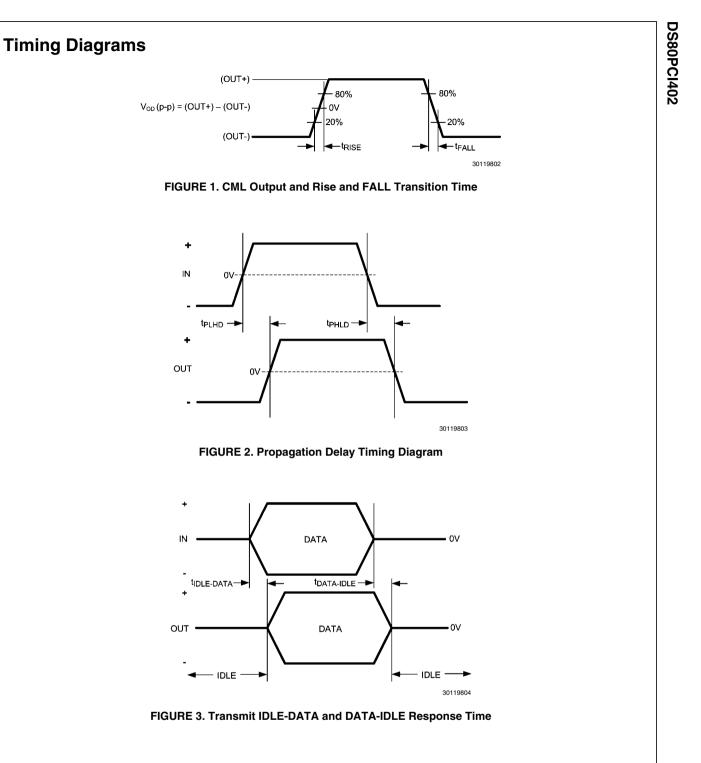
Note 8: Recommended value.

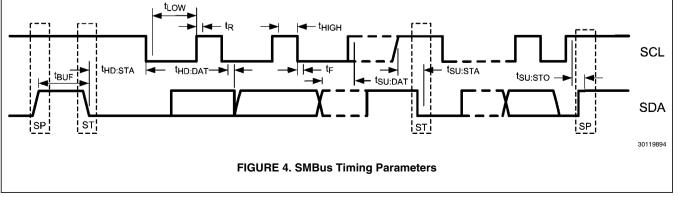
Note 9: Recommended maximum capacitance load per bus segment is 400pF.

Note 10: Maximum termination voltage should be identical to the device supply voltage.

Note 11: Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

Note 12: Guaranteed by Design. Parameter not tested in production.





#### **Functional Descriptions**

The DS80PCI402 is a low power media compensation 4 lane repeater optimized for PCI Express Gen 1/2 and 3. The DS80PCI402 compensates for lossy FR-4 printed circuit board backplanes and balanced cables. The DS80PCI402 operates in 3 modes: Pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) and SMBus Master Mode (ENSMB = float) to load register informations from external EEPROM; please refer to SMBUS Master Mode for additional information.

#### Pin Control Mode:

When in pin mode (ENSMB = 0), equalization and de-emphasis can be selected via pin for each side independently. When de-emphasis is asserted VOD is automatically adjusted per the De- Emphasis table below. The RXDET pins provides automatic and manual control for input termination ( $50\Omega \text{ or } >50K\Omega$ ). RATE setting is also pin controllable with pin selections (Gen 1/2, auto detect and Gen 3). The receiver electrical idle detect threshold is also adjustable via the SD\_TH pin.

#### SMBUS Mode:

When in SMBus mode (ENSMB = 1), the VOD (output amplitude), equalization, de-emphasis, and termination disable features are all programmable on a individual lane basis, instead of grouped by A or B as in the pin mode case. Upon assertion of ENSMB, the EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. The other external control pins (RATE, RXDET and SD\_TH) remain active unless their respective registers are written to and the appropriate override bit is set, in which case they are ignored until ENSMB is driven low (pin mode). On power-up and when ENSMB is driven low all registers are reset to their default state. If PRSNT is asserted while ENSMB is high, the registers retain their current state.

Equalization settings accessible via the pin controls were chosen to meet the needs of most PCIe applications. If additional fine tuning or adjustment is needed, additional equalization settings can be accessed via the SMBus registers. Each input has a total of 256 possible equalization settings. The tables show the 16 setting when the device is in pin mode. When using SMBus mode, the equalization, VOD and de-Emphasis levels are set by registers.

The input control pins have been enhanced to have 4 different levels and provide a wider range of control settings when EN-SMB=0.

#### Table 1: 4–Level Control Pin Settings

Pin Setting	Description	Voltage at Pin
0	Tie 1kΩ to GND	0.03 x VDD
R	Tie 20kΩ to GND	1/3 x VDD
Float	Float (leave pin open)	2/3 x VDD
1	Tie 1kΩ to VDD	0.98 x VDD

Note: The above required resistor value is for a single device. When there are multiple devices connected to the pull-up / pull-down resistor, the value must scale with the number of devices. If 4 devices are connected to a single pull-up or pull-down, the  $1k\Omega$  resistor value should be  $250\Omega$ . For the  $20k\Omega$  to GND, this should also scale to  $5k\Omega$ .

#### 3.3V or 2.5V Supply Mode Operation

The DS80PCI402 has an optional internal voltage regulator to provide the 2.5V supply to the device. In 3.3V mode operation, the VIN pin = 3.3V is used to supply power to the device. The internal regulator will provide the 2.5V to the VDD pins of the device and a 0.1 uF cap is needed at each of the 5 VDD pins for power supply de-coupling (total capacitance should be  $\leq$ 0.5 uF), and the VDD pins should be left open. The VDD\_SEL pin must be tied to GND to enable the internal regulator. In 2.5V mode operation, the VIN pin should be left open and 2.5V supply must be applied to the 5 VDD pins to power the device. The VDD\_SEL pin must be left open (no connect) to disable the internal regulator.

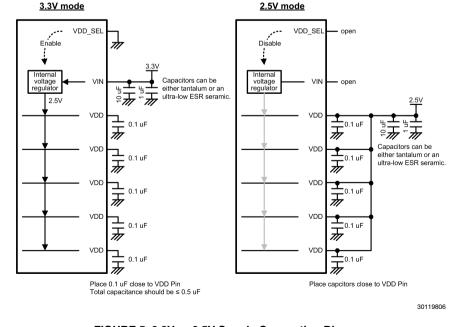


FIGURE 5. 3.3V or 2.5V Supply Connection Diagram

#### **System Information**

When using the DS80PCI402 in CPU systems, there are specific signal integrity settings to ensure signal integrity margin. The settings were achieved with completing extensive testing. Please contact your field representative for more information regarding the testing completed to achieve these settings.

For tuning the in the downstream direction (from CPU to EP). EQ: use the guidelines outlined in table 2. •

#### **Table 2: Equalizer Settings**

- De-Emphasis: use the guidelines outlined in table 3. •
- VOD: use the guidelines outlined in table 3. ٠
- For tuning in the upstream direction (from EP to CPU).
- EQ: use the guidelines outlined in table 2. • •
  - De-Emphasis:
  - For trace lengths < 15" set to -3.5 dB
  - For trace lengths > 15" set to -6 dB
- VOD: set to 900 mV

		•	•				
Level	EQA1	EQA0	EQ – 8 bits [7:0]	dB at	dB at	dB at	Suggested Use
	EQB1	EQB0		1.25 GHz	2.5 GHz	4 GHz	
1	0	0	0000 0000 = 0x00	2.1	3.7	4.9	FR4 < 5 inch trace
2	0	R	0000 0001 = 0x01	3.4	5.8	7.9	FR4 5 inch 5-mil trace
3	0	Float	0000 0010 = 0x02	4.8	7.7	9.9	FR4 5 inch 4-mil trace
4	0	1	0000 0011 = 0x03	5.9	8.9	11.0	FR4 10 inch 5-mil trace
5	R	0	0000 0111 = 0x07	7.2	11.2	14.3	FR4 10 inch 4-mil trace
6	R	R	0001 0101 = 0x15	6.1	11.4	14.6	FR4 15 inch 4-mil trace
7	R	Float	0000 1011 = 0x0B	8.8	13.5	17.0	FR4 20 inch 4-mil trace
8	R	1	0000 1111 = 0x0F	10.2	15.0	18.5	FR4 25 to 30 inch 4-mil trace
9	Float	0	0101 0101 = 0x55	7.5	12.8	18.0	FR4 30 inch 4-mil trace
10	Float	R	0001 1111 = 0x1F	11.4	17.4	22.0	FR4 35 inch 4-mil trace
11	Float	Float	0010 1111 = 0x2F	13.0	19.7	24.4	10m, 30awg cable
12	Float	1	0011 1111 = 0x3F	14.2	21.1	25.8	10m – 12m cable
13	1	0	1010 1010 = 0xAA	13.8	21.7	27.4	
14	1	R	0111 1111 = 0x7F	15.6	23.5	29.0	
15	1	Float	1011 1111 = 0xBF	17.2	25.8	31.4	
16	1	1	1111 1111 = 0xFF	18.4	27.3	32.7	

### Table 3: Output Voltage and De-emphasis Settings

	•		•	•	•	
Level	DEMA1 DEMB1	DEMA0 DEMB0	VOD Vp-p	DEM dB (see note below)	Inner Amplitude Vp-p	Suggested Use
1	0	0	0.8	0	0.8	FR4 <5 inch 4-mil trace
2	0	R	0.9	0	0.9	FR4 <5 inch 4-mil trace
3	0	Float	0.9	- 3.5	0.6	FR4 10 inch 4-mil trace
4	0	1	1.0	0	1.0	FR4 <5 inch 4-mil trace
5	R	0	1.0	- 3.5	0.7	FR4 10 inch 4-mil trace
6	R	R	1.0	- 6	0.5	FR4 15 inch 4-mil trace
7	R	Float	1.1	0	1.1	FR4 <5 inch 4-mil trace
8	R	1	1.1	- 3.5	0.7	FR4 10 inch 4-mil trace
9	Float	0	1.1	- 6	0.6	FR4 15 inch 4-mil trace
10	Float	R	1.2	0	1.2	FR4 <5 inch 4-mil trace
11	Float	Float	1.2	- 3.5	0.8	FR4 10 inch 4-mil trace
12	Float	1	1.2	- 6	0.6	FR4 15 inch 4-mil trace
13	1	0	1.3	0	1.3	FR4 <5 inch 4-mil trace
14	1	R	1.3	- 3.5	0.9	FR4 10 inch 4-mil trace
15	1	Float	1.3	- 6	0.7	FR4 15 inch 4-mil trace
16	1	1	1.3	- 9	0.5	FR4 20 inch 4-mil trace
lote The		amnlitude a	and DEM de-empl	nasis levels are set	t with the DEMA/B[1·	01 pips

Note: The VOD output amplitude and DEM de-emphasis levels are set with the DEMA/B[1:0] pins. The de-emphasis levels are also available in GEN 3 mode when RATE = 1 (tied to VDD).

#### Table 4: RX-Detect Settings

PRSNT#	RXDET	SMBus REG bit[3:2]	Input Termination	Termination sensed on output pins	Comments
0	0	00	High Impedance	Х	Manual RX-Detect, input is high impedance mode
0	Tie 20kΩ to GND	01	High Impedance 50 Ω	High Z until receiver is detected	Auto RX-Detect, outputs test every 12 msec for 600 msec then stops; termination is high-z until detection; once detected input termination is 50 $\Omega$ Reset function by pulsing PRSNT# high for 5 usec then low again
0	Float (Default)	10	High Impedance 50 Ω	High Z until recevier is detected	Auto RX-Detect, outputs test every 12 msec until detection occurs; termination is high-z until detection; once detected input termination is 50 $\Omega$
0	1	11	50 Ω	Х	Manual RX-Detect, input is 50 $\Omega$
1	Х		High Impedance	X	Power down mode, input is high impedance, output drivers are disabled Used to reset RX-Detect State Machine when held high for 5 usec

#### Table 5: Signal Detect Threshold Level

SD_TH	SMBus REG bit [3:2] and [1:0]	Assert Level (typ)	De-assert Level (typ)
0	10	210 mVp-p	150 mVp-p
R	01	160 mVp-p	100 mVp-p
F (default)	00	180 mVp-p	110 mVp-p
1	11	190 mVp-p	130 mVp-p
Note: VDD - 2.5V	25°C and 0101 nattern at 8 Gbns	•	· · · · ·

Note: VDD = 2.5V,  $25^{\circ}C$  and 0101 pattern at 8 Gbps

#### **SMBUS Master Mode**

The DS80PCl402 device supports reading directly from an external EEPROM device by implementing SMBus Master mode. When using the SMBus master mode, the DS80PCl402 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines.

- Set ENSMB = Float enable the SMBUS master mode.
- The external EEPROM device address byte must be 0xA0'h and capable of 400 kHz operation at 2.5V and 3.3V supply.
- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is B0'h.

When tying multiple DS80PCI402 devices to the SDA and SCL bus, use these guidelines to configure the devices.

• Use SMBus AD[3:0] address bits so that each device can loaded it's configuration from the EEPROM. Example below is for 4 device.

U1: AD[3:0] = 0000 = 0xB0'h, U2: AD[3:0] = 0001 = 0xB2'h, U3: AD[3:0] = 0010 = 0xB4'h, U4: AD[3:0] = 0011 = 0xB6'h

- Use a pull-up resistor on SDA and SCL; value = 2k ohms
- Daisy-chain READEN# (pin 26) and ALL\_DONE# (pin 27) from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
- 1. Tie READEN# of the 1st device in the chain (U1) to GND
- 2. Tie ALL\_DONE# of U1 to READEN# of U2
- 3. Tie ALL\_DONE# of U2 to READEN# of U3
- 4. Tie ALL\_DONE# of U3 to READEN# of U4
- 5. Optional: Tie ALL\_DONE# output of U4 to a LED to show the devices have been loaded successfully

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for the DS80PCI402 device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the I2C bus. CRC enable flag to enable/disable CRC checking. If CRC checking is disabled, a fixed pattern (8'hA5) is written/read instead of the CRC byte from the CRC location, to simplify the control. There is a MAP bit to flag the presence of an address map that specifies the configuration data start in the EEPROM. If the MAP bit is not present the configuration data start address is derived from the DS80PCI402 address and the configuration data size. A bit to indicate an EEPROM size > 256 bytes is necessary to properly address the EEPROM. There are 37 bytes of data size for each DS80PCI402 device.

EEPROM Address Byte	SS	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Blt 0
Description	0	CRC EN	Address Map Present	EEPROM > 256 Bytes	RES	DEVICE COUNT [3]	DEVICE COUNT [2]	DEVICE COUNT [1]	DEVICE COUNT [0]
Value	1	0	0	0	0	0	0	0	0
Description		RES	RES	RES	RES	RES	RES	RES	RES
Value		0	0	0	0	0	0	0	0
Description	~	Max EEPROM	Max EEPROM	Max EEPROM	Max EEPROM	Max EEPROM	Max EEPROM	Max EEPROM	Max EEPROM
Value		0 0	0 0		Duist size[4]	0		0 0	Durst size[0]
Description	с	PWDN_ch7	PWDN_ch6	PWDN_ch5	PWDN_ch4	PWDN_ch3	PWDN_ch2	PWDN_ch1	PWDN_ch0
Value	1	0	0	0	0	0	0	0	0
Description	4	lpbk_1	lpbk_0	PWDN_INPUTS	PWDN_OSC	Ovrd_PRSNT	RES	RES	RES
Value		0	0	0	0	0	0	0	0
Description	5	RES	RES	RES	RES	RES	rxdet_btb_en	Ovrd_idle_th	Ovrd_RES
Value		0	0	0	0	0	+	0	0
Description	9	Ovrd_IDLE	Ovrd_RX_DET	Ovrd_RATE	Ovrd_RES	Ovrd_RES	rx_delay_sel_2	rx_delay_sel_1	rx_delay_sel_0
Value		0	0	0	0	0	-	-	-
Description	7	RD_delay_sel_3	RD_delay_sel_2	RD_delay_sel_1	RD_delay_sel_0	ch0_ldle_auto	ch0_ldle_sel	ch0_RXDET_1	ch0_RXDET_0
Value		0	0	0	0	0	0	0	0
Description	8	ch0_BST_7	ch0_BST_6	ch0_BST_5	ch0_BST_4	ch0_BST_3	ch0_BST_2	ch0_BST_1	ch0_BST_0
Value		0	0	1	0	1	+	+	1
Description	6	ch0_Sel_scp	ch0_Sel_mode	ch0_RES_2	ch0_RES_1	ch0_RES_0	ch0_VOD_2	ch0_VOD_1	ch0_VOD_0
Value		+	0	1	0	1	+	0	1
Description	9	ch0_DEM_2	ch0_DEM_1	ch0_DEM_0	ch0_Slow	ch0_idle_tha_1	ch0_idle_tha_0	ch0_idle_thd_1	ch0_idle_thd_0
Value		0	1	0	0	0	0	0	0
Description	÷	ch1_ldle_auto	ch1_ldle_sel	ch1_RXDET_1	ch1_RXDET_0	ch1_BST_7	ch1_BST_6	ch1_BST_5	ch1_BST_4
Value		0	0	0	0	0	0	-	0
Description	12	ch1_BST_3	ch1_BST_2	ch1_BST_1	ch1_BST_0	ch1_Sel_scp	ch1_Sel_mode	ch1_RES_2	ch1_RES_1
Value		-	-	1	+	1	0	+	0
Description	13	ch1_RES_0	ch1_VOD_2	ch1_VOD_1	ch1_VOD_0	ch1_DEM_2	ch1_DEM_1	ch1_DEM_0	ch1_Slow
Value		+	-	0	+	0	+	0	0
Description	4	ch1_idle_tha_1	ch1_idle_tha_0	ch1_idle_thd_1	ch1_idle_thd_0	ch2_ldle_auto	ch2_ldle_sel	ch2_RXDET_1	ch2_RXDET_0
Value		0	0	0	0	0	0	0	0

Description	12	ch2_BST_7	ch2_BST_6	ch2_BST_5	ch2_BST_4	ch2_BST_3	ch2_BST_2	ch2_BST_1	ch2_BST_0
Value									(
Description	9	ch2_Sel_scp	ch2_Sel_mode	ch2_RES_2	ch2_RES_1	ch2_RES_0	ch2_VOD_2	ch2_VOD_1	ch2_VOD_0
Value		-	0	1	0	-	1	0	-
Description	17	ch2_DEM_2	ch2_DEM_1	ch2_DEM_0	ch2_Slow	ch2_idle_tha_1	ch2_idle_tha_0	ch2_idle_thd_1	ch2_idle_thd_0
Value		0	-	0	0	0	0	0	0
Description	48	ch3_ldle_auto	ch3_ldle_sel	ch3_RXDET_1	ch3_RXDET_0	ch3_BST_7	ch3_BST_6	ch3_BST_5	ch3_BST_4
Value		0	0	0	0	0	0	+	0
Description	19	ch3_BST_3	ch3_BST_2	ch3_BST_1	ch3_BST_0	ch3_Sel_scp	ch3_Sel_mode	ch3_RES_2	ch3_RES_1
Value		+	-	1	+	1	0	F	0
Description	20	ch3_RES_0	ch3_VOD_2	ch3_VOD_1	ch3_VOD_0	ch3_DEM_2	ch3_DEM_1	ch3_DEM_0	ch3_Slow
Value		1	-	0	+	0	+	0	0
Description	21	ch3_idle_tha_1	ch3_idle_tha_0	ch3_idle_thd_1	ch3_idle_thd_0	ovrd_fast_idle	en_high_idle_th_n	en_high_idle_th_s	en_fast_idle_n
Value		0	0	0	0	0	0	0	Ŧ
Description	22	en_fast_idle_s	eqsd_mgain_n	eqsd_mgain_s	ch4_ldle_auto	ch4_Idle_sel	ch4_RXDET_1	ch4_RXDET_0	ch4_BST_7
Value		Ŧ	0	0	0	0	0	0	0
Description	23	ch4_BST_6	ch4_BST_5	ch4_BST_4	ch4_BST_3	ch4_BST_2	ch4_BST_1	ch4_BST_0	ch4_Sel_scp
Value		0	1	0	+	1	1	1	1
Description	24	ch4_Sel_mode	ch4_RES_2	ch4_RES_1	ch4_RES_0	ch4_VOD_2	ch4_VOD_1	ch4_VOD_0	ch4_DEM_2
Value		0	1	0	-	1	0	1	0
Description	25	ch4_DEM_1	ch4_DEM_0	ch4_Slow	ch4_idle_tha_1	ch4_idle_tha_0	ch4_idle_thd_1	ch4_idle_thd_0	ch5_ldle_auto
Value		1	0	0	0	0	0	0	0
Description	26	ch5_Idle_sel	ch5_RXDET_1	ch5_RXDET_0	ch5_BST_7	ch5_BST_6	ch5_BST_5	ch5_BST_4	ch5_BST_3
Value		0	0	0	0	0	1	0	Ŧ
Description	27	ch5_BST_2	ch5_BST_1	ch5_BST_0	ch5_Sel_scp	ch5_Sel_mode	ch5_RES_2	ch5_RES_1	ch5_RES_0
Value		1	1	1	+	0	1	0	1
Description	28	ch5_VOD_2	ch5_VOD_1	ch5_VOD_0	ch5_DEM_2	ch5_DEM_1	ch5_DEM_0	ch5_Slow	ch5_idle_tha_1
Value		1	0	1	0	1	0	0	0
Description	29	ch5_idle_tha_0	ch5_idle_thd_1	ch5_idle_thd_0	ch6_ldle_auto	ch6_ldle_sel	ch6_RXDET_1	ch6_RXDET_0	ch6_BST_7
Value		0	0	0	0	0	0	0	0
Description	30	ch6_BST_6	ch6_BST_5	ch6_BST_4	ch6_BST_3	ch6_BST_2	ch6_BST_1	ch6_BST_0	ch6_Sel_scp
Value		0	1	0	1	1	1	1	1
Description	31	ch6_Sel_mode	ch6_RES_2	ch6_RES_1	ch6_RES_0	ch6_VOD_2	ch6_VOD_1	ch6_VOD_0	ch6_DEM_2
Value		0	-	0	Ŧ	-	0	-	0

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Description	32	ch6_DEM_1	ch6_DEM_0	ch6_Slow	ch6_idle_tha_1	ch6_idle_tha_0	ch6_idle_thd_1	ch6_idle_thd_0	ch7_Idle_auto
Value		-	0	0	0	0	0	0	0
Description	33	ch7_ldle_sel	ch7_RXDET_1	ch7_RXDET_0	ch7_BST_7	ch7_BST_6	ch7_BST_5	ch7_BST_4	ch7_BST_3
Value		0	0	0	0	0	1	0	1
Description	34	ch7_BST_2	ch7_BST_1	ch7_BST_0	ch7_Sel_scp	ch7_Sel_mode	ch7_RES_2	ch7_RES_1	ch7_RES_0
Value		+	1	1	1	0	1	0	1
Description	35	ch7_VOD_2	ch7_VOD_1	ch7_VOD_0	ch7_DEM_2	ch7_DEM_1	ch7_DEM_0	ch7_Slow	ch7_idle_tha_1
Value		Ŧ	0	1	0	1	0	0	0
Description	36	ch7_idle_tha_0	ch7_idle_thd_1	ch7_idle_thd_0	iph_dac_ns_1	iph_dac_ns_0	ipp_dac_ns_1	ipp_dac_ns_0	ipp_dac_1
Value		0	0	0	0	0	0	0	0
Description	37	ipp_dac_0	RD23_67	RD01_45	RD_PD_ovrd	RD_Sel_test	RD_RESET_ovrd	PWDB_input_DC	DEM_VOD_ovrd
Value		0	0	0	0	0	0	0	0
Description	38	DEM_ovrd_N2	DEM_ovrd_N1	DEM_ovrd_N0	VOD_ovrd_N2	VOD_ovrd_N1	VOD_ovrd_N0	SPARE0	SPARE1
Value		0	Ŧ	0	1	0	1	0	0
Description	39	DEM_ovrd_S2	DEM_ovrd_S1	DEM_ovrd_S0	VOD_ovrd_S2	VOD_ovrd_S1	VOD_ovrd_S0	<b>SPARE0</b>	SPARE1
Value		0	Ţ	0	1	0	-	0	0

### Table 7: Example of EEPROM for 4Devices using 2 Address Maps

r			
EEPROM			Comments
Address	(Hex)	Data	
0	00	0x43	CRC_EN = 0, Address
			Map = 1, $>256$ bytes = 0,
			Device Count[3:0] = 3
1	01	0x00	
2	02	0x08	EEPROM Burst Size
3	03	0x00	CRC not used
4	04	0x0B	Device 0 Address
			Location
5	05	0x00	CRC not used
6	06	0x0B	Device 1 Address
			Location
7	07	0x00	CRC not used
8	08	0x30	Device 2 Address
			Location
9	09	0x00	CRC not used
10	0A	0x30	Device 3 Address
			Location
11	0B	0x00	Begin Device 0, 1 -
			Address Offset 3
12	0C	0x00	
13	0D	0x04	
14	0E	0x07	
15	0F	0x00	
16	10	0x00	EQ CHB0 = 00
17	10	0xAB	VOD CHB0 = 1.0V
18	12	0x00	DEM CHB0 = 0 (0dB)
19	13		EQ CHB1 = $00$
		0x00	
20	14	0x0A	VOD CHB1 = $1.0V$
21	15	0xB0	DEM CHB1 = 0 (0dB)
22	16	0x00	
23	17	0x00	EQ CHB2 = 00
24	18	0xAB	VOD CHB2 = 1.0V
25	19	0x00	DEM CHB2 = 0 (0dB)
26	1A	0x00	EQ CHB3 = 00
27	1B	0x0A	VOD CHB3 = 1.0V
28	1C	0xB0	DEM CHB3 = 0 (0dB)
29	1D	0x01	
30	1E	0x80	
31	1F	0x01	EQ CHA0 = 00
32	20	0x56	VOD CHA0 = 1.0V
33	21	0x00	DEM CHA0 = 0 (0dB)
34	22	0x00	EQ CHA1 = $00$
35	23	0x00	VOD CHA1 = 1.0V
	23		
36		0x60	DEM CHA1 = 0 (0dB)
37	25	0x00	
38	26	0x01	EQ CHA2 = 00

39	27	0x56	VOD CHA2 = 1.0V
40	28	0x00	DEM CHA2 = 0 (0dB)
41	29	0x00	EQ CHA3 = 00
42	2A	0x15	VOD CHA3 = 1.0V
43	2B	0x60	DEM CHA3 = 0 (0dB)
44	2C	0x00	
45	2D	0x00	
46	2E	0x54	
47	2F	0x54	End Device 0, 1 - Address
47		0,04	Offset 39
48	30	0x00	Begin Device 2, 3 - Address Offset 3
49	31	0x00	
50	32	0x04	
51	33	0x07	
52	34	0x00	
53	35	0x00	EQ CHB0 = 00
54	36	0xAB	VOD CHB0 = 1.0V
55	37	0x00	DEM CHB0 = 0 (0dB)
56	38	0x00	EQ CHB1 = 00
57	39	0x0A	VOD CHB1 = 1.0V
58	3A	0xB0	DEM CHB1 = 0 (0dB)
59	3B	0x00	
60	3C	0x00	EQ CHB2 = 00
61	3D	0xAB	VOD CHB2 = 1.0V
62	3E	0x00	DEM CHB2 = 0 (0dB)
63	3F	0x00	EQ CHB3 = 00
64	40	0x00	VOD CHB3 = 1.0V
65	41	0x0A	DEM CHB3 = 0 (0dB)
66	42	0x01	
67	43	0x80	
68	44	0x00	EQ CHA0 = 00
69	44		VOD CHA0 = 00
		0x56	
70	46	0x00	DEM CHA0 = 0 (0dB)
71	47	0x00	EQ CHA1 = $00$
72	48	0x15	VOD CHA1 = 1.0V
73	49	0x60	DEM CHA1 = 0 (0dB)
74	4A	0x00	
75	4B	0x01	EQ CHA2 = 00
76	4C	0x56	VOD CHA2 = 1.0V
77	4D	0x00	DEM CHA2 = 0 (0dB)
78	4E	0x00	EQ CHA3 = 00
79	4F	0x15	VOD CHA3 = 1.0V
80	50	0x60	DEM CHA3 = 0 (0dB)
81	51	0x00	
82	52	0x00	
83	53	0x54	
84	54	0x54	End Device 2, 3 - Address Offset 39

Note: CRC\_EN = 0, Address Map = 1, >256 byte = 0, Device Count[3:0] = 3. This example has all 8–channels set to EQ = 00 (min boost), VOD = 1.0V, DEM = 0 (0dB) and multiple device can point to the same address map.

### System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SM-Bus 2.0 physical layer specification. ENSMB =  $1k\Omega$  to VDD to enable SMBus slave mode and allow access to the configuration registers.

The DS80PCI402 has the AD[3:0] inputs in SMBus mode. These pins are the user set SMBUS slave address inputs. The AD[3:0] pins have internal pull-down. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is B0'h. Based on the SMBus 2.0 specification, the DS80PCI402 has a 7-bit slave address. The LSB is set to 0'b (for a WRITE). The device supports up to 16 address byte, which can be set with the AD[3:0] inputs. Below are the 16 addresses.

#### **Table 8: Device Slave Address Bytes**

AD[3:0] Settings         Address Bytes (HEX)           0000         B0           0001         B2           0010         B4           0011         B6           0100         B8           0101         BA           0101         BA           0101         BA           0110         BC           0111         BE           1000         C0           1001         C2           1010         C4           1011         C6           1100         C8           1110         CA           1111         CE	Tuble of Betrice C	Juve Addi coo Byteo
0001         B2           0010         B4           0011         B6           0100         B8           0101         BA           0101         BC           0111         BE           1000         C0           1001         C2           1010         C4           1011         C6           1100         C8           1101         CA           1110         CC	AD[3:0] Settings	Address Bytes (HEX)
0010         B4           0011         B6           0100         B8           0101         BA           0110         BC           0111         BE           1000         C0           1001         C2           1010         C4           1011         C6           1100         C8           1101         CA           1110         CC	0000	B0
0011         B6           0100         B8           0101         BA           0110         BC           0111         BE           1000         C0           1001         C2           1010         C4           1011         C6           1100         C8           1101         CA           1110         CC	0001	B2
0100         B8           0101         BA           0110         BC           0111         BE           1000         C0           1001         C2           1010         C4           1011         C6           1100         C8           1101         CA           1110         CC	0010	B4
0101         BA           0110         BC           0111         BE           1000         C0           1001         C2           1010         C4           1011         C6           1100         C8           1101         CA           1110         CC	0011	B6
0110         BC           0111         BE           1000         C0           1001         C2           1010         C4           1011         C6           1100         C8           1101         CA           1110         CC	0100	B8
0111         BE           1000         C0           1001         C2           1010         C4           1011         C6           1100         C8           1101         CA           1110         CC	0101	BA
1000         C0           1001         C2           1010         C4           1011         C6           1100         C8           1101         CA           1110         CC	0110	BC
1001         C2           1010         C4           1011         C6           1100         C8           1101         CA           1110         CC	0111	BE
1010         C4           1011         C6           1100         C8           1101         CA           1110         CC	1000	CO
1011         C6           1100         C8           1101         CA           1110         CC	1001	C2
1100         C8           1101         CA           1110         CC	1010	C4
1101 CA 1110 CC	1011	C6
1110 CC	1100	C8
	1101	CA
1111 CE	1110	CC
	1111	CE

The SDA, SCL pins are 3.3V tolerant, but are not 5V tolerant. External pull-up resistor is required on the SDA. The resistor value can be from 1 k $\Omega$  to 5 k $\Omega$  depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

#### TRANSFER OF DATA VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

**START:** A High-to-Low transition on SDA while SCL is High indicates a message START condition.

**STOP:** A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

**IDLE:** If SCL and SDA are both High for a time exceeding  $t_{\rm BUF}$  from the last detected STOP condition or if they are High for a total exceeding the maximum specification for  $t_{\rm HIGH}$  then the bus will transfer to the IDLE state.

#### SMBus TRANSACTIONS

The device supports WRITE and READ transactions. See Register Description table for register address, type (Read/ Write, Read Only), default value and function information.

#### WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

- 1. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
- 2. The Device (Slave) drives the ACK bit ("0").
- 3. The Host drives the 8-bit Register Address.
- 4. The Device drives an ACK bit ("0").
- 5. The Host drive the 8-bit data byte.
- 6. The Device drives an ACK bit ("0").
- 7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

#### **READING A REGISTER**

To read a register, the following protocol is used (see SMBus 2.0 specification).

- 1. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
- 2. The Device (Slave) drives the ACK bit ("0").
- 3. The Host drives the 8-bit Register Address.
- 4. The Device drives an ACK bit ("0").
- 5. The Host drives a START condition.
- 6. The Host drives the 7-bit SMBus Address, and a "1" indicating a READ.
- 7. The Device drives an ACK bit "0".
- 8. The Device drives the 8-bit data value (register contents).
- 9. The Host drives a NACK bit "1" indicating end of the READ transfer.
- 10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur. Please see SMBus Register Map Table for more information.

### Table 9: SMBUS Slave Mode Register Map

Address	Register Name	Bit (s)	Field	Туре	Default	Description
0x00	Observation,	7	Reserved	R/W	0x00	Set bit to 0.
	Reset	6:3	Address Bit	R	1	Observation of AD[3:0] bits
			AD[3:0]			[6]: AD3
						[5]: AD2
						[4]: AD1
						[3]: AD0
		2	EEPROM Read	R		1: Device completed the read from external
			Done			EEPROM.
		1	Block Reset	R/W		1: Block bit 0 from resettting the registers; self
						clearing.
		0	Reset	R/W		SMBus Reset
						1: Reset registers to default value; self clearing.
0x01	PWDN Channels	7:0	PWDN CHx	R/W	0x00	Power Down per Channel
						[7]: CH7 – CHA_3
						[6]: CH6 – CHA_2
						[5]: CH5 – CHA_1
						[4]: CH4 – CHA_0
						[3]: CH3 – CHB_3
						[2]: CH2 – CHB_2
						[1]: CH1 – CHB_1
						[0]: CH0 – CHB_0
						00'h = all channels enabled
						FF'h = all channels disabled
						Note: override PRSNT pin.
0x02	Override PRSNT,	7:6	Reserved	R/W	0x00	Set bits to 0.
	LPBK Control	5:4	LPBK			00: Use LPBK pin control
			Control			01: INA_n to OUTB_n loopback
						10: INB_n to OUTA_n loopback
						11: Disable loopback and ignore LPBK pin.
		3:1	Reserved	4		Set bits to 0.
		0	Override PRSNT			1: Block PRSNT pin control
			pin			0: Allow PRSNT pin control
0x05	Slave Mode CRC bits	7:0	CRC bits	R/W	0x00	CRC bits [7:0]
0x06	Slave CRC Control	7:5	Reserved	R/W	0x10	Set bits to 0.
		4	Reserved			Set bit to 1.
		3	Slave CRC			1: Disables the slave CRC mode
						0: Enables the slave CRC mode
						Note: In order to change VOD, DEM and EQ of
						the channels in slave mode, set bit to 1 to disable
						the CRC.
		2:0	Reserved	]		Set bits to 0.

0x08	Override	7	Reserved	R/W	0x00	Set bit to 0.
	Pin Control	6	Override SD_TH	1		1: Block SD_TH pin control
						0: Allow SD_TH pin control
		5	Reserved	7		Set bit to 0.
		4	Override IDLE	7		1: IDLE control by registers
						0: IDLE control by signal detect
		3	Override RXDET	7		1: Block RXDET pin control
						0: Allow RXDET pin control
		2	Override RATE	7		1: Block RATE pin control
						0: Allow RATE pin control
		1	Reserved			Set bit to 0.
		0	Reserved	1		Set bit to 0.
0x0E	СН0 - СНВ0	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE, RXDET	5	IDLE_AUTO	1		1: Automatic IDLE detect
						0: Allow IDLE_SEL control in bit 4
						Note: override IDLE control.
		4	IDLE_SEL	1		1: Output is MUTED (electrical idle)
						0: Output is ON
						Note: override IDLE control.
		3:2	RXDET	7		00: Input is high-z impedance
						01: Auto RX-Detect,
						outputs test every 12 ms for 600 ms (50 times
						then stops; termination is high-z until detectio
						once detected input termination is 50 $\Omega$
						10: Auto RX-Detect,
						outputs test every 12 ms until detection occur
						termination is high-z until detection; once
						detected input termination is 50 $\Omega$
						11: Input is 50 Ω
				_		Note: override RXDET pin.
		1:0	Reserved			Set bits to 0.
0x0F	CH0 - CHB0	7:0	EQ Control	R/W	0x2F	IB0 EQ Control - total of 256 levels.
	EQ		_			See Table 2: Equalizer Settings.
0x10	CH0 - CHB0	7	Short Circuit	R/W	0xAD	1: Enable the short circuit protection
	VOD		Protection	_		0: Disable the short circuit protection
		6	RATE_SEL			1: Gen 1/2,
						0: Gen 3
				4		Note: override the RATE pin.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OB0 VOD Control
						000: 0.7 V
						001: 0.8 V
				1		010: 0.9 V
				1		011: 1.0 V
				1		100: 1.1 V
				1		101: 1.2 V (default)
						110: 1.3 V 111: 1.4 V
				1	1	1 1 1 . 1 .4 V

0x11	CH0 - CHB0 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH0 - CHB0. 1: RX = detected 0: RX = not detected
		6:5	RATE_DET STATUS	R	-	Observation bit for RATE_DET CH0 - CHB0. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G)
		4:3	Reserved	R/W	-	Set bits to 0.
					-	
		2:0	DEM Control	R/W		OB0 DEM Control 000: 0 dB
						001: -1.5 dB
						010: -3.5 dB (default)
						011: -5 dB
						100: –6 dB
						101: –8 dB
						110: –9 dB
						111: -12 dB
0x12	СНО - СНВО	7:4	Reserved	R/W	0x00	Set bits to 0.
UNIT	IDLE Threshold	3:2	IDLE thd			De-assert threshold
		0.2				00 = 110  mVp-p (default)
						01 = 100  mVp-p
						10 = 150  mVp-p
						11 = 130 mVp-p
						Note: override the SD_TH pin.
		1:0	IDLE tha	-		Assert threshold
		1.0				00 = 180  mVp-p (default)
						01 = 160  mVp-p
						10 = 210  mVp-p
						11 = 190 mVp-p
						Note: override the SD_TH pin.
0x15	CH1 - CHB1	7:6	Reserved	R/W	0x00	Set bits to 0.
0,110						
	IIDLE. RXDET	15				1. Automatic IDI E detect
	IDLE, RXDET	5	IDLE_AUTO			1: Automatic IDLE detect 0: Allow IDLE SEL control in bit 4
	IDLE, RXDET	5	IDLE_AUTO			0: Allow IDLE_SEL control in bit 4
						0: Allow IDLE_SEL control in bit 4 Note: override IDLE control.
	IDLE, RXDET	5	IDLE_AUTO	_		0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle)
	IDLE, RXDET			-		0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON
	IDLE, RXDET	4	IDLE_SEL	-		<ul> <li>0: Allow IDLE_SEL control in bit 4</li> <li>Note: override IDLE control.</li> <li>1: Output is MUTED (electrical idle)</li> <li>0: Output is ON</li> <li>Note: override IDLE control.</li> </ul>
	IDLE, RXDET			-		0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance
	IDLE, RXDE I	4	IDLE_SEL	_		0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect,
	IDLE, RXDE I	4	IDLE_SEL	-		0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times)
	IDLE, RXDE I	4	IDLE_SEL	-		0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection;
	IDLE, RXDE I	4	IDLE_SEL	-		<ul> <li>0: Allow IDLE_SEL control in bit 4 Note: override IDLE control.</li> <li>1: Output is MUTED (electrical idle)</li> <li>0: Output is ON Note: override IDLE control.</li> <li>00: Input is high-z impedance</li> <li>01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω</li> </ul>
	IDLE, RXDE I	4	IDLE_SEL	-		0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection;
	IDLE, RXDE I	4	IDLE_SEL	-		<ul> <li>0: Allow IDLE_SEL control in bit 4 Note: override IDLE control.</li> <li>1: Output is MUTED (electrical idle)</li> <li>0: Output is ON Note: override IDLE control.</li> <li>00: Input is high-z impedance</li> <li>01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω</li> <li>10: Auto RX-Detect,</li> </ul>
	IDLE, RXDE I	4	IDLE_SEL	-		0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 $\Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once
	IDLE, RXDE I	4	IDLE_SEL	-		0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 $\Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 $\Omega$
	IDLE, RXDE I	4	IDLE_SEL			0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 $\Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 $\Omega$ 11: Input is 50 $\Omega$
	IDLE, RXDE I	4	IDLE_SEL			0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 $\Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 $\Omega$ 11: Input is 50 $\Omega$ Note: override RXDET pin.
0x16	IDLE, RXDE I	4	IDLE_SEL	R/W	0x2F	0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 $\Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 $\Omega$ 11: Input is 50 $\Omega$

0x17	CH1 - CHB1	7	Short Circuit	R/W	0xAD	1: Enable the short circuit protection
	VOD		Protection			0: Disable the short circuit protection
		6	RATE_SEL			1: Gen 1/2,
						0: Gen 3
						Note: override the RATE pin.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OB1 VOD Control
						000: 0.7 V
						001: 0.8 V
						010: 0.9 V
						011: 1.0 V
						100: 1.1 V
						101: 1.2 V (default)
						110: 1.3 V
						111: 1.4 V
0x18	CH1 - CHB1	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH1 - CHB1.
	DEM					1: RX = detected
						0: RX = not detected
		6:5	RATE_DET	R		Observation bit for RATE_DET CH1 - CHB1.
			STATUS			00: GEN1 (2.5G)
						01: GEN2 (5G)
						11: GEN3 (8G)
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OB1 DEM Control
						000: 0 dB
						001: –1.5 dB
						010: –3.5 dB (default)
						011: –5 dB
						100: –6 dB
						101: –8 dB
						110: –9 dB
						111: –12 dB
0x19	CH1 - CHB1	7:4	Reserved	R/W	0x00	Set bits to 0.
	IDLE Threshold	3:2	IDLE thd			De-assert threshold
						00 = 110 mVp-p (default)
						01 = 100 mVp-p
						10 = 150 mVp-p
						11 = 130 mVp-p
						Note: override the SD_TH pin.
		1:0	IDLE tha	1		Assert threshold
						00 = 180 mVp-p (default)
						01 = 160 mVp-p
						10 = 210 mVp-p
						11 = 190 mVp-p
	1	1	1		1	Note: override the SD_TH pin.

0x1C	CH2 - CHB2	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE, RXDET	5	IDLE_AUTO	1		1: Automatic IDLE detect
						0: Allow IDLE_SEL control in bit 4
						Note: override IDLE control.
		4	IDLE_SEL			1: Output is MUTED (electrical idle) 0: Output is ON
						Note: override IDLE control.
		3:2	RXDET	-		00: Input is high-z impedance
		3.2				01: Auto RX-Detect,
						outputs test every 12 ms for 600 ms (50 times)
						then stops; termination is high-z until detection;
						once detected input termination is 50 $\Omega$ 10: Auto RX-Detect,
						outputs test every 12 ms until detection occurs;
						termination is high-z until detection; once
						detected input termination is 50 $\Omega$
						11: Input is 50 $\Omega$
						Note: override RXDET pin.
		1:0	Reserved	1		Set bits to 0.
0x1D	CH2 - CHB2	7:0	EQ Control	R/W	0x2F	IB2 EQ Control - total of 256 levels.
	EQ					See Table 2: Equalizer Settings.
0x1E	CH2 - CHB2	7	Short Circuit	R/W	0xAD	1: Enable the short circuit protection
	VOD		Protection			0: Disable the short circuit protection
		6	RATE_SEL	1		1: Gen 1/2,
			_			0: Gen 3
						Note: override the RATE pin.
		5:3	Reserved	1		Set bits to default value - 101.
		2:0	VOD Control	1		OB2 VOD Control
						000: 0.7 V
						001: 0.8 V
						010: 0.9 V
						011: 1.0 V
						100: 1.1 V
						101: 1.2 V (default)
						110: 1.3 V
						111: 1.4 V
0x1F	CH2 - CHB2	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH2 - CHB2.
	DEM					1: RX = detected
					1	0: RX = not detected
		6:5	RATE_DET	R		Observation bit for RATE_DET CH2 - CHB2.
			STATUS			00: GEN1 (2.5G)
						01: GEN2 (5G)
					4	11: GEN3 (8G)
		4:3	Reserved	R/W	4	Set bits to 0.
		2:0	DEM Control	R/W		OB2 DEM Control
						000: 0 dB
						001: -1.5 dB
						010: -3.5 dB (default)
						011: -5 dB
						100: -6 dB
						101:8 dB
						110: –9 dB
	1	1	1	1	1	111: –12 dB

0x20	CH2 - CHB2	7:4	Reserved	R/W	0x00	Set bits to 0.
	IDLE Threshold	3:2	IDLE thd			De-assert threshold
						00 = 110 mVp-p (default)
						01 = 100 mVp-p
						10 = 150 mVp-p
						11 = 130 mVp-p
						Note: override the SD_TH pin.
		1:0	IDLE tha			Assert threshold
						00 = 180 mVp-p (default)
						01 = 160 mVp-p
						10 = 210 mVp-p
						11 = 190 mVp-p
						Note: override the SD_TH pin.
0x23	СНЗ - СНВЗ	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE, RXDET	5	IDLE_AUTO	-		1: Automatic IDLE detect
		ľ				0: Allow IDLE_SEL control in bit 4
						Note: override IDLE control.
		4	IDLE_SEL	-		1: Output is MUTED (electrical idle)
		1				0: Output is ON
						Note: override IDLE control.
		0.0				
		3:2	RXDET			00: Input is high-z impedance
						01: Auto RX-Detect,
						outputs test every 12 ms for 600 ms (50 times
						then stops; termination is high-z until detection
						once detected input termination is 50 $\Omega$
						10: Auto RX-Detect,
						outputs test every 12 ms until detection occurs
						termination is high-z until detection; once
						detected input termination is 50 $\Omega$
						11: Input is 50 $\Omega$
			_			Note: override RXDET pin.
		1:0	Reserved			Set bits to 0.
0x24	CH3 - CHB3	7:0	EQ Control	R/W	0x2F	IB3 EQ Control - total of 256 levels.
	EQ					See Table 2: Equalizer Settings.
0x25	CH3 - CHB3	7	Short Circuit	R/W	0xAD	1: Enable the short circuit protection
	VOD		Protection			0: Disable the short circuit protection
		6	RATE_SEL			1: Gen 1/2,
						0: Gen 3
						Note: override the RATE pin.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OB0 VOD Control
						000: 0.7 V
						001: 0.8 V
						010: 0.9 V
						011: 1.0 V
						100: 1.1 V
						101: 1.2 V (default)
						110: 1.3 V
			1	1	1	111: 1.4 V

	CH3 - CHB3 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH3 - CHB3. 1: RX = detected
		6:5	RATE_DET STATUS	R	_	0: RX = not detected Observation bit for RATE_DET CH3 - CHB3. 00: GEN1 (2.5G)
						01: GEN2 (5G) 11: GEN3 (8G)
		4:3	Reserved	R/W	-	Set bits to 0.
		2:0	DEM Control	R/W	-	OB3 DEM Control
		2.0	DEM CONTON	1.0.00		000: 0 dB
						001: –1.5 dB
						010: –3.5 dB (default)
						011: –5 dB
						100: –6 dB
						101: –8 dB
						110: –9 dB
						111: –12 dB
0x27	CH3 - CHB3	7:4	Reserved	R/W	0x00	Set bits to 0.
	IDLE Threshold	3:2	IDLE thd			De-assert threshold
						00 = 110 mVp-p (default)
						01 = 100 mVp-p
						10 = 150 mVp-p
						11 = 130 mVp-p
				_		Note: override the SD_TH pin.
		1:0	IDLE tha	1		Assert threshold
						00 = 180 mVp-p (default)
						01 = 160 mVp-p
						10 = 210  mVp-p
						11 = 190  mVp-p
						Note: override the SD_TH pin.
0 0 D						
0x2B	CH4 - CHA0	7:6	Reserved	R/W	0x00	Set bits to 0.
0x2B	CH4 - CHA0 IDLE, RXDET	7:6 5	IDLE_AUTO	R/W		1: Automatic IDLE detect
0x2B				R/W	0000	1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4
0x2B		5	IDLE_AUTO	R/W	0000	1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control.
0x2B				R/W		1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle)
0x2B		5	IDLE_AUTO	R/W		1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON
0x2B		5	IDLE_AUTO	R/W	0.00	1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control.
0x2B		5	IDLE_AUTO	R/W		1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance
0x2B		5	IDLE_AUTO	- -		1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect,
0x2B		5	IDLE_AUTO	R/W		<ol> <li>Automatic IDLE detect</li> <li>Allow IDLE_SEL control in bit 4</li> <li>Note: override IDLE control.</li> <li>Output is MUTED (electrical idle)</li> <li>Output is ON</li> <li>Note: override IDLE control.</li> <li>Input is high-z impedance</li> <li>Auto RX-Detect,</li> <li>outputs test every 12 ms for 600 ms (50 times)</li> </ol>
0x2B		5	IDLE_AUTO			1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection;
0x2B		5	IDLE_AUTO			<ol> <li>Automatic IDLE detect</li> <li>Allow IDLE_SEL control in bit 4</li> <li>Note: override IDLE control.</li> <li>Output is MUTED (electrical idle)</li> <li>Output is ON</li> <li>Note: override IDLE control.</li> <li>Input is high-z impedance</li> <li>Auto RX-Detect,</li> <li>outputs test every 12 ms for 600 ms (50 times)</li> <li>then stops; termination is high-z until detection;</li> <li>once detected input termination is 50 Ω</li> </ol>
0x2B		5	IDLE_AUTO			<ol> <li>Automatic IDLE detect</li> <li>Allow IDLE_SEL control in bit 4</li> <li>Note: override IDLE control.</li> <li>Output is MUTED (electrical idle)</li> <li>Output is ON</li> <li>Note: override IDLE control.</li> <li>O0: Input is high-z impedance</li> <li>O1: Auto RX-Detect,</li> <li>outputs test every 12 ms for 600 ms (50 times)</li> <li>then stops; termination is high-z until detection;</li> <li>once detected input termination is 50 Ω</li> <li>10: Auto RX-Detect,</li> </ol>
0x2B		5	IDLE_AUTO			<ol> <li>Automatic IDLE detect</li> <li>Allow IDLE_SEL control in bit 4</li> <li>Note: override IDLE control.</li> <li>Output is MUTED (electrical idle)</li> <li>Output is ON</li> <li>Note: override IDLE control.</li> <li>O0: Input is high-z impedance</li> <li>O1: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times)</li> <li>then stops; termination is high-z until detection; once detected input termination is 50 Ω</li> <li>Auto RX-Detect, outputs test every 12 ms until detection occurs;</li> </ol>
0x2B		5	IDLE_AUTO	_ R/W		1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 $\Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once
0x2B		5	IDLE_AUTO	_ R/W		1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 $\Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 $\Omega$
0x2B		5	IDLE_AUTO	_ R/W		1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 $\Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 $\Omega$ 11: Input is 50 $\Omega$
0x2B		5 4 3:2	IDLE_AUTO IDLE_SEL RXDET	_ R/W		1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 $\Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 $\Omega$ 11: Input is 50 $\Omega$ Note: override RXDET pin.
0x2B 0x2C		5	IDLE_AUTO	R/W	0x00	1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. 1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control. 00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 $\Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 $\Omega$ 11: Input is 50 $\Omega$

0x2D	CH4 - CHA0	7	Short Circuit	R/W	0xAD	1: Enable the short circuit protection
	VOD		Protection			0: Disable the short circuit protection
		6	RATE_SEL			1: Gen 1/2,
						0: Gen 3
						Note: override the RATE pin.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OA0 VOD Control
						000: 0.7 V
						001: 0.8 V
						010: 0.9 V
						011: 1.0 V
						100: 1.1 V
						101: 1.2 V (default)
						110: 1.3 V
						111: 1.4 V
0x2E	CH4 - CHA0	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH4 - CHA0.
	DEM					1: RX = detected
						0: RX = not detected
		6:5	RATE_DET	R		Observation bit for RATE_DET CH4 - CHA0.
			STATUS			00: GEN1 (2.5G)
						01: GEN2 (5G)
						11: GEN3 (8G)
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OA0 DEM Control
						000: 0 dB
						001: –1.5 dB
						010: –3.5 dB (default)
						011: –5 dB
						100: –6 dB
						101: –8 dB
						110: –9 dB
						111: –12 dB
0x2F	CH4 - CHA0	7:4	Reserved	R/W	0x00	Set bits to 0.
	IDLE Threshold	3:2	IDLE thd			De-assert threshold
						00 = 110 mVp-p (default)
						01 = 100 mVp-p
						10 = 150 mVp-p
						11 = 130 mVp-p
						Note: override the SD_TH pin.
		1:0	IDLE tha			Assert threshold
						00 = 180 mVp-p (default)
						01 = 160 mVp-p
						10 = 210 mVp-p
						11 = 190 mVp-p
				1		Note: override the SD_TH pin.

0x32	CH5 - CHA1	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE, RXDET	5	IDLE_AUTO	1		1: Automatic IDLE detect
						0: Allow IDLE_SEL control in bit 4
						Note: override IDLE control.
		4	IDLE_SEL			1: Output is MUTED (electrical idle) 0: Output is ON
						Note: override IDLE control.
		3:2	RXDET	-		00: Input is high-z impedance
		3.2				01: Auto RX-Detect,
						outputs test every 12 ms for 600 ms (50 times)
						then stops; termination is high-z until detection;
						once detected input termination is 50 $\Omega$ 10: Auto RX-Detect,
						outputs test every 12 ms until detection occurs;
						termination is high-z until detection; once
						detected input termination is 50 $\Omega$
						11: Input is 50 $\Omega$
						Note: override RXDET pin.
		1:0	Reserved	1		Set bits to 0.
0x33	CH5 - CHA1	7:0	EQ Control	R/W	0x2F	IA1 EQ Control - total of 256 levels.
0,00	EQ	7.0				See Table 2: Equalizer Settings.
0x34	CH5 - CHA1	7	Short Circuit	R/W	0xAD	1: Enable the short circuit protection
0704	VOD	ľ	Protection			0: Disable the short circuit protection
	100	6	RATE_SEL	-		1: Gen 1/2,
		ľ				0: Gen 3
						Note: override the RATE pin.
		5:3	Reserved	1		Set bits to default value - 101.
		2:0	VOD Control	-		OA1 VOD Control
		2.0	VOD Control			000: 0.7 V
						001: 0.8 V
						010: 0.9 V
						011: 1.0 V
						100: 1.1 V
						101: 1.2 V (default)
						110: 1.3 V
						111: 1.4 V
0x35	CH5 - CHA1	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH5 - CHA1.
	DEM					1: RX = detected
						0: RX = not detected
		6:5	RATE_DET	R	1	Observation bit for RATE_DET CH5 - CHA1.
			STATUS			00: GEN1 (2.5G)
						01: GEN2 (5G)
						11: GEN3 (8G)
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OA1 DEM Control
						000: 0 dB
						001: –1.5 dB
						010: –3.5 dB (default)
						011: –5 dB
						100: –6 dB
						101: –8 dB
						110: –9 dB
	1		1	1	1	111: –12 dB

0x36	CH5 - CHA1	7:4	Reserved	R/W	0x00	Set bits to 0.
	IDLE Threshold	3:2	IDLE thd			De-assert threshold
						00 = 110  mVp-p (default)
						01 = 100 mVp-p
						10 = 150 mVp-p
						11 = 130 mVp-p
						Note: override the SD_TH pin.
		1:0	IDLE tha			Assert threshold
						00 = 180  mVp-p (default)
						01 = 160 mVp-p
						10 = 210 mVp-p
						11 = 190 mVp-p
						Note: override the SD_TH pin.
0x39	CH6 - CHA2	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE, RXDET	5	IDLE_AUTO			1: Automatic IDLE detect
						0: Allow IDLE_SEL control in bit 4
						Note: override IDLE control.
		4	IDLE_SEL			1: Output is MUTED (electrical idle)
						0: Output is ON
						Note: override IDLE control.
		3:2	RXDET			00: Input is high-z impedance
						01: Auto RX-Detect,
						outputs test every 12 ms for 600 ms (50 times
						then stops; termination is high-z until detection
						once detected input termination is 50 $\Omega$
						10: Auto RX-Detect,
						outputs test every 12 ms until detection occurs
						termination is high-z until detection; once
						detected input termination is 50 $\Omega$
						11: Input is 50 Ω
						Note: override RXDET pin.
		1:0	Reserved			Set bits to 0.
0x3A	CH6 - CHA2	7:0	EQ Control	R/W	0x2F	IA2 EQ Control - total of 256 levels.
	EQ					See Table 2: Equalizer Settings.
0x3B	CH6 - CHA2	7	Short Circuit	R/W	0xAD	1: Enable the short circuit protection
	VOD		Protection			0: Disable the short circuit protection
		6	RATE_SEL			1: Gen 1/2,
						0: Gen 3
						Note: override the RATE pin.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OA2 VOD Control
		2.0				000: 0.7 V
						001: 0.8 V
						010: 0.9 V
						011: 1.0 V
						100: 1.1 V
			1			
						1101: 1.2 V (detault)
						101: 1.2 V (default) 110: 1.3 V

0x3C	CH6 - CHA2 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH6 - CHA2. 1: RX = detected 0: RX = not detected
		6:5	RATE_DET STATUS	R		Observation bit for RATE_DET CH6 - CHA2. 00: GEN1 (2.5G) 01: GEN2 (5G)
				<b>D</b> 444	4	11: GEN3 (8G)
		4:3	Reserved	R/W	4	Set bits to 0.
		2:0	DEM Control	R/W		OA2 DEM Control 000: 0 dB
						001: –1.5 dB
						010: -3.5 dB (default)
						011: –5 dB
						100: –6 dB
						101: –8 dB
						110: –9 dB
						111: –12 dB
0x3D	CH6 - CHA2	7:4	Reserved	R/W	0x00	Set bits to 0.
	IDLE Threshold	3:2	IDLE thd			De-assert threshold
						00 = 110 mVp-p (default)
						01 = 100 mVp-p
						10 = 150 mVp-p
						11 = 130 mVp-p
						Note: override the SD_TH pin.
		1:0	IDLE tha			Assert threshold
						00 = 180 mVp-p (default)
						01 = 160 mVp-p
						10 = 210 mVp-p
						11 = 190 mVp-p
						Note: override the SD_TH pin.
0x40	CH7 - CHA3	7:6	Reserved	R/W	0x00	Set bits to 0.
	IDLE, RXDET	5	IDLE_AUTO			1: Automatic IDLE detect
						0: Allow IDLE_SEL control in bit 4
						Note: override IDLE control.
		4	IDLE_SEL			1: Output is MUTED (electrical idle)
						0: Output is ON
						Note: override IDLE control.
		3:2	RXDET	7		00: Input is high-z impedance
						01: Auto RX-Detect,
						outputs test every 12 ms for 600 ms (50 times)
						then stops; termination is high-z until detection;
						once detected input termination is 50 $\Omega$
						10: Auto RX-Detect,
						outputs test every 12 ms until detection occurs;
						termination is high-z until detection; once
						detected input termination is 50 $\Omega$
						11: Input is 50 $\Omega$
						Note: override RXDET pin.
		1:0	Reserved			Set bits to 0.
0x41	CH7 - CHA3	7:0	EQ Control	R/W	0x2F	IA3 EQ Control - total of 256 levels.
	EQ			1	1	See Table 2: Equalizer Settings.

0x42	CH7 - CHA3 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	RATE_SEL	1		1: Gen 1/2,
		ľ				0: Gen 3
						Note: override the RATE pin.
		5:3	Reserved	1		Set bits to default value - 101.
		2:0	VOD Control	1		OA3 VOD Control
		2.0				000: 0.7 V
						001: 0.8 V
						010: 0.9 V
						011: 1.0 V
						100: 1.1 V
						101: 1.2 V (default)
						110: 1.3 V
						111: 1.4 V
0x43	CH7 - CHA3	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH7 - CHA3.
0,110	DEM				0.00	1: $RX = detected$
						0: RX = not detected
		6:5	RATE_DET	R	-	Observation bit for RATE_DET CH7 - CHA3.
			STATUS			00: GEN1 (2.5G)
						01: GEN2 (5G)
					_	11: GEN3 (8G)
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OA3 DEM Control
		2.0				000: 0 dB
						001: –1.5 dB
						010: -3.5 dB (default)
						011: –5 dB
						100: –6 dB
						101: –8 dB
						110: –9 dB
						111: –12 dB
0x44	CH7 - CHA3	7:4	Reserved	R/W	0x00	Set bits to 0.
	IDLE Threshold	3:2	IDLE thd	1		De-assert threshold
						00 = 110 mVp-p (default)
						01 = 100 mVp-p
						10 = 150 mVp-p
						11 = 130 mVp-p
						Note: override the SD_TH pin.
		1:0	IDLE tha	1		Assert threshold
						00 = 180 mVp-p (default)
						01 = 160 mVp-p
						10 = 210 mVp-p
						11 = 190 mVp-p
						Note: override the SD_TH pin.
0x51	Device ID	7:5	VERSION	R	0x44	010'b
		4:0	ID	1	1	00100'b

#### **Applications Information**

The DS80PCI402 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the information below and Revision 4 of the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

### PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and LPDS outputs have been optimized to work with interconnects using a controlled differential

impedance of 85 -  $100\Omega$ . It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187 for additional information on LLP packages.

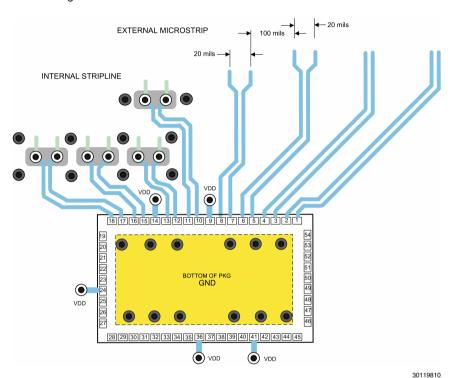


FIGURE 6. Typical Routing Options

The graphic shown above depicts different transmission line topologies which can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each hole and providing for a low inductance return current path. When the via structure is associated with thick backplane PCB, further optimization such as back drilling is often used to reduce the deterimential high frequency effects of stubs on the signal path.

#### POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS80PCI402 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be

connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V<sub>DD</sub> and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 µF bypass capacitor should be connected to each V<sub>DD</sub> pin such that the capacitor is placed as close as possible to the DS80PCI402. Smaller body size capacitors can help facilitate proper component placement. Additionally, capacitor with capacitance in the range of 1 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

#### **Typical Performance Curves Characteristics**

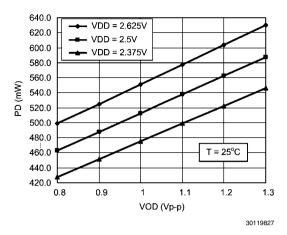


FIGURE 7. Power Dissipation (PD) vs. Output Differential Voltage (VOD)

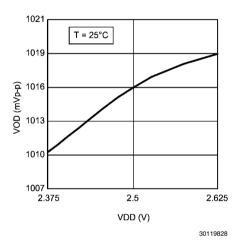


FIGURE 8. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Supply Voltage (VDD)

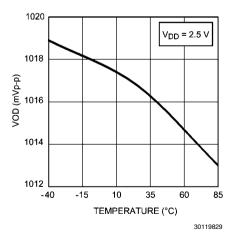
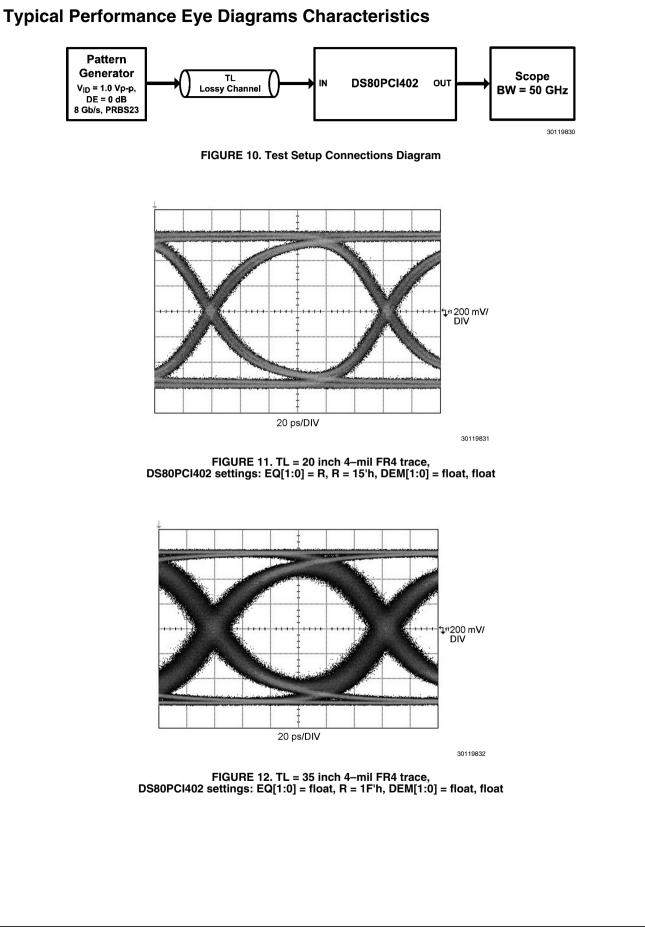
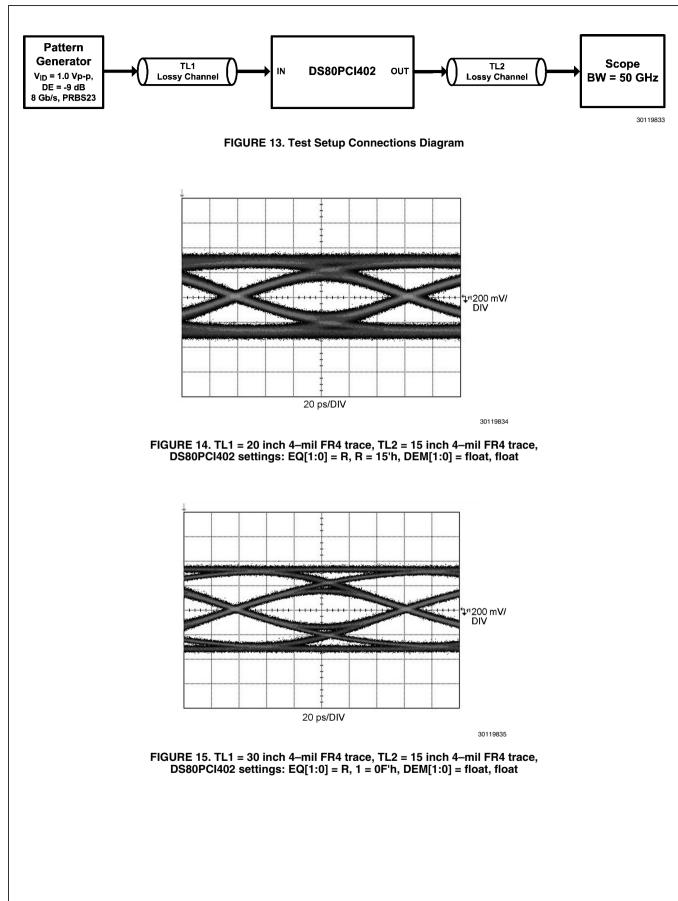
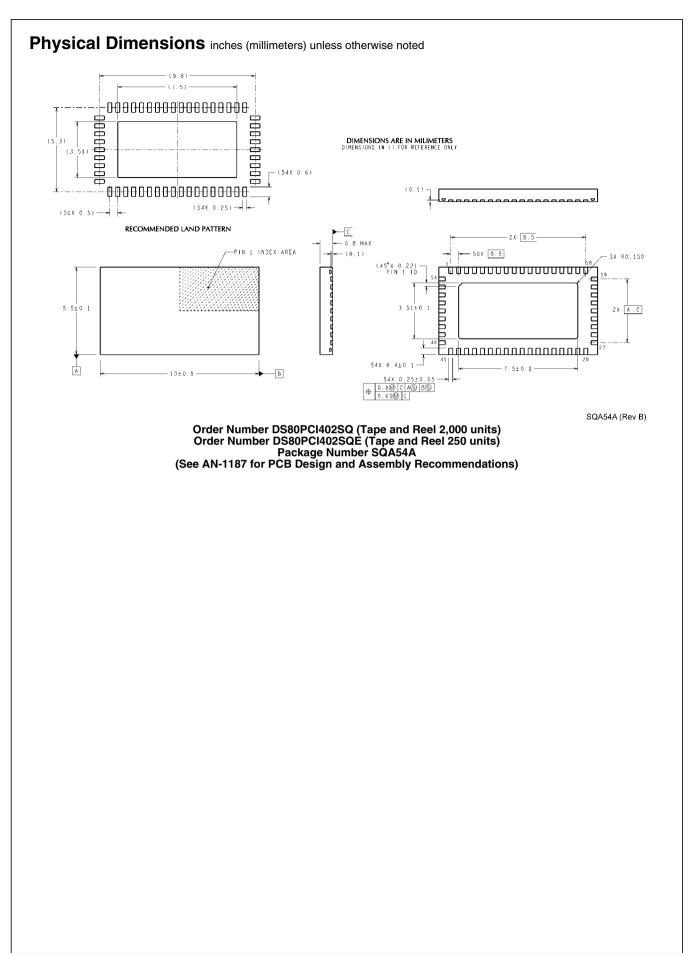


FIGURE 9. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Temperature









### Notes

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