### 2.5 Gbps / 5.0 Gbps / 8.0 Gbps 4 Lane PCI Express Repeater with Equalization and De-Emphasis

## General Description

The DS80PCI402 is a low power, 4 lane repeater with 4-stage input equalization, and output de-emphasis driver to enhance the reach of PCl express serial links in board-to-board or cable interconnects. Ideal for x 4 (or lower) PCI express configuration, the DS80PCI402 automatically detects and adapts to Gen-1, Gen-2 and Gen-3 data rates for easy system upgrade. Each channel supports seamless detection and management of the new Gen-3 transmit equalizer coefficients (FIR tap) handshake protocol and PCle control signals such as transmit idle, beacon etc. without external system intervention. An automatic receive detection circuitry controls the input termination impedance based upon endpoint insertion (hot-plug events). These features guarantee PCle interoperability at both the electrical and system level, while reducing design complexity.
Powered by National's SiGe BiCMOS process, DS80PCI402 offers programmable transmit de-emphasis (up to 12 dB ), transmit VoD (up to $1300 \mathrm{mVp}-\mathrm{p}$ ) and receive equalization (up to 36 dB ) to enable longer distance transmission in lossy copper cables $(10 \mathrm{~m}+$ ), or backplanes ( 40 " + ) with multiple connectors. The receiver is capable of opening an input eye that is completely closed due to inter-symbol interference (ISI) introduced by the interconnect medium.
The programmable settings can be applied easily via pins, software (SMBus/I2C) or loaded via an external EEPROM. When operating in the EEPROM mode, the configuration information is automatically loaded on power up, which eliminates the need for an external microprocessor or software driver.

With a low power consumption and control to turn-off unused channels, the DS80PCI402 is part of PowerWise family of energy efficient devices.

## Features

- Comprehensive family, proven system inter-operability DS80PCl102: x1 PCle Gen-1/2/3
DS80PCI402 : x4 PCle Gen-1/2/3
DS80PCI800 : x8/x16 PCle Gen-1/2/3
- Automatic rate detect and adaptation to Gen-1/2/3 speeds
- Seamless support for Gen-3 transmit FIR handshake
- Rate adaptive receive EQ (up to 36 dB ), transmit deemphasis (up to 12 dB ) only Gen-1/2
- Adjustable Transmit VOD: 0.8 to $1.3 \mathrm{Vp}-\mathrm{p}$ (pin mode)
- 0.2 UI of residual deterministic jitter at 8 Gbps after 40 " of FR4 or 10m 30awg PCle Cable
- Low power dissipation with ability to turnoff unused channels: $65 \mathrm{~mW} /$ channel
- Automatic receiver detect (hot-plug)
- Multiple configuration modes: Pins/SMbus/DirectEEPROM load
- Flow-thru pinout: 54 -pin LLP ( $10 \mathrm{~mm} \times 5.5 \mathrm{~mm}, 0.5 \mathrm{~mm}$ pitch)
- Single supply voltage: 2.5 V or 3.3 V (selectable)
- 5 kV HBM ESD rating
- -40 to $85^{\circ} \mathrm{C}$ operating temperature range

Typical Application


Block Diagram - Detail View Of Channel (1 Of 8)


## Pin Diagram



DS80PCI402 Pin Diagram 54 lead

## Ordering Information

| NSID | Qty | Spec | Package |
| :--- | :--- | :--- | :--- |
| DS80PCI402SQ | Tape \& Reel Supplied As 2,000 Units | NOPB | SQA54A |
| DS80PCI402SQE | Tape \& Reel Supplied As 250 Units | NOPB | SQA54A |

## Pin Descriptions

| Pin Name | Pin Number | I/O, Type | Pin Description |
| :---: | :---: | :---: | :---: |
| Differential High Speed I/O's |  |  |  |
| $\begin{aligned} & \text { INB_0+, INB_0- }, \\ & \text { INB_1+, INB_1-, } \\ & \text { INB_2+, INB_2-, } \\ & \text { INB_3+, INB_3- } \end{aligned}$ | $\begin{aligned} & 45,44,43,42 \\ & 40,39,38,37 \end{aligned}$ | 1 | Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip $50 \Omega$ termination resistor connects INB_n+ to VDD and INB_n- to VDD when enabled. |
| OUTB_0+, OUTB_0-, OUTB_1+, OUTB_1-, OUTB_2+, OUTB_2-, OUTB_3+, OUTB_3- | $\begin{aligned} & 1,2,3,4 \\ & 5,6,7,8 \end{aligned}$ | 0 | Inverting and non-inverting $50 \Omega$ driver outputs with deemphasis. Compatible with AC coupled CML inputs. |
| $\begin{array}{\|l\|} \hline \text { INA_0+, INA_0- }, \\ \text { INA_1+, INA_1-, } \\ \text { INA_2+, INA_2-, } \\ \text { INA_3+, INA_3- } \end{array}$ | $\begin{aligned} & 10,11,12,13 \\ & 15,16,17,18 \end{aligned}$ | 1 | Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip $50 \Omega$ termination resistor connects INA_n+ to VDD and INA_n- to VDD when enabled. |
| OUTA_0+, OUTA_0-, <br> OUTA_1+, OUTA_1-, <br> OUTA_2+, OUTA_2-, <br> OUTA_3+, OUTA_3- | $\begin{aligned} & 35,34,33,32 \\ & 31,30,29,28 \end{aligned}$ | 0 | Inverting and non-inverting $50 \Omega$ driver outputs with deemphasis. Compatible with AC coupled CML inputs. |
| Control Pins - Shared (LVCMOS) |  |  |  |
| ENSMB | 48 | I, LVCMOS | System Management Bus (SMBus) enable pin Tie $1 \mathrm{k} \Omega$ to VDD = Register Access SMBus Slave mode FLOAT = Read External EEPROM (Master SMBUS Mode) Tie $1 \mathrm{k} \Omega$ to $\mathrm{GND}=$ Pin Mode |
| ENSMB = 1 (SMBUS MODE) |  |  |  |
| SCL | 50 | I, LVCMOS, O, OPEN Drain | ENSMB Master or Slave mode SMBUS clock input pin is enabled (slave mode). Clock output when loading EEPROM configuration (master mode). |
| SDA | 49 | I, LVCMOS, O, OPEN Drain | ENSMB Master or Slave mode The SMBus bi-directional SDA pin is enabled. Data input or open drain (pull-down only) output. |
| AD0-AD3 | 54, 53, 47, 46 | I, LVCMOS | ENSMB Master or Slave mode SMBus Slave Address Inputs. In SMBus mode, these pins are the user set SMBus slave address inputs. |
| READ_EN | 26 | I, LVCMOS | When using an External EEPROM, a transition from high to low starts the load from the external EEPROM |
| ENSMB = 0 (PIN MODE) |  |  |  |
| EQAO, EQA1 <br> EQB0, EQB1 | $\begin{aligned} & 20,19 \\ & 46,47 \end{aligned}$ | I, 4-LEVEL, LVCMOS | EQA[1:0] and EQB[1:0] control the level of equalization of the $A / B$ sides as shown in. The pins are active only when ENSMB is de-asserted (low). Each of the $4 \mathrm{~A} / \mathrm{B}$ channels have the same level unless controlled by the SMBus control registers When ENSMB goes high the SMBus registers provide independent control of each lane. The EQB[1:0] pins are converted to SMBUS AD2, AD3 inputs. See Table 2: Equalizer Settings. |


| Pin Name | Pin Number | I/O, Type | Pin Description |
| :---: | :---: | :---: | :---: |
| DEMA0, DEMA1 DEMB0, DEMB1 | $\begin{aligned} & 49,50 \\ & 53,54 \end{aligned}$ | $\begin{aligned} & \hline \text { I, 4-LEVEL, } \\ & \text { LVCMOS } \end{aligned}$ | DEMA[1:0] and DEMB[1:0] control the level of de-emphasis of the $A / B$ sides as shown in. The pins are only active when ENSMB is de-asserted (low). Each of the $4 \mathrm{~A} / \mathrm{B}$ channels have the same level unless controlled by the SMBus control registers. When ENSMB goes high the SMBus registers provide independent control of each lane. The DEMA[1:0] pins are converted to SMBUS SCL/SDA and DEMB[1:0] pins are converted to AD0, AD1 inputs. See Table 3: Output Voltage and De-emphasis Settings. |
| RATE | 21 | $\begin{array}{\|l} \hline \text { I, 4-LEVEL, } \\ \text { LVCMOS } \end{array}$ | RATE control pin selects GEN 1,2 and GEN 3 operating modes. <br> Tie $1 \mathrm{k} \Omega$ to GND $=$ GEN 1,2 <br> Float = Auto Rate select <br> Tie $20 \mathrm{k} \Omega$ to GND $=$ GEN 3 without De-emphasis <br> Tie $1 \mathrm{k} \Omega$ to VDD = GEN 3 with De-emphasis |
| SD_TH | 26 | I, 4-LEVEL, LVCMOS | Controls the internal Signal Detect Threshold. See Table 5: Signal Detect Threshold Level. |
| Control Pins - Both Pin and SMBus Modes (LVCMOS) |  |  |  |
| RXDET | 22 | $\begin{aligned} & \text { I, 4-LEVEL, } \\ & \text { LVCMOS } \end{aligned}$ | The RXDET pin controls the receiver detect function. Depending on the input level, a $50 \Omega$ or $>50 \mathrm{~K} \Omega$ termination to the power rail is enabled. <br> See Table 4: RX-Detect Settings. |
| LPBK | 23 | $\begin{aligned} & \text { I, 4-LEVEL, } \\ & \text { LVCMOS } \end{aligned}$ | Controls the loopback function <br> Tie $1 \mathrm{k} \Omega$ to GND $=$ Root Complex Loopback (INA_n to OUTB_n <br> Float $=$ Normal Operation <br> Tie $1 \mathrm{k} \Omega$ to VDD = End-point Loopback (INB_n to OUTA_n) |
| VDD_SEL | 25 | I, FLOAT | Controls the internal regulator <br> Float $=2.5 \mathrm{~V}$ mode <br> Tie GND = 3.3V mode |
| $\overline{\text { PRSNT }}$ | 52 | I, LVCMOS | Cable Present Detect input. high when a cable is not present per PCle Cabling Spec. 1.0. Puts part into low power mode. When low (normal operation) part is enabled. See Table 4: $R X$-Detect Settings. |
| Outputs |  |  |  |
| ALL_DONE | 27 | O, LVCMOS | Valid Register Load Status Output HIGH = External EEPROM load failed <br> LOW = External EEPROM load passed |
| Power |  |  |  |
| VIN | 24 | Power | In 3.3V mode, feed 3.3V to VIN In 2.5 V mode, leave floating. |
| VDD | $\begin{aligned} & 9,14,36,41, \\ & 51 \end{aligned}$ | Power | Power supply pins CML/analog <br> 2.5 V mode, connect to 2.5 V <br> 3.3V mode, connect 0.1 uF cap to each VDD pin |
| GND | DAP | Power | Ground pad (DAP - die attach pad). |
| Notes: <br> LVCMOS inputs without the "Float" conditions must be driven to a logic low or high at all times or operation is not guaranteed. <br> Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10-90\%. <br> For 3.3 V mode operation, VIN pin $=3.3 \mathrm{~V}$ and the "VDD" for the 4 -level input is 3.3 V . <br> For 2.5 V mode operation, VDD pin $=2.5 \mathrm{~V}$ and the "VDD" for the 4 -level input is 2.5 V . |  |  |  |

$\begin{array}{lr}\text { Absolute Maximum Ratings (Note 1) } \\ \text { If Military/Aerospace specified devices are required, } \\ \text { please contact the Texas Instruments Sales Office/ } \\ \text { Distributors for availability and specifications. } \\ \text { Supply Voltage (VDD }-2.5 \mathrm{~V} \text { ) } & -0.5 \mathrm{~V} \text { to }+2.75 \mathrm{~V} \\ \text { Supply Voltage (VIN }-3.3 \mathrm{~V} \text { ) } & -0.5 \mathrm{~V} \text { to }+4.0 \mathrm{~V} \\ \text { LVCMOS Input/Output Voltage } & -0.5 \mathrm{~V} \text { to }+4.0 \mathrm{~V} \\ \text { CML Input Voltage } & -0.5 \mathrm{~V} \text { to (VDD }+0.5 \text { ) } \\ \text { CML Input Current } & -30 \text { to }+30 \mathrm{~mA} \\ \text { Junction Temperature } & 125^{\circ} \mathrm{C} \\ \text { Storage Temperature } & -40^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ \text { Lead Temperature Range Soldering } & +260^{\circ} \mathrm{C} \\ \text { (4 sec.) } & \\ \text { SQA54A Package } & \\ \text { Derate SQA54A Package } & 52.6 \mathrm{~mW} /{ }^{\circ} \mathrm{C} \text { above } \\ & +25^{\circ} \mathrm{C}\end{array}$

| Supply Voltage (VDD -2.5 V ) | -0.5 V to +2.75 V |
| :--- | ---: |
| Supply Voltage (VIN -3.3 V ) | -0.5 V to +4.0 V |
| LVCMOS Input/Output Voltage | -0.5 V to +4.0 V |
| CML Input Voltage | -0.5 V to (VDD +0.5 ) |
| CML Input Current | -30 to +30 mA |
| Junction Temperature | $125^{\circ} \mathrm{C}$ |
| Storage Temperature | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Lead Temperature Range Soldering | $+260^{\circ} \mathrm{C}$ |
| (4 sec.) |  |
| SQA54A Package |  |
| Derate SQA54A Package | $52.6 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above |
|  | $+25^{\circ} \mathrm{C}$ |

ESD Rating
HBM, STD - JESD22-A114F 5 kV
MM, STD - JESD22-A115-A 150 V
CDM, STD - JESD22-C101-D 1000 V
Thermal Resistance
$\theta \mathrm{JC}$
$11.5^{\circ} \mathrm{C} / \mathrm{W}$
ӨJA, No Airflow, 4 layer JEDEC $19.1^{\circ} \mathrm{C} / \mathrm{W}$
For soldering specifications: see product folder at www.national.com/ms/MS/MS-SOLDERING.pdf

|  | Min | Typ | Max | Units |
| :--- | :--- | :--- | :--- | :--- |
|  |  |  |  |  |
| Supply Voltage (2.5V mode) | 2.375 | 2.5 | 2.625 | V |
| Supply Voltgae (3.3V mode) | 3.0 | 3.3 | 3.6 | V |
| Ambient Temperature | -40 | 25 | +85 | ${ }^{\circ} \mathrm{C}$ |
| SMBus (SDA, SCL) |  |  | 3.6 | V |
| Supply Noise up to 50 MHz |  |  | 100 | $\mathrm{mVp}-\mathrm{p}$ |
| (Note 4) |  |  |  |  |


| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Power |  |  |  |  |  |  |
| PD | Power Dissipation | VDD = 2.5 V supply, <br> EQ Enabled, <br> VOD = $1.0 \mathrm{Vp}-\mathrm{p}$, <br> RXDET $=1$, PRSNT $=0$ |  | 500 | 700 | mW |
|  |  | VIN = 3.3 V supply, <br> EQ Enabled, $\mathrm{VOD}=1.0 \mathrm{Vp}-\mathrm{p}$, RXDET $=1, \mathrm{PRSNT}=0$ |  | 660 | 900 | mW |

## LVCMOS / LVTTL DC Specifications

| $\mathrm{V}_{\text {ih }}$ | High Level Input Voltage |  | 2.0 | 3.6 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{il}}$ | Low Level Input Voltage |  | 0 | 0.8 | V |
| $\mathrm{V}_{\text {oh }}$ | High Level Output Voltage <br> (ALL_DONE pin) | $\mathrm{I}_{\text {oh }}=-4 \mathrm{~mA}$ | 2.0 |  | V |
| $\mathrm{V}_{\text {ol }}$ | Low Level Output Voltage <br> (ALL_DONE pin) | $\mathrm{l}_{01}=4 \mathrm{~mA}$ |  | 0.4 | V |
| $\mathrm{t}_{\text {ih }}$ | Input High Current (PRSNT pin) | $\begin{aligned} & \mathrm{VIN}=3.6 \mathrm{~V}, \\ & \text { LVCMOS }=3.6 \mathrm{~V} \end{aligned}$ | -15 | +15 | uA |
|  | Input High Current with internal resistors (4-level input pin) |  | +20 | +150 | uA |
| $\mathrm{I}_{\mathrm{il}}$ | Input Low Current (PRSNT pin) | $\begin{aligned} & \mathrm{VIN}=3.6 \mathrm{~V}, \\ & \text { LVCMOS = } 0 \mathrm{~V} \end{aligned}$ | -15 | +15 | uA |
|  | Input Low Current with internal resistors (4-level input pin) |  | -160 | -40 | uA |


| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CML Receiver Inputs (IN_n+, IN_n-) |  |  |  |  |  |  |
| $\mathrm{RL}_{\text {rx-diff }}$ | RX Differential return loss | 0.05-1.25 GHz |  | -16 |  | dB |
|  |  | $1.2-2.5 \mathrm{GHz}$ |  | -16 |  | dB |
|  |  | $2.5-4.0 \mathrm{GHz}$ |  | -14 |  | dB |
| RLrx-cm | RX Common mode return loss | 0.05-2.5 GHz |  | -12 |  | dB |
|  |  | $2.5-4.0 \mathrm{GHz}$ |  | -8 |  | dB |
| Zrx-dc | RX DC common mode impedance | Tested at VDD $=2.5 \mathrm{~V}$ | 40 | 50 | 60 | $\Omega$ |
| Zrx-diff-dc | RX DC differntial mode impedance | Tested at VDD $=2.5 \mathrm{~V}$ | 80 | 100 | 120 | $\Omega$ |
| Vrx-diff-dc | Differential RX peak to peak voltage (VID) | Tested at pins | 0.6 | 1.0 | 1.2 | V |
| Zrx-high-imp-dc-pos | DC Input common mode impedance for $\mathrm{V}>0$ | $\begin{aligned} & \mathrm{VID}=0 \text { to } 200 \mathrm{mV}, \\ & \mathrm{ENSMB}=0, \text { RXDET }=0, \\ & \text { VDD }=2.5 \mathrm{~V} \\ & \hline \end{aligned}$ |  | 50 |  | $\mathrm{K} \Omega$ |
| Vrx-signal-det-diff-pp | Signal detect assert level for active data signal | SD_TH = F (float), 0101 pattern at 8 Gbps |  | 180 |  | mVp-p |
| Vrx-idle-det-diff-pp | Signal detect de-assert level for electrical idle | SD_TH = F (float), 0101 pattern at 8 Gbps |  | 110 |  | mVp-p |


| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| High Speed Outputs |  |  |  |  |  |  |
| $\mathrm{V}_{\text {tx-dift-pp }}$ | Output Voltage Differential Swing | Differential measurement with Out_n+ and OUT_n-, terminated by $50 \Omega$ to GND, AC-Coupled, VID $=1.0 \mathrm{Vp}-\mathrm{p}$, DEM0 $=1$, DEM1 $=0$ <br> (Note 7) | 0.8 | 1.0 | 1.2 | mVp-p |
| $\mathrm{V}_{\text {tx-de-ratio_3.5 }}$ | TX de-emphasis ratio | $\begin{aligned} & \text { VOD = } 1.0 \text { Vp-p, } \\ & \text { DEM0 = 0, DEM1 = R, } \\ & \text { Gen } 1 \& 2 \text { modes only } \end{aligned}$ |  | -3.5 |  | dB |
| $\mathrm{V}_{\text {tx-de-ratio_6 }}$ | TX de-emphasis ratio | $\begin{aligned} & \text { VOD = } 1.0 \text { Vp-p, } \\ & \text { DEM0 = R, DEM1 = R, } \\ & \text { Gen } 1 \text { \& } 2 \text { modes only } \\ & \hline \end{aligned}$ |  | -6 |  | dB |
| $\mathrm{T}_{\text {TX-HF-DJ-DD }}$ | TX Dj > 1.5 MHz |  |  |  | 0.15 | UI |
| $\mathrm{T}_{\text {TX-HF-DJ-DD }}$ | TX RMS jitter $<1.5 \mathrm{MHz}$ |  |  |  | 3.0 | ps RMS |
| $\mathrm{T}_{\text {TX-RISE-FALL }}$ | Transmitter rise/fall time | $20 \%$ to $80 \%$ of differential output voltage | 35 | 45 |  | ps |
| T RF-MISMATCH | Transmitter rise/fall mismatch | $20 \%$ to $80 \%$ of differential output voltage |  | 0.01 | 0.1 | UI |
| $\overline{\mathrm{RL}_{\text {TX-DIFF }}}$ | TX Differential return | $0.05-1.25 \mathrm{GHz}$ |  | -16 |  | dB |
|  | loss | $1.25-2.5 \mathrm{GHz}$ |  | -12 |  | dB |
|  |  | 2.5-4 GHz |  | -11 |  | dB |
| $\mathrm{RL}_{\text {TX-CM }}$ | TX Common mode | 0.05-2.5 GHz |  | -12 |  | dB |
|  | return loss | 2.5-4 GHz |  | -8 |  | dB |
| $\mathrm{Z}_{\text {TX-DIFF-DC }}$ | DC differential TX impedance |  |  | 100 |  | $\Omega$ |
| $\mathrm{V}_{\text {TX-CM-AC-PP }}$ | TX AC common mode voltage | $\begin{aligned} & \hline \text { VOD = } 1.0 \mathrm{Vp}-\mathrm{p}, \\ & \text { DEM0 = 1, DEM1 = } \end{aligned}$ |  |  | 100 | mVp-p |
| $\overline{\mathrm{I}_{\text {TX-SHORT }}}$ | Transmitter short circuit current limit | Total current the transmitter can supply when shorted to VDD or GND |  | 20 |  | mA |
| $\overline{V_{\text {TX-CM-DC }}}$ <br> ACTIVE-IDLE-DELTA | Absolute delta of DC common mode voltage during LO and electrical idle |  |  |  | 100 | mV |
| $\mathrm{V}_{\text {TX-CM-DC-LINE- }}$ <br> DELTA | Absolute delta of DC common mode voltgae between TX+ and TX- |  |  |  | 25 | mV |
| $\mathrm{T}_{\text {TX-IDLE-DATA }}$ | Max time to transition to valid differential signal after idle | $\mathrm{VID}=1.0 \mathrm{Vp-p}, 8 \mathrm{Gbps}$ |  | 3.5 |  | ns |
| $\mathrm{T}_{\text {TX-DATA-IDLE }}$ | Max time to transition to idle after differential signal | $\mathrm{VID}=1.0 \mathrm{Vp-p}, 8 \mathrm{Gbps}$ |  | 6.2 |  | ns |
| $\mathrm{T}_{\text {PDEQ }}$ | Differential propagation delay | EQ = 00, (Note 6) |  | 200 |  | ps |
| $\mathrm{T}_{\text {LSK }}$ | Lane to lane skew | $\mathrm{T}=25 \mathrm{C}, \mathrm{VDD}=2.5 \mathrm{~V}$ |  | 25 |  | ps |
| $\mathrm{T}_{\text {PPSK }}$ | Part to part propagation delay skew | $\mathrm{T}=25 \mathrm{C}, \mathrm{VDD}=2.5 \mathrm{~V}$ |  | 40 |  | ps |


| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Equalization |  |  |  |  |  |  |
| DJE1 | Residual deterministic jitter at 8 Gbps | $\begin{aligned} & 35^{\prime \prime} \text { 4mils FR4, } \\ & \text { VID }=0.8 \mathrm{Vp-p}, \\ & \text { PRBS15, EQ }=1 \text { F'h, } \\ & \text { DEM }=0 \mathrm{~dB} \end{aligned}$ |  | 0.14 |  | UI |
| DJE2 | Residual deterministic jitter at 5 Gbps | $\begin{aligned} & 35^{\prime \prime} \text { 4mils FR4, } \\ & \text { VID }=0.8 \mathrm{Vp-p}, \\ & \text { PRBS15, EQ }=1 \text { F'h, } \\ & \text { DEM }=0 \mathrm{~dB} \end{aligned}$ |  | 0.1 |  | UI |
| DJE3 | Residual deterministic jitter at 2.5 Gbps | $\begin{aligned} & 35^{\prime \prime} \text { 4mils FR4, } \\ & \text { VID }=0.8 \mathrm{Vp-p}, \\ & \text { PRBS15, EQ }=1 \text { F'h, } \\ & \text { DEM }=0 \mathrm{~dB} \end{aligned}$ |  | 0.05 |  | UI |
| DJE4 | Residual deterministic jitter at 8 Gbps | 10 meters 30 awg cable, $\begin{aligned} & \text { VID }=0.8 \mathrm{Vp}-\mathrm{p}, \\ & \text { PRBS15, EQ }=2 \mathrm{~F} \text { h, } \\ & \text { DEM }=0 \mathrm{~dB} \end{aligned}$ |  | 0.16 |  | UI |
| DJE5 | Residual deterministic jitter at 5 Gbps | 10 meters 30 awg cable, VID $=0.8 \mathrm{Vp}-\mathrm{p}$, PRBS15, EQ = 2F'h, DEM $=0 \mathrm{~dB}$ |  | 0.1 |  | UI |
| DJE6 | Residual deterministic jitter at 2.5 Gbps | 10 meters 30 awg cable, $\begin{aligned} & \text { VID }=0.8 \mathrm{Vp}-\mathrm{p}, \\ & \text { PRBS15, EQ }=2 \mathrm{~F} \text { h, } \\ & \text { DEM }=0 \mathrm{~dB} \end{aligned}$ |  | 0.05 |  | UI |
| De-emphasis (Gen 1\&2 mode only) |  |  |  |  |  |  |
| DJD1 | Residual deterministic jitter at 2.5 Gbps AND 5.0 Gbps | $\begin{aligned} & 10 " 4 \text { mils FR4, } \\ & \text { VID }=0.8 \mathrm{Vp}-\mathrm{p}, \\ & \text { PRBS15, EQ }=00, \\ & \text { VOD }=1.0 \mathrm{Vp}-\mathrm{p}, \\ & \text { DEM }=-3.5 \mathrm{~dB}, \end{aligned}$ |  | 0.1 |  | UI |
| DJD2 | Residual deterministic jitter at 2.5 Gbps AND 5.0 Gbps | $\begin{aligned} & \hline 20 " 4 \text { mils FR4, } \\ & \text { VID }=0.8 \mathrm{Vp}-\mathrm{p}, \\ & \text { PRBS15, EQ }=00, \\ & \text { VOD }=1.0 \mathrm{Vp}-\mathrm{p}, \\ & \text { DEM }=-9 \mathrm{~dB}, \end{aligned}$ |  | 0.1 |  | UI |

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are guaranteed for a junction temperature range of $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$. Models are validated to Maximum Operating Voltages only.
Note 2: Typical values represent most likely parametric norms at VDD $=2.5 \mathrm{~V}, \mathrm{TA}=25^{\circ} \mathrm{C}$., and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.
Note 3: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
Note 4: Allowed supply noise ( mVp -p sine wave) under typical conditions.
Note 5: Guaranteed by device characterization.
Note 6: Propagation Delay measurements will change slightly based on the level of $E Q$ selected. $E Q=00$ will result in the shortest propagation delays.
Note 7: In GEN3 mode, the output VOD level is not fixed. It will be adjusted automatically based on the VID input amplitude level. The output VOD level set by DEMA/B[1:0] in GEN3 mode is dependent on the VID level and the frequency content. The DS80PCI800 repeater in GEN3 mode is designed to be transparent, so the TX-FIR (de-emphasis) is passed to the RX to support the PCle GEN3 handshake negotiation link training.

## Electrical Characteristics - Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SERIAL BUS INTERFACE DC SPECIFICATIONS |  |  |  |  |  |  |
| $\mathrm{V}_{\text {IL }}$ | Data, Clock Input Low Voltage |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | Data, Clock Input High Voltage |  | 2.1 |  | 3.6 | V |
| $\mathrm{I}_{\text {PULLUP }}$ | Current Through Pull-Up Resistor or Current Source | High Power Specification | 4 |  |  | mA |
| $\overline{\mathrm{V}} \mathrm{DD}$ | Nominal Bus Voltage |  | 2.375 |  | 3.6 | V |
| $\mathrm{I}_{\text {LEAK-Bus }}$ | Input Leakage Per Bus Segment | (Note 8) | -200 |  | +200 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {LEAK-Pin }}$ | Input Leakage Per Device Pin |  |  | -15 |  | $\mu \mathrm{A}$ |
| $\mathrm{C}_{1}$ | Capacitance for SDA and SCL | (Note 8, Note 9) |  |  | 10 | pF |
| $\mathrm{R}_{\text {TERM }}$ | External Termination Resistance pull to $\mathrm{V}_{\mathrm{DD}}=2.5 \mathrm{~V} \pm 5 \%$ OR $3.3 \mathrm{~V} \pm$ 10\% | Pullup $\mathrm{V}_{\mathrm{DD}}=3.3 \mathrm{~V}$, (Note 8, Note 9, Note 10) |  | 2000 |  | $\Omega$ |
|  |  | Pullup $\mathrm{V}_{\mathrm{DD}}=2.5 \mathrm{~V}$, <br> (Note 8, Note 9, Note 10) |  | 1000 |  | $\Omega$ |

SERIAL BUS INTERFACE TIMING SPECIFICATIONS

| FSMB | Bus Operating Frequency | ENSMB = VDD (Slave Mode) |  |  | 400 | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | ENSMB = FLOAT (Master Mode) | 280 | 400 | 520 | kHz |
| TBUF | Bus Free Time Between Stop and Start Condition |  | 1.3 |  |  | $\mu \mathrm{s}$ |
| THD:STA | Hold time after (Repeated) Start Condition. After this period, the first clock is generated. | At I $\mathrm{P}_{\text {PuLlup }}$, Max | 0.6 |  |  | $\mu \mathrm{s}$ |
| TSU:STA | Repeated Start Condition Setup Time |  | 0.6 |  |  | $\mu \mathrm{s}$ |
| TSU:STO | Stop Condition Setup Time |  | 0.6 |  |  | $\mu \mathrm{s}$ |
| THD:DAT | Data Hold Time |  | 0 |  |  | ns |
| TSU:DAT | Data Setup Time |  | 100 |  |  | ns |
| T Low | Clock Low Period |  | 1.3 |  |  | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\text {HIGH }}$ | Clock High Period | (Note 11) | 0.6 |  | 50 | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\mathrm{F}}$ | Clock/Data Fall Time | (Note 11) |  |  | 300 | ns |
| $\mathrm{t}_{\mathrm{R}}$ | Clock/Data Rise Time | (Note 11) |  |  | 300 | ns |
| $\mathrm{t}_{\mathrm{POR}}$ | Time in which a device must be operational after power-on reset | (Note 11, Note 12) |  |  | 500 | ms |

Note 8: Recommended value.
Note 9: Recommended maximum capacitance load per bus segment is 400 pF .
Note 10: Maximum termination voltage should be identical to the device supply voltage
Note 11: Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

Note 12: Guaranteed by Design. Parameter not tested in production.

## Timing Diagrams



FIGURE 1. CML Output and Rise and FALL Transition Time


FIGURE 2. Propagation Delay Timing Diagram


FIGURE 3. Transmit IDLE-DATA and DATA-IDLE Response Time


FIGURE 4. SMBus Timing Parameters

## Functional Descriptions

The DS80PCI402 is a low power media compensation 4 lane repeater optimized for PCl Express Gen $1 / 2$ and 3. The DS80PCI402 compensates for lossy FR-4 printed circuit board backplanes and balanced cables. The DS80PCI402 operates in 3 modes: Pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) and SMBus Master Mode (ENSMB = float) to load register informations from external EEPROM; please refer to SMBUS Master Mode for additional information.
Pin Control Mode:
When in pin mode (ENSMB = 0), equalization and de-emphasis can be selected via pin for each side independently. When de-emphasis is asserted VOD is automatically adjusted per the De- Emphasis table below. The RXDET pins provides automatic and manual control for input termination ( $50 \Omega$ or $>50 \mathrm{~K} \Omega$ ). RATE setting is also pin controllable with pin selections (Gen 1/2, auto detect and Gen 3). The receiver electrical idle detect threshold is also adjustable via the SD_TH pin.
SMBUS Mode:
When in SMBus mode (ENSMB = 1), the VOD (output amplitude), equalization, de-emphasis, and termination disable features are all programmable on a individual lane basis, instead of grouped by A or B as in the pin mode case. Upon assertion of ENSMB, the EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to ADO-AD3 SMBus address inputs. The other external control pins (RATE, RXDET and SD_TH) remain active unless their respective registers are written to and the appropriate override bit is set, in which case they are ignored until ENSMB is driven low (pin mode). On power-up and when ENSMB is driven low all registers are reset to their default state. If PRSNT is asserted while ENSMB is high, the registers retain their current state.
Equalization settings accessible via the pin controls were chosen to meet the needs of most PCle applications. If additional fine tuning or adjustment is needed, additional equal-
ization settings can be accessed via the SMBus registers. Each input has a total of 256 possible equalization settings. The tables show the 16 setting when the device is in pin mode. When using SMBus mode, the equalization, VOD and deEmphasis levels are set by registers.
The input control pins have been enhanced to have 4 different levels and provide a wider range of control settings when ENSMB=0.

## Table 1: 4-Level Control Pin Settings

| Pin Setting | Description | Voltage at Pin |
| :--- | :--- | :--- |
| 0 | Tie $1 \mathrm{k} \Omega$ to GND | $0.03 \times$ VDD |
| R | Tie $20 \mathrm{k} \Omega$ to GND | $1 / 3 \times$ VDD |
| Float | Float (leave pin open) | $2 / 3 \times$ VDD |
| 1 | Tie $1 \mathrm{k} \Omega$ to VDD | $0.98 \times$ VDD |

Note: The above required resistor value is for a single device. When there are multiple devices connected to the pull-up / pull-down resistor, the value must scale with the number of devices. If 4 devices are connected to a single pull-up or pull-down, the $1 \mathrm{k} \Omega$ resistor value should be $250 \Omega$. For the $20 \mathrm{k} \Omega$ to GND, this should also scale to $5 \mathrm{k} \Omega$.

### 3.3V or 2.5V Supply Mode Operation

The DS80PCI402 has an optional internal voltage regulator to provide the 2.5 V supply to the device. In 3.3 V mode operation, the VIN pin $=3.3 \mathrm{~V}$ is used to supply power to the device. The internal regulator will provide the 2.5 V to the VDD pins of the device and a 0.1 uF cap is needed at each of the 5 VDD pins for power supply de-coupling (total capacitance should be $\leq 0.5 \mathrm{uF}$ ), and the VDD pins should be left open. The VDD_SEL pin must be tied to GND to enable the internal regulator. In 2.5 V mode operation, the VIN pin should be left open and 2.5 V supply must be applied to the 5 VDD pins to power the device. The VDD_SEL pin must be left open (no connect) to disable the internal regulator.


FIGURE 5. 3.3V or 2.5V Supply Connection Diagram

## System Information

When using the DS80PCI402 in CPU systems, there are specific signal integrity settings to ensure signal integrity margin. The settings were achieved with completing extensive testing. Please contact your field representative for more information regarding the testing completed to achieve these settings.
For tuning the in the downstream direction (from CPU to EP).

- EQ: use the guidelines outlined in table 2.
- De-Emphasis: use the guidelines outlined in table 3.
- VOD: use the guidelines outlined in table 3.

For tuning in the upstream direction (from EP to CPU).

- EQ: use the guidelines outlined in table 2.
- De-Emphasis:

Table 2: Equalizer Settings

| Level | $\begin{aligned} & \text { EQA1 } \\ & \text { EQB1 } \end{aligned}$ | $\begin{aligned} & \text { EQAO } \\ & \text { EQBO } \end{aligned}$ | EQ - 8 bits [7:0] | $\begin{gathered} \mathrm{dB} \text { at } \\ 1.25 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} \mathrm{dB} \text { at } \\ 2.5 \mathrm{GHz} \end{gathered}$ | $\begin{aligned} & \mathrm{dB} \text { at } \\ & 4 \mathrm{GHz} \end{aligned}$ | Suggested Use |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | $00000000=0 \times 00$ | 2.1 | 3.7 | 4.9 | FR4 < 5 inch trace |
| 2 | 0 | R | $00000001=0 \times 01$ | 3.4 | 5.8 | 7.9 | FR4 5 inch 5-mil trace |
| 3 | 0 | Float | $00000010=0 \times 02$ | 4.8 | 7.7 | 9.9 | FR4 5 inch 4-mil trace |
| 4 | 0 | 1 | $00000011=0 \times 03$ | 5.9 | 8.9 | 11.0 | FR4 10 inch 5-mil trace |
| 5 | R | 0 | $00000111=0 \times 07$ | 7.2 | 11.2 | 14.3 | FR4 10 inch 4-mil trace |
| 6 | R | R | $00010101=0 \times 15$ | 6.1 | 11.4 | 14.6 | FR4 15 inch 4-mil trace |
| 7 | R | Float | $00001011=0 \times 0 \mathrm{~B}$ | 8.8 | 13.5 | 17.0 | FR4 20 inch 4-mil trace |
| 8 | R | 1 | $00001111=0 \times 0 \mathrm{~F}$ | 10.2 | 15.0 | 18.5 | FR4 25 to 30 inch 4-mil trace |
| 9 | Float | 0 | $01010101=0 \times 55$ | 7.5 | 12.8 | 18.0 | FR4 30 inch 4-mil trace |
| 10 | Float | R | $00011111=0 \times 1 \mathrm{~F}$ | 11.4 | 17.4 | 22.0 | FR4 35 inch 4-mil trace |
| 11 | Float | Float | $00101111=0 \times 2 \mathrm{~F}$ | 13.0 | 19.7 | 24.4 | 10m, 30awg cable |
| 12 | Float | 1 | $00111111=0 \times 3 \mathrm{~F}$ | 14.2 | 21.1 | 25.8 | 10m-12m cable |
| 13 | 1 | 0 | $10101010=0 x A A$ | 13.8 | 21.7 | 27.4 |  |
| 14 | 1 | R | $01111111=0 \times 7 \mathrm{~F}$ | 15.6 | 23.5 | 29.0 |  |
| 15 | 1 | Float | $10111111=0 x B F$ | 17.2 | 25.8 | 31.4 |  |
| 16 | 1 | 1 | $11111111=0 x F F$ | 18.4 | 27.3 | 32.7 |  |

Table 3: Output Voltage and De-emphasis Settings

| Level | DEMA1 <br> DEMB1 | DEMA0 <br> DEMB0 | VOD Vp-p | DEM dB <br> (see note below) | Inner Amplitude <br> Vp-p | Suggested Use |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 0.8 | 0 | 0.8 | FR4 $<5$ inch 4-mil trace |
| 2 | 0 | R | 0.9 | 0 | 0.9 | FR4 $<5$ inch 4-mil trace |
| 3 | 0 | Float | 0.9 | -3.5 | 0.6 | FR4 10 inch 4-mil trace |
| 4 | 0 | 1 | 1.0 | 0 | 1.0 | FR4 $<5$ inch 4-mil trace |
| 5 | R | 0 | 1.0 | -3.5 | 0.7 | FR4 10 inch 4-mil trace |
| 6 | R | R | 1.0 | -6 | 0.5 | FR4 15 inch 4-mil trace |
| 7 | R | Float | 1.1 | 0 | 1.1 | FR4 $<5$ inch 4-mil trace |
| 8 | R | 1 | 1.1 | -3.5 | 0.7 | FR4 10 inch 4-mil trace |
| 9 | Float | 0 | 1.1 | -6 | 0.6 | FR4 15 inch 4-mil trace |
| 10 | Float | R | 1.2 | 0 | 1.2 | FR4 $<5$ inch 4-mil trace |
| 11 | Float | Float | 1.2 | -3.5 | 0.8 | FR4 10 inch 4-mil trace |
| 12 | Float | 1 | 1.2 | -6 | 0.6 | FR4 15 inch 4-mil trace |
| 13 | 1 | 0 | 1.3 | 0 | 1.3 | FR4 $<5$ inch 4-mil trace |
| 14 | 1 | R | 1.3 | -3.5 | 0.9 | FR4 10 inch 4-mil trace |
| 15 | 1 | Float | 1.3 | -6 | 0.7 | FR4 15 inch 4-mil trace |
| 16 | 1 | 1 | 1.3 | -9 | 0.5 | FR4 20 inch 4-mil trace |

Note: The VOD output amplitude and DEM de-emphasis levels are set with the DEMA/B[1:0] pins.
The de-emphasis levels are also available in GEN 3 mode when RATE $=1$ (tied to VDD).
Table 4: RX-Detect Settings
\(\left.$$
\begin{array}{|c|c|c|c|c|l|}\hline \text { PRSNT\# } & \text { RXDET } & \begin{array}{c}\text { SMBus REG } \\
\text { bit[3:2] }\end{array} & \text { Input Termination } & \begin{array}{c}\text { Termination sensed } \\
\text { on output pins }\end{array} & \text { Comments } \\
\hline 0 & 0 & 00 & \text { High Impedance } & \text { X } & \begin{array}{l}\text { Manual RX-Detect, input is high } \\
\text { impedance mode }\end{array} \\
\hline 0 & \begin{array}{c}\text { Tie 20k } \\
\text { to GND }\end{array} & 01 & \begin{array}{c}\text { High Impedance } \\
50 \Omega\end{array} & \begin{array}{c}\text { High Z until receiver } \\
\text { is detected }\end{array} & \begin{array}{l}\text { Auto RX-Detect, outputs test every } 12 \\
\text { msec for } 600 \text { msec then stops; termination } \\
\text { is high-z until detection; once detected }\end{array}
$$ <br>
input termination is 50 \Omega <br>
Reset function by pulsing PRSNT\# high for <br>

5 usec then low again\end{array}\right]\)| (Default) |
| :--- |

## Table 5: Signal Detect Threshold Level

| SD_TH | SMBus REG bit [3:2] and [1:0] | Assert Level (typ) | De-assert Level (typ) |
| :--- | :--- | :--- | :--- |
| 0 | 10 | $210 \mathrm{mVp}-\mathrm{p}$ | $150 \mathrm{mVp}-\mathrm{p}$ |
| R | 01 | $160 \mathrm{mVp}-\mathrm{p}$ | $100 \mathrm{mVp}-\mathrm{p}$ |
| F (default) | 00 | $180 \mathrm{mVp}-\mathrm{p}$ | $110 \mathrm{mVp}-\mathrm{p}$ |
| 1 | 11 | $190 \mathrm{mVp}-\mathrm{p}$ | $130 \mathrm{mVp}-\mathrm{p}$ |
| Note: VDD $=2.5 \mathrm{~V}, 25^{\circ} \mathrm{C}$ and 0101 pattern at 8 Gbps |  |  |  |

## SMBUS Master Mode

The DS80PCI402 device supports reading directly from an external EEPROM device by implementing SMBus Master mode. When using the SMBus master mode, the DS80PCI402 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines.

- Set ENSMB = Float - enable the SMBUS master mode.
- The external EEPROM device address byte must be $0 x A 0$ ' h and capable of 400 kHz operation at 2.5 V and 3.3 V supply.
- Set the $A D[3: 0]$ inputs for SMBus address byte. When the $A D[3: 0]=0000$ 'b, the device address byte is $B^{\prime} h$.

When tying multiple DS80PCI402 devices to the SDA and SCL bus, use these guidelines to configure the devices.

- Use SMBus AD[3:0] address bits so that each device can loaded it's configuration from the EEPROM. Example below is for 4 device.
U1: $\mathrm{AD}[3: 0]=0000=0 x B 0 ' \mathrm{~h}$,
U2: $A D[3: 0]=0001=0 \times B 2 ' h$,
U3: $A D[3: 0]=0010=0 x B 4 '^{\prime} h$,
U4: AD[3:0] = $0011=0 \times B 6$ 'h
- Use a pull-up resistor on SDA and SCL; value $=2 k$ ohms
- Daisy-chain READEN\# (pin 26) and ALL_DONE\# (pin 27) from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.

1. Tie READEN\# of the 1 st device in the chain (U1) to GND
2. Tie ALL_DONE\# of U1 to READEN\# of U2
3. Tie ALL_DONE\# of U2 to READEN\# of U3
4. Tie ALL_DONE\# of U3 to READEN\# of U4
5. Optional: Tie ALL_DONE\# output of U4 to a LED to show the devices have been loaded successfully

Below is an example of a 2 kbits ( $256 \times 8$-bit) EEPROM in hex format for the DS80PCI402 device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the I2C bus. CRC enable flag to enable/disable CRC checking. If CRC checking is disabled, a fixed pattern ( 8 'hA5) is written/read instead of the CRC byte from the CRC location, to simplify the control. There is a MAP bit to flag the presence of an address map that specifies the configuration data start in the EEPROM. If the MAP bit is not present the configuration data start address is derived from the DS80PCI402 address and the configuration data size. A bit to indicate an EEPROM size $>256$ bytes is necessary to properly address the EEPROM. There are 37 bytes of data size for each DS80PCI402 device.

## :2000000000001000000407002FAD4002FAD4002FAD4002FAD401805F5A8005F5A8005F5AD8

:200020008005F5A800005454000000000000000000000000000000000000000000000000000F6 :20006000000000000000000000000000000000000000000000000000000000000000000080 :200080000000000000000000000000000000000000000000000000000000000000000000060 :2000A00000000000000000000000000000000000000000000000000000000000000000000040 :2000C0000000000000000000000000000000000000000000000000000000000000000000000020 :2000E00000000000000000000000000000000000000000000000000000000000000000000000 :2000400000000000000000000000000000000000000000000000000000000000000000000A0
DS80PCI402

| Table 6: EEPROM Register Map - Single Device with Default Value |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| EEPROM Address Byte |  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Blt 0 |
| Description | 0 | CRC EN | Address Map <br> Present | EEPROM > 256 <br> Bytes | RES | DEVICE COUNT <br> [3] | DEVICE COUNT <br> [2] | DEVICE COUNT <br> [1] | DEVICE COUNT [0] |
| Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 1 | RES | RES | RES | RES | RES | RES | RES | RES |
| Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 2 | Max EEPROM Burst size[7] | Max EEPROM <br> Burst size[6] | Max EEPROM <br> Burst size[5] | Max EEPROM Burst size[4] | Max EEPROM <br> Burst size[3] | Max EEPROM <br> Burst size[2] | Max EEPROM <br> Burst size[1] | Max EEPROM <br> Burst size[0] |
| Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 3 | PWDN_ch7 | PWDN_ch6 | PWDN_ch5 | PWDN_ch4 | PWDN_ch3 | PWDN_ch2 | PWDN_ch1 | PWDN_ch0 |
| Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 4 | lpbk_1 | lpbk_0 | PWDN_INPUTS | PWDN_OSC | Ovrd_PRSNT | RES | RES | RES |
| Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 5 | RES | RES | RES | RES | RES | rxdet_btb_en | Ovrd_idle_th | Ovrd_RES |
| Value |  | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Description | 6 | Ovrd_IDLE | Ovrd_RX_DET | Ovrd_RATE | Ovrd_RES | Ovrd_RES | rx_delay_sel_2 | rx_delay_sel_1 | r_delay_sel_0 |
| Value |  | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| Description | 7 | RD_delay_sel_3 | RD_delay_sel_2 | RD_delay_sel_1 | RD_delay_sel_0 | ch0_Idle_auto | ch0_Idle_sel | ch0_RXDET_1 | ch0_RXDET_0 |
| Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 8 | ch0_BST_7 | ch0_BST_6 | ch0_BST_5 | ch0_BST_4 | ch0_BST_3 | ch0_BST_2 | ch0_BST_1 | ch0_BST_0 |
| Value |  | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| Description | 9 | ch0_Sel_scp | ch0_Sel_mode | ch0_RES_2 | ch0_RES_1 | ch0_RES_0 | ch0_VOD_2 | ch0_VOD_1 | ch0_VOD_0 |
| Value |  | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| Description | 10 | ch0_DEM_2 | ch0_DEM_1 | ch0_DEM_0 | ch0_Slow | ch0_idle_tha_1 | ch0_idle_tha_0 | ch0_idle_thd_1 | ch0_idle_thd_0 |
| Value |  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 11 | ch1_Idle_auto | ch1_Idle_sel | ch1_RXDET_1 | ch1_RXDET_0 | ch1_BST_7 | ch1_BST_6 | ch1_BST_5 | ch1_BST_4 |
| Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Description | 12 | ch1_BST_3 | ch1_BST_2 | ch1_BST_1 | ch1_BST_0 | ch1_Sel_scp | ch1_Sel_mode | ch1_RES_2 | ch1_RES_1 |
| Value |  | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| Description | 13 | ch1_RES_0 | ch1_VOD_2 | ch1_VOD_1 | ch1_VOD_0 | ch1_DEM_2 | ch1_DEM_1 | ch1_DEM_0 | ch1_Slow |
| Value |  | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| Description | 14 | ch1_idle_tha_1 | ch1_idle_tha_0 | ch1_idle_thd_1 | ch1_idle_thd_0 | ch2_Idle_auto | ch2_Idle_sel | ch2_RXDET_1 | ch2_RXDET_0 |
| Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


| Description | 15 | ch2_BST_7 | ch2_BST_6 | ch2_BST_5 | ch2_BST_4 | ch2_BST_3 | ch2_BST_2 | ch2_BST_1 | ch2_BST_0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Value |  | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| Description | 16 | ch2_Sel_scp | ch2_Sel_mode | ch2_RES_2 | ch2_RES_1 | ch2_RES_0 | ch2_VOD_2 | ch2_VOD_1 | ch2_VOD_0 |
| Value |  | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| Description | 17 | ch2_DEM_2 | ch2_DEM_1 | ch2_DEM_0 | ch2_Slow | ch2_idle_tha_1 | ch2_idle_tha_0 | ch2_idle_thd_1 | ch2_idle_thd_0 |
| Value |  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 18 | ch3_Idle_auto | ch3_Idle_sel | ch3_RXDET_1 | ch3_RXDET_0 | ch3_BST_7 | ch3_BST_6 | ch3_BST_5 | ch3_BST_4 |
| Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Description | 19 | ch3_BST_3 | ch3_BST_2 | ch3_BST_1 | ch3_BST_0 | ch3_Sel_scp | ch3_Sel_mode | ch3_RES_2 | ch3_RES_1 |
| Value |  | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| Description | 20 | ch3_RES_0 | ch3_VOD_2 | ch3_VOD_1 | ch3_VOD_0 | ch3_DEM_2 | ch3_DEM_1 | ch3_DEM_0 | ch3_Slow |
| Value |  | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| Description | 21 | ch3_idle_tha_1 | ch3_idle_tha_0 | ch3_idle_thd_1 | ch3_idle_thd_0 | ovrd_fast_idle | en_high_idle_th_n | en_high_idle_th_s | en_fast_idle_n |
| Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Description | 22 | en_fast_idle_s | eqsd_mgain_n | eqsd_mgain_s | ch4_Idle_auto | ch4_Idle_sel | ch4_RXDET_1 | ch4_RXDET_0 | ch4_BST_7 |
| Value |  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 23 | ch4_BST_6 | ch4_BST_5 | ch4_BST_4 | ch4_BST_3 | ch4_BST_2 | ch4_BST_1 | ch4_BST_0 | ch4_Sel_scp |
| Value |  | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| Description | 24 | ch4_Sel_mode | ch4_RES_2 | ch4_RES_1 | ch4_RES_0 | ch4_VOD_2 | ch4_VOD_1 | ch4_VOD_0 | ch4_DEM_2 |
| Value |  | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| Description | 25 | ch4_DEM_1 | ch4_DEM_0 | ch4_Slow | ch4_idle_tha_1 | ch4_idle_tha_0 | ch4_idle_thd_1 | ch4_idle_thd_0 | ch5_Idle_auto |
| Value |  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 26 | ch5_Idle_sel | ch5_RXDET_1 | ch5_RXDET_0 | ch5_BST_7 | ch5_BST_6 | ch5_BST_5 | ch5_BST_4 | ch5_BST_3 |
| Value |  | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| Description | 27 | ch5_BST_2 | ch5_BST_1 | ch5_BST_0 | ch5_Sel_scp | ch5_Sel_mode | ch5_RES_2 | ch5_RES_1 | ch5_RES_0 |
| Value |  | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| Description | 28 | ch5_VOD_2 | ch5_VOD_1 | ch5_VOD_0 | ch5_DEM_2 | ch5_DEM_1 | ch5_DEM_0 | ch5_Slow | ch5_idle_tha_1 |
| Value |  | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| Description | 29 | ch5_idle_tha_0 | ch5_idle_thd_1 | ch5_idle_thd_0 | ch6_Idle_auto | ch6_Idle_sel | ch6_RXDET_1 | ch6_RXDET_0 | ch6_BST_7 |
| Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 30 | ch6_BST_6 | ch6_BST_5 | ch6_BST_4 | ch6_BST_3 | ch6_BST_2 | ch6_BST_1 | ch6_BST_0 | ch6_Sel_scp |
| Value |  | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| Description | 31 | ch6_Sel_mode | ch6_RES_2 | ch6_RES_1 | ch6_RES_0 | ch6_VOD_2 | ch6_VOD_1 | ch6_VOD_0 | ch6_DEM_2 |
| Value |  | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |

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| Description | 32 | ch6_DEM_1 | ch6_DEM_0 | ch6_Slow | ch6_idle_tha_1 | ch6_idle_tha_0 | ch6_idle_thd_1 | ch6_idle_thd_0 | ch7_Idle_auto |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Value |  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 33 | ch7_Idle_sel | ch7_RXDET_1 | ch7_RXDET_0 | ch7_BST_7 | ch7_BST_6 | ch7_BST_5 | ch7_BST_4 | ch7_BST_3 |
| Value |  | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| Description | 34 | ch7_BST_2 | ch7_BST_1 | ch7_BST_0 | ch7_Sel_scp | ch7_Sel_mode | ch7_RES_2 | ch7_RES_1 | ch7_RES_0 |
| Value |  | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| Description | 35 | ch7_VOD_2 | ch7_VOD_1 | ch7_VOD_0 | ch7_DEM_2 | ch7_DEM_1 | ch7_DEM_0 | ch7_Slow | ch7_idle_tha_1 |
| Value |  | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| Description | 36 | ch7_idle_tha_0 | ch7_idle_thd_1 | ch7_idle_thd_0 | iph_dac_ns_1 | iph_dac_ns_0 | ipp_dac_ns_1 | ipp_dac_ns_0 | ipp_dac_1 |
| Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 37 | ipp_dac_0 | RD23_67 | RD01_45 | RD_PD_ovrd | RD_Sel_test | RD_RESET_ovrd | PWDB_input_DC | DEM_VOD_ovrd |
| Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | 38 | DEM_ovrd_N2 | DEM_ovrd_N1 | DEM_ovrd_N0 | VOD_ovrd_N2 | VOD_ovrd_N1 | VOD_ovrd_N0 | SPAREO | SPARE1 |
| Value |  | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| Description | 39 | DEM__ovrd_S2 | DEM__ovrd_S1 | DEM_ovrd_S0 | VOD_ovrd_S2 | VOD_ovrd_S1 | VOD_ovrd_S0 | SPARE0 | SPARE1 |
| Value |  | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |

Table 7: Example of EEPROM for 4 Devices using 2 Address Maps

| EEPROM <br> Address | Address (Hex) | EEPROM <br> Data | Comments |
| :---: | :---: | :---: | :---: |
| 0 | 00 | 0x43 | CRC_EN = 0, Address Map $=1$, $>256$ bytes $=0$, Device Count[3:0] = 3 |
| 1 | 01 | 0x00 |  |
| 2 | 02 | 0x08 | EEPROM Burst Size |
| 3 | 03 | 0x00 | CRC not used |
| 4 | 04 | 0x0B | Device 0 Address Location |
| 5 | 05 | 0x00 | CRC not used |
| 6 | 06 | 0x0B | Device 1 Address Location |
| 7 | 07 | 0x00 | CRC not used |
| 8 | 08 | 0x30 | Device 2 Address Location |
| 9 | 09 | 0x00 | CRC not used |
| 10 | 0A | 0x30 | Device 3 Address Location |
| 11 | OB | 0x00 | Begin Device 0, 1 Address Offset 3 |
| 12 | OC | 0x00 |  |
| 13 | OD | 0x04 |  |
| 14 | OE | 0x07 |  |
| 15 | OF | 0x00 |  |
| 16 | 10 | 0x00 | EQ CHB0 $=00$ |
| 17 | 11 | 0xAB | $\mathrm{VOD} \mathrm{CHB0}=1.0 \mathrm{~V}$ |
| 18 | 12 | 0x00 | DEM CHBO $=0(0 \mathrm{~dB})$ |
| 19 | 13 | 0x00 | EQ CHB1 = 00 |
| 20 | 14 | 0x0A | VOD CHB1 $=1.0 \mathrm{~V}$ |
| 21 | 15 | 0xB0 | DEM CHB1 = 0 (0dB) |
| 22 | 16 | 0x00 |  |
| 23 | 17 | 0x00 | EQ CHB2 $=00$ |
| 24 | 18 | 0xAB | VOD CHB2 $=1.0 \mathrm{~V}$ |
| 25 | 19 | 0x00 | DEM CHB2 $=0$ (0dB) |
| 26 | 1A | 0x00 | EQ CHB3 $=00$ |
| 27 | 1B | 0x0A | VOD CHB3 $=1.0 \mathrm{~V}$ |
| 28 | 1C | 0xB0 | DEM CHB3 $=0$ (0dB) |
| 29 | 1D | 0x01 |  |
| 30 | 1 E | 0x80 |  |
| 31 | 1F | 0x01 | EQ CHAO $=00$ |
| 32 | 20 | 0x56 | $\mathrm{VOD} \mathrm{CHAO}=1.0 \mathrm{~V}$ |
| 33 | 21 | 0x00 | DEM CHAO $=0$ (0dB) |
| 34 | 22 | 0x00 | EQ CHA1 = 00 |
| 35 | 23 | 0x15 | VOD CHA1 $=1.0 \mathrm{~V}$ |
| 36 | 24 | 0x60 | DEM CHA1 $=0(0 \mathrm{~dB})$ |
| 37 | 25 | 0x00 |  |
| 38 | 26 | 0x01 | EQ CHA2 $=00$ |

Note: CRC_EN = 0, Address Map = 1, >256 byte = 0, Device Count[3:0] $=3$. This example has all 8-channels set to EQ = 00 ( min boost), $\mathrm{VOD}=1.0 \mathrm{~V}, \mathrm{DEM}=0(0 \mathrm{~dB})$ and multiple device can point to the same address map.

## System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. $\mathrm{ENSMB}=1 \mathrm{k} \Omega$ to VDD to enable SMBus slave mode and allow access to the configuration registers.
The DS80PCI402 has the AD[3:0] inputs in SMBus mode. These pins are the user set SMBUS slave address inputs. The $\mathrm{AD}[3: 0]$ pins have internal pull-down. When left floating or pulled low the $A D[3: 0]=0000$ 'b, the device default address byte is B0'h. Based on the SMBus 2.0 specification, the DS80PCI402 has a 7 -bit slave address. The LSB is set to $0^{\prime} b$ (for a WRITE). The device supports up to 16 address byte, which can be set with the $\mathrm{AD}[3: 0]$ inputs. Below are the 16 addresses.

Table 8: Device Slave Address Bytes

| AD[3:0] Settings | Address Bytes (HEX) |
| :--- | :--- |
| 0000 | B0 |
| 0001 | B2 |
| 0010 | B4 |
| 0011 | B6 |
| 0100 | B8 |
| 0101 | BA |
| 0110 | BC |
| 0111 | BE |
| 1000 | C0 |
| 1001 | C2 |
| 1010 | C4 |
| 1011 | C6 |
| 1100 | C8 |
| 1101 | CA |
| 1110 | CC |
| 1111 | CE |

The SDA, SCL pins are 3.3 V tolerant, but are not 5V tolerant. External pull-up resistor is required on the SDA. The resistor value can be from $1 \mathrm{k} \Omega$ to $5 \mathrm{k} \Omega$ depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

## TRANSFER OF DATA VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.
There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.
STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.
IDLE: If SCL and SDA are both High for a time exceeding $\mathrm{t}_{\text {BUF }}$ from the last detected STOP condition or if they are High for a total exceeding the maximum specification for $\mathrm{t}_{\mathrm{HIGH}}$ then the bus will transfer to the IDLE state.

## SMBus TRANSACTIONS

The device supports WRITE and READ transactions. See Register Description table for register address, type (Read/ Write, Read Only), default value and function information.

## WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a " 0 " indicating a WRITE.
2. The Device (Slave) drives the ACK bit ("0").
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit ("0").
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit ("0").
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

## READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a " 0 " indicating a WRITE.
2. The Device (Slave) drives the ACK bit ("0").
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit ("0").
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a "1" indicating a READ.
7. The Device drives an ACK bit " 0 ".
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit "1"indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.
Please see SMBus Register Map Table for more information.

## Table 9: SMBUS Slave Mode Register Map

| Address | Register Name | Bit (s) | Field | Type | $\begin{array}{\|l\|} \hline \text { Default } \\ \hline 0 \times 00 \\ \hline \end{array}$ |  Description <br> Set bit to 0.  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0x00 | Observation, Reset | 7 | Reserved | R/W | $0 \times 00$ |  |
|  |  | 6:3 | $\begin{aligned} & \text { Address Bit } \\ & \text { AD[3:0] } \end{aligned}$ | R |  | Observation of AD[3:0] bits [6]: AD3 [5]: AD2 [4]: AD1 [3]: AD0 |
|  |  | 2 | EEPROM Read Done | R |  | 1: Device completed the read from external EEPROM. |
|  |  | 1 | Block Reset | R/W |  | 1: Block bit 0 from resettting the registers; self clearing. |
|  |  | 0 | Reset | R/W |  | SMBus Reset <br> 1: Reset registers to default value; self clearing. |
| 0x01 | PWDN Channels | 7:0 | PWDN CHx | R/W | 0x00 | Power Down per Channel <br> [7]: CH7 - CHA_3 <br> [6]: CH6 - CHA_2 <br> [5]: CH5 - CHA_1 <br> [4]: CH4 - CHA_0 <br> [3]: CH3 - CHB_3 <br> [2]: $\mathrm{CH} 2-\mathrm{CHB}$ _2 <br> [1]: CH1 - CHB_1 <br> [0]: CHO - CHB_0 <br> OO'h = all channels enabled <br> FF'h = all channels disabled <br> Note: override PRSNT pin. |
| 0x02 | Override PRSNT, LPBK Control | 7:6 | Reserved | R/W | 0x00 | Set bits to 0 . |
|  |  | 5:4 | LPBK <br> Control |  |  | 00: Use LPBK pin control <br> 01: INA_n to OUTB_n loopback <br> 10: INB_n to OUTA_n loopback <br> 11: Disable loopback and ignore LPBK pin. |
|  |  | 3:1 | Reserved |  |  | Set bits to 0. |
|  |  | 0 | Override PRSNT pin |  |  | 1: Block PRSNT pin control 0: Allow PRSNT pin control |
| 0x05 | Slave Mode CRC bits | 7:0 | CRC bits | R/W | 0x00 | CRC bits [7:0] |
| 0x06 | Slave CRC Control | 7:5 | Reserved | R/W | 0x10 | Set bits to 0. |
|  |  | 4 | Reserved |  |  | Set bit to 1. |
|  |  | 3 | Slave CRC |  |  | 1: Disables the slave CRC mode 0 : Enables the slave CRC mode Note: In order to change VOD, DEM and EQ of the channels in slave mode, set bit to 1 to disable the CRC. |
|  |  | 2:0 | Reserved |  |  | Set bits to 0 . |


| $0 \times 08$ | Override Pin Control | 7 | Reserved | R/W | 0x00 | Set bit to 0. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 6 | Override SD_TH |  |  | 1: Block SD_TH pin control <br> 0: Allow SD_TH pin control |
|  |  | 5 | Reserved |  |  | Set bit to 0 . |
|  |  | 4 | Override IDLE |  |  | 1: IDLE control by registers <br> 0: IDLE control by signal detect |
|  |  | 3 | Override RXDET |  |  | 1: Block RXDET pin control 0: Allow RXDET pin control |
|  |  | 2 | Override RATE |  |  | 1: Block RATE pin control 0: Allow RATE pin control |
|  |  | 1 | Reserved |  |  | Set bit to 0 . |
|  |  | 0 | Reserved |  |  | Set bit to 0 . |
| 0x0E | CH0 - CHB0 | 7:6 | Reserved | R/W | 0x00 | Set bits to 0 . |
|  | IDLE, RXDET | 5 | IDLE_AUTO |  |  | 1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. |
|  |  | 4 | IDLE_SEL |  |  | 1: Output is MUTED (electrical idle) 0 : Output is ON <br> Note: override IDLE control. |
|  |  | 3:2 | RXDET |  |  | 00: Input is high-z impedance <br> 01: Auto RX-Detect, outputs test every 12 ms for 600 ms ( 50 times) then stops; termination is high-z until detection; once detected input termination is $50 \Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is $50 \Omega$ <br> 11: Input is $50 \Omega$ <br> Note: override RXDET pin. |
|  |  | 1:0 | Reserved |  |  | Set bits to 0 . |
| 0x0F | $\begin{aligned} & \mathrm{CHO}-\mathrm{CHBO} \\ & \mathrm{EQ} \end{aligned}$ | 7:0 | EQ Control | R/W | 0x2F | IB0 EQ Control - total of 256 levels. <br> See Table 2: Equalizer Settings. |
| 0x10 | CHO - CHBO VOD | 7 | Short Circuit Protection | R/W | 0xAD | 1: Enable the short circuit protection 0: Disable the short circuit protection |
|  |  | 6 | RATE_SEL |  |  | 1: Gen $1 / 2$, <br> 0 : Gen 3 <br> Note: override the RATE pin. |
|  |  | 5:3 | Reserved |  |  | Set bits to default value - 101. |
|  |  | 2:0 | VOD Control |  |  | ```OBO VOD Control 000:0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V``` |


| 0x11 | $\begin{aligned} & \mathrm{CHO}-\mathrm{CHBO} \\ & \mathrm{DEM} \end{aligned}$ | 7 | RXDET STATUS | R | 0x02 | ```Observation bit for RXDET CHO - CHBO. 1: RX = detected 0 : \(\mathrm{RX}=\) not detected``` |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 6:5 | RATE_DET STATUS | R |  | ```Observation bit for RATE_DET CH0 - CHBO. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G)``` |
|  |  | 4:3 | Reserved | R/W |  | Set bits to 0 . |
|  |  | 2:0 | DEM Control | R/W |  | OB0 DEM Control $000: 0 \mathrm{~dB}$ $001:-1.5 \mathrm{~dB}$ $010:-3.5 \mathrm{~dB}$ (default) $011:-5 \mathrm{~dB}$ $100:-6 \mathrm{~dB}$ $101:-8 \mathrm{~dB}$ $110:-9 \mathrm{~dB}$ $111:-12 \mathrm{~dB}$ |
| 0x12 | CHO - CHBO <br> IDLE Threshold | 7:4 | Reserved | R/W | 0x00 | Set bits to 0 . |
|  |  | 3:2 | IDLE thd |  |  | $\begin{aligned} & \text { De-assert threshold } \\ & 00=110 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=100 \mathrm{mVp}-\mathrm{p} \\ & 10=150 \mathrm{mVp}-\mathrm{p} \\ & 11=130 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
|  |  | 1:0 | IDLE tha |  |  | Assert threshold $\begin{aligned} & 00=180 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=160 \mathrm{mVp}-\mathrm{p} \\ & 10=210 \mathrm{mVp}-\mathrm{p} \\ & 11=190 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
| 0x15 | CH1 - CHB1 IDLE, RXDET | 7:6 | Reserved | R/W | 0x00 | Set bits to 0. |
|  |  | 5 | IDLE_AUTO |  |  | 1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. |
|  |  | 4 | IDLE_SEL |  |  | 1: Output is MUTED (electrical idle) <br> 0 : Output is ON <br> Note: override IDLE control. |
|  |  | 3:2 | RXDET |  |  | 00: Input is high-z impedance <br> 01: Auto RX-Detect, outputs test every 12 ms for 600 ms ( 50 times) then stops; termination is high-z until detection; once detected input termination is $50 \Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is $50 \Omega$ <br> 11: Input is $50 \Omega$ <br> Note: override RXDET pin. |
|  |  | 1:0 | Reserved |  |  | Set bits to 0 . |
| 0x16 | $\begin{array}{\|l\|} \hline \mathrm{CH} 1-\mathrm{CHB} 1 \\ \mathrm{EQ} \\ \hline \end{array}$ | 7:0 | EQ Control | R/W | 0x2F | IB1 EQ Control - total of 256 levels. See Table 2: Equalizer Settings. |


| 0x17 | CH1-CHB1 VOD | 7 | Short Circuit | R/W | OxAD | 1: Enable the short circuit protection |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 6 | RATE_SEL |  |  | 1: Gen $1 / 2$, <br> 0 : Gen 3 <br> Note: override the RATE pin. |
|  |  | 5:3 | Reserved |  |  | Set bits to default value - 101. |
|  |  | 2:0 | VOD Control |  |  | OB1 VOD Control <br> 000: 0.7 V <br> 001: 0.8 V <br> 010: 0.9 V <br> 011: 1.0 V <br> 100: 1.1 V <br> 101: 1.2 V (default) <br> 110: 1.3 V <br> 111: 1.4 V |
| 0x18 | $\begin{aligned} & \text { CH1-CHB1 } \\ & \text { DEM } \end{aligned}$ | 7 | RXDET STATUS | R | 0x02 | Observation bit for RXDET CH1 - CHB1. <br> 1: $\mathrm{RX}=$ detected <br> 0 : RX = not detected |
|  |  | 6:5 | RATE_DET STATUS | R |  | ```Observation bit for RATE_DET CH1 - CHB1. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G)``` |
|  |  | 4:3 | Reserved | R/W |  | Set bits to 0 . |
|  |  | 2:0 | DEM Control | R/W |  | ```OB1 DEM Control 000: 0 dB 001: -1.5 dB 010: -3.5 dB (default) 011:-5 dB 100: -6 dB 101:-8 dB 110: -9 dB 111: -12 dB``` |
| 0x19 | CH1-CHB1 IDLE Threshold | 7:4 | Reserved | R/W | 0x00 | Set bits to 0 . |
|  |  | 3:2 | IDLE thd |  |  | De-assert threshold $\begin{aligned} & 00=110 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=100 \mathrm{mVp}-\mathrm{p} \\ & 10=150 \mathrm{mVp}-\mathrm{p} \\ & 11=130 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
|  |  | 1:0 | IDLE tha |  |  | Assert threshold $\begin{aligned} & 00=180 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=160 \mathrm{mVp}-\mathrm{p} \\ & 10=210 \mathrm{mVp}-\mathrm{p} \\ & 11=190 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |


| 0x1C | CH2-CHB2 IDLE, RXDET | 7:6 | Reserved | R/W | 0x00 | Set bits to 0. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 5 | IDLE_AUTO |  |  | 1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. |
|  |  | 4 | IDLE_SEL |  |  | 1: Output is MUTED (electrical idle) 0 : Output is ON <br> Note: override IDLE control. |
|  |  | 3:2 | RXDET |  |  | 00: Input is high-z impedance <br> 01: Auto RX-Detect, outputs test every 12 ms for 600 ms ( 50 times) then stops; termination is high-z until detection; once detected input termination is $50 \Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is $50 \Omega$ <br> 11: Input is $50 \Omega$ <br> Note: override RXDET pin. |
|  |  | 1:0 | Reserved |  |  | Set bits to 0 . |
| 0x1D | $\begin{aligned} & \mathrm{CH} 2-\mathrm{CHB} 2 \\ & \mathrm{EQ} \end{aligned}$ | 7:0 | EQ Control | R/W | 0x2F | IB2 EQ Control - total of 256 levels. See Table 2: Equalizer Settings. |
| 0x1E | $\begin{aligned} & \mathrm{CH} 2-\mathrm{CHB2} \\ & \mathrm{VOD} \end{aligned}$ | 7 | Short Circuit Protection | R/W | 0xAD | 1: Enable the short circuit protection 0 : Disable the short circuit protection |
|  |  | 6 | RATE_SEL |  |  | $\begin{array}{\|l\|} \hline \text { 1: Gen } 1 / 2, \\ \text { 0: Gen } 3 \\ \text { Note: override the RATE pin. } \\ \hline \end{array}$ |
|  |  | 5:3 | Reserved |  |  | Set bits to default value - 101. |
|  |  | 2:0 | VOD Control |  |  | OB2 VOD Control $000: 0.7 \mathrm{~V}$ $001: 0.8 \mathrm{~V}$ $010: 0.9 \mathrm{~V}$ $011: 1.0 \mathrm{~V}$ $100: 1.1 \mathrm{~V}$ $101: 1.2 \mathrm{~V}$ (default) $110: 1.3 \mathrm{~V}$ $111: 1.4 \mathrm{~V}$ |
| 0x1F | $\begin{aligned} & \mathrm{CH} 2-\mathrm{CHB} 2 \\ & \mathrm{DEM} \end{aligned}$ | 7 | RXDET STATUS | R | 0x02 | ```Observation bit for RXDET CH2 - CHB2. 1: RX = detected \(0: R X=\) not detected``` |
|  |  | 6:5 | RATE_DET STATUS | R |  | Observation bit for RATE_DET CH2 - CHB2. 00: GEN1 (2.5G) <br> 01: GEN2 (5G) <br> 11: GEN3 (8G) |
|  |  | 4:3 | Reserved | R/W |  | Set bits to 0 . |
|  |  | 2:0 | DEM Control | R/W |  | OB2 DEM Control $000: 0 \mathrm{~dB}$ $001:-1.5 \mathrm{~dB}$ $010:-3.5 \mathrm{~dB}$ (default) $011:-5 \mathrm{~dB}$ $100:-6 \mathrm{~dB}$ $101:-8 \mathrm{~dB}$ $110:-9 \mathrm{~dB}$ $111:-12 \mathrm{~dB}$ |


| $0 \times 20$ | $\begin{aligned} & \mathrm{CH} 2-\mathrm{CHB} 2 \\ & \text { IDLE Threshold } \end{aligned}$ | 7:4 | Reserved | R/W | 0x00 | Set bits to 0. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 3:2 | IDLE thd |  |  | De-assert threshold $\begin{aligned} & 00=110 \mathrm{mVp}-\mathrm{p}(\text { default }) \\ & 01=100 \mathrm{mVp}-\mathrm{p} \\ & 10=150 \mathrm{mVp}-\mathrm{p} \\ & 11=130 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
|  |  | 1:0 | IDLE tha |  |  | Assert threshold $\begin{aligned} & 00=180 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=160 \mathrm{mVp}-\mathrm{p} \\ & 10=210 \mathrm{mVp}-\mathrm{p} \\ & 11=190 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
| 0x23 | $\begin{aligned} & \text { CH3 - CHB3 } \\ & \text { IDLE, RXDET } \end{aligned}$ | 7:6 | Reserved | R/W | 0x00 | Set bits to 0 . |
|  |  | 5 | IDLE_AUTO |  |  | 1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. |
|  |  | 4 | IDLE_SEL |  |  | 1: Output is MUTED (electrical idle) 0 : Output is ON <br> Note: override IDLE control. |
|  |  | 3:2 | RXDET |  |  | 00: Input is high-z impedance <br> 01: Auto RX-Detect, outputs test every 12 ms for 600 ms ( 50 times) then stops; termination is high-z until detection; once detected input termination is $50 \Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is $50 \Omega$ <br> 11: Input is $50 \Omega$ <br> Note: override RXDET pin. |
|  |  | 1:0 | Reserved |  |  | Set bits to 0 . |
| 0x24 | $\begin{aligned} & \mathrm{CH} 3-\mathrm{CHB} 3 \\ & \mathrm{EQ} \end{aligned}$ | 7:0 | EQ Control | R/W | 0x2F | IB3 EQ Control - total of 256 levels. See Table 2: Equalizer Settings. |
| 0x25 | $\begin{aligned} & \text { CH3-CHB3 } \\ & \text { VOD } \end{aligned}$ | 7 | Short Circuit Protection | R/W | 0xAD | 1: Enable the short circuit protection <br> 0: Disable the short circuit protection |
|  |  | 6 | RATE_SEL |  |  | 1: Gen $1 / 2$, <br> 0 : Gen 3 <br> Note: override the RATE pin. |
|  |  | 5:3 | Reserved |  |  | Set bits to default value - 101. |
|  |  | 2:0 | VOD Control |  |  | OB0 VOD Control 000: 0.7 V $001: 0.8 \mathrm{~V}$ $010: 0.9 \mathrm{~V}$ $011: 1.0 \mathrm{~V}$ 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V |


| 0x26 | $\begin{aligned} & \text { CH3 - CHB3 } \\ & \text { DEM } \end{aligned}$ | 7 | RXDET STATUS | R | 0x02 | Observation bit for RXDET CH3-CHB3. <br> 1: $\mathrm{RX}=$ detected <br> 0: RX = not detected |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 6:5 | RATE_DET STATUS | R |  | ```Observation bit for RATE_DET CH3 - CHB3. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G)``` |
|  |  | 4:3 | Reserved | R/W |  | Set bits to 0 . |
|  |  | 2:0 | DEM Control | R/W |  | OB3 DEM Control $000: 0 \mathrm{~dB}$ $001:-1.5 \mathrm{~dB}$ $010:-3.5 \mathrm{~dB}$ (default) $011:-5 \mathrm{~dB}$ 100: -6 dB 101: -8 dB $110:-9 \mathrm{~dB}$ $111:-12 \mathrm{~dB}$ |
| 0x27 | $\begin{aligned} & \hline \text { CH3 - CHB3 } \\ & \text { IDLE Threshold } \end{aligned}$ | 7:4 | Reserved | R/W | 0x00 | Set bits to 0 . |
|  |  | 3:2 | IDLE thd |  |  | $\begin{aligned} & \text { De-assert threshold } \\ & 00=110 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=100 \mathrm{mVp}-\mathrm{p} \\ & 10=150 \mathrm{mVp}-\mathrm{p} \\ & 11=130 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
|  |  | 1:0 | IDLE tha |  |  | Assert threshold $\begin{aligned} & 00=180 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=160 \mathrm{mVp}-\mathrm{p} \\ & 10=210 \mathrm{mVp}-\mathrm{p} \\ & 11=190 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
| 0x2B | CH4 - CHAO IDLE, RXDET | 7:6 | Reserved | R/W | 0x00 | Set bits to 0. |
|  |  | 5 | IDLE_AUTO |  |  | 1: Automatic IDLE detect 0 : Allow IDLE_SEL control in bit 4 Note: override IDLE control. |
|  |  | 4 | IDLE_SEL |  |  | 1: Output is MUTED (electrical idle) <br> 0 : Output is ON <br> Note: override IDLE control. |
|  |  | 3:2 | RXDET |  |  | 00: Input is high-z impedance <br> 01: Auto RX-Detect, outputs test every 12 ms for 600 ms ( 50 times) then stops; termination is high-z until detection; once detected input termination is $50 \Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is $50 \Omega$ <br> 11: Input is $50 \Omega$ <br> Note: override RXDET pin. |
|  |  | 1:0 | Reserved |  |  | Set bits to 0. |
| 0x2C | $\begin{aligned} & \mathrm{CH} 4-\mathrm{CHAO} \\ & \mathrm{EQ} \end{aligned}$ | 7:0 | EQ Control | R/W | 0x2F | IAO EQ Control - total of 256 levels. See Table 2: Equalizer Settings. |


| 0x2D | CH4-CHAO VOD |  | Short Circuit <br> Protection <br> RATE_SEL <br> Reserved <br> VOD Control | R/W | OxAD | 1: Enable the short circuit protection <br> 0: Disable the short circuit protection <br> 1: Gen $1 / 2$, <br> 0 : Gen 3 <br> Note: override the RATE pin. <br> Set bits to default value - 101 . <br> OAO VOD Control <br> 000: 0.7 V <br> 001: 0.8 V <br> 010: 0.9 V <br> 011: 1.0 V <br> 100: 1.1 V <br> 101: 1.2 V (default) <br> 110: 1.3 V <br> 111: 1.4 V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0x2E | $\begin{aligned} & \text { CH4 - CHAO } \\ & \text { DEM } \end{aligned}$ | 7 | RXDET STATUS | R | 0x02 | Observation bit for RXDET CH4 - CHAO. <br> 1: $\mathrm{RX}=$ detected <br> $0: R X=$ not detected |
|  |  | 6:5 | RATE_DET STATUS | R |  | ```Observation bit for RATE_DET CH4 - CHAO. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G)``` |
|  |  | 4:3 | Reserved | R/W |  | Set bits to 0 . |
|  |  | 2:0 | DEM Control | R/W |  | ```OAO DEM Control 000: 0 dB 001: -1.5 dB 010: -3.5 dB (default) 011: -5 dB 100: -6 dB 101:-8 dB 110: -9 dB 111: -12 dB``` |
| 0x2F | CH4-CHAO <br> IDLE Threshold | 7:4 | Reserved | R/W | 0x00 | Set bits to 0 . |
|  |  | 3:2 | IDLE thd |  |  | De-assert threshold $\begin{aligned} & 00=110 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=100 \mathrm{mVp}-\mathrm{p} \\ & 10=150 \mathrm{mVp}-\mathrm{p} \\ & 11=130 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
|  |  | 1:0 | IDLE tha |  |  | Assert threshold $\begin{aligned} & 00=180 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=160 \mathrm{mVp}-\mathrm{p} \\ & 10=210 \mathrm{mVp}-\mathrm{p} \\ & 11=190 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |


| $0 \times 32$ | CH5-CHA1 IDLE, RXDET | 7:6 | Reserved | R/W | $0 \times 00$ | Set bits to 0. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 5 | IDLE_AUTO |  |  | 1: Automatic IDLE detect 0 : Allow IDLE_SEL control in bit 4 Note: override IDLE control. |
|  |  | 4 | IDLE_SEL |  |  | 1: Output is MUTED (electrical idle) 0 : Output is ON <br> Note: override IDLE control. |
|  |  | 3:2 | RXDET |  |  | 00: Input is high-z impedance <br> 01: Auto RX-Detect, outputs test every 12 ms for 600 ms ( 50 times) then stops; termination is high-z until detection; once detected input termination is $50 \Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is $50 \Omega$ <br> 11: Input is $50 \Omega$ <br> Note: override RXDET pin. |
|  |  | 1:0 | Reserved |  |  | Set bits to 0 . |
| $0 \times 33$ | $\begin{aligned} & \text { CH5-CHA1 } \\ & \text { EQ } \end{aligned}$ | 7:0 | EQ Control | R/W | 0x2F | IA1 EQ Control - total of 256 levels. See Table 2: Equalizer Settings. |
| 0x34 | $\begin{aligned} & \text { CH5 - CHA1 } \\ & \text { VOD } \end{aligned}$ | 7 | Short Circuit Protection | R/W | 0xAD | 1: Enable the short circuit protection 0 : Disable the short circuit protection |
|  |  | 6 | RATE_SEL |  |  | $\begin{array}{\|l\|} \hline \text { 1: Gen } 1 / 2 \text {, } \\ \text { 0: Gen } 3 \\ \text { Note: override the RATE pin. } \\ \hline \end{array}$ |
|  |  | 5:3 | Reserved |  |  | Set bits to default value - 101. |
|  |  | 2:0 | VOD Control |  |  | OA1 VOD Control $000: 0.7 \mathrm{~V}$ $001: 0.8 \mathrm{~V}$ $010: 0.9 \mathrm{~V}$ 011: 1.0 V $100: 1.1 \mathrm{~V}$ $101: 1.2 \mathrm{~V}$ (default) $110: 1.3 \mathrm{~V}$ $111: 1.4 \mathrm{~V}$ |
| 0x35 | $\begin{aligned} & \text { CH5 - CHA1 } \\ & \text { DEM } \end{aligned}$ | 7 | RXDET STATUS | R | 0x02 | ```Observation bit for RXDET CH5 - CHA1. 1: RX = detected 0: RX = not detected``` |
|  |  | 6:5 | RATE_DET STATUS | R |  | ```Observation bit for RATE_DET CH5 - CHA1. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G)``` |
|  |  | 4:3 | Reserved | R/W |  | Set bits to 0 . |
|  |  | 2:0 | DEM Control | R/W |  | OA1 DEM Control $000: 0 \mathrm{~dB}$ 001: -1.5 dB $010:-3.5 \mathrm{~dB}$ (default) $011:-5 \mathrm{~dB}$ $100:-6 \mathrm{~dB}$ $101:-8 \mathrm{~dB}$ $110:-9 \mathrm{~dB}$ $111:-12 \mathrm{~dB}$ |


| $0 \times 36$ | CH5-CHA1 IDLE Threshold | 7:4 | Reserved | R/W | 0x00 | Set bits to 0 . |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 3:2 | IDLE thd |  |  | De-assert threshold $\begin{aligned} & 00=110 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=100 \mathrm{mVp}-\mathrm{p} \\ & 10=150 \mathrm{mVp}-\mathrm{p} \\ & 11=130 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
|  |  | 1:0 | IDLE tha |  |  | Assert threshold $\begin{aligned} & 00=180 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=160 \mathrm{mVp}-\mathrm{p} \\ & 10=210 \mathrm{mVp}-\mathrm{p} \\ & 11=190 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
| 0x39 | CH6 - CHA2 IDLE, RXDET | 7:6 | Reserved | R/W | 0x00 | Set bits to 0 . |
|  |  | 5 | IDLE_AUTO |  |  | 1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. |
|  |  | 4 | IDLE_SEL |  |  | 1: Output is MUTED (electrical idle) <br> 0 : Output is ON <br> Note: override IDLE control. |
|  |  | 3:2 | RXDET |  |  | 00: Input is high-z impedance <br> 01: Auto RX-Detect, outputs test every 12 ms for 600 ms ( 50 times) then stops; termination is high-z until detection; once detected input termination is $50 \Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is $50 \Omega$ <br> 11: Input is $50 \Omega$ <br> Note: override RXDET pin. |
|  |  | 1:0 | Reserved |  |  | Set bits to 0 . |
| 0x3A | $\begin{aligned} & \mathrm{CH} 6-\mathrm{CHA} 2 \\ & \mathrm{EQ} \end{aligned}$ | 7:0 | EQ Control | R/W | 0x2F | IA2 EQ Control - total of 256 levels. See Table 2: Equalizer Settings. |
| 0x3B | $\begin{aligned} & \text { CH6 - CHA2 } \\ & \text { VOD } \end{aligned}$ | 7 | Short Circuit Protection | R/W | 0xAD | 1: Enable the short circuit protection 0: Disable the short circuit protection |
|  |  | 6 | RATE_SEL |  |  | 1: Gen $1 / 2$, <br> 0 : Gen 3 <br> Note: override the RATE pin. |
|  |  | 5:3 | Reserved |  |  | Set bits to default value - 101. |
|  |  | 2:0 | VOD Control |  |  | ```OA2 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V``` |


| 0x3C | $\begin{aligned} & \text { CH6 - CHA2 } \\ & \text { DEM } \end{aligned}$ | 7 | RXDET STATUS | R | 0x02 | Observation bit for RXDET CH6 - CHA2. <br> 1: $\mathrm{RX}=$ detected <br> 0: RX = not detected |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 6:5 | $\begin{aligned} & \text { RATE_DET } \\ & \text { STATUS } \end{aligned}$ | R |  | Observation bit for RATE_DET CH6 - CHA2. <br> 00: GEN1 (2.5G) <br> 01: GEN2 (5G) <br> 11: GEN3 (8G) |
|  |  | 4:3 | Reserved | R/W |  | Set bits to 0 . |
|  |  | 2:0 | DEM Control | R/W |  | OA2 DEM Control $000: 0 \mathrm{~dB}$ $001:-1.5 \mathrm{~dB}$ $010:-3.5 \mathrm{~dB}$ (default) $011:-5 \mathrm{~dB}$ $100:-6 \mathrm{~dB}$ $101:-8 \mathrm{~dB}$ $110:-9 \mathrm{~dB}$ $111:-12 \mathrm{~dB}$ |
| 0x3D | CH6 - CHA2 IDLE Threshold | 7:4 | Reserved | R/W | 0x00 | Set bits to 0 . |
|  |  | 3:2 | IDLE thd |  |  | De-assert threshold $\begin{aligned} & 00=110 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=100 \mathrm{mVp}-\mathrm{p} \\ & 10=150 \mathrm{mVp}-\mathrm{p} \\ & 11=130 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
|  |  | 1:0 | IDLE tha |  |  | Assert threshold $\begin{aligned} & 00=180 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=160 \mathrm{mVp}-\mathrm{p} \\ & 10=210 \mathrm{mVp}-\mathrm{p} \\ & 11=190 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
| 0x40 | CH7-CHA3 <br> IDLE, RXDET | 7:6 | Reserved | R/W | 0x00 | Set bits to 0 . |
|  |  | 5 | IDLE_AUTO |  |  | 1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control. |
|  |  | 4 | IDLE_SEL |  |  | 1: Output is MUTED (electrical idle) 0 : Output is ON Note: override IDLE control. |
|  |  | 3:2 | RXDET |  |  | 00: Input is high-z impedance <br> 01: Auto RX-Detect, outputs test every 12 ms for 600 ms ( 50 times) then stops; termination is high-z until detection; once detected input termination is $50 \Omega$ 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is $50 \Omega$ <br> 11: Input is $50 \Omega$ <br> Note: override RXDET pin. |
|  |  | 1:0 | Reserved |  |  | Set bits to 0 . |
| 0x41 | $\begin{aligned} & \mathrm{CH} 7-\mathrm{CHA} \\ & \mathrm{EQ} \end{aligned}$ | 7:0 | EQ Control | R/W | 0x2F | IA3 EQ Control - total of 256 levels. See Table 2: Equalizer Settings. |


| 0x42 | $\mathrm{CH} 7-\mathrm{CHA}$ <br> VOD | 7 | Short Circuit Protection | R/W | OxAD | 1: Enable the short circuit protection 0. Disable the short circuit protection |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 6 | RATE_SEL |  |  | 1: Gen $1 / 2$, <br> 0 : Gen 3 <br> Note: override the RATE pin. |
|  |  | 5:3 | Reserved |  |  | Set bits to default value - 101. |
|  |  | 2:0 | VOD Control |  |  | OA3 VOD Control <br> 000: 0.7 V <br> 001: 0.8 V <br> 010: 0.9 V <br> 011: 1.0 V <br> 100: 1.1 V <br> 101: 1.2 V (default) <br> 110: 1.3 V <br> 111: 1.4 V |
| $0 \times 43$ | $\mathrm{CH} 7-\mathrm{CHA} 3$ <br> DEM | 7 | RXDET STATUS | R | 0x02 | Observation bit for RXDET CH7-CHA3. <br> 1: RX = detected <br> $0: R X=$ not detected |
|  |  | 6:5 | RATE_DET STATUS | R |  | ```Observation bit for RATE_DET CH7-CHA3. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G)``` |
|  |  | 4:3 | Reserved | R/W |  | Set bits to 0 . |
|  |  | 2:0 | DEM Control | R/W |  | ```OA3 DEM Control 000: 0 dB 001: -1.5 dB 010: -3.5 dB (default) 011: -5 dB 100: -6 dB 101: -8 dB 110: -9 dB 111: -12 dB``` |
| 0x44 | CH7-CHA3 IDLE Threshold | 7:4 | Reserved | R/W | 0x00 | Set bits to 0 . |
|  |  | 3:2 | IDLE thd |  |  | De-assert threshold $\begin{aligned} & 00=110 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=100 \mathrm{mVp}-\mathrm{p} \\ & 10=150 \mathrm{mVp}-\mathrm{p} \\ & 11=130 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
|  |  | 1:0 | IDLE tha |  |  | Assert threshold $\begin{aligned} & 00=180 \mathrm{mVp}-\mathrm{p} \text { (default) } \\ & 01=160 \mathrm{mVp}-\mathrm{p} \\ & 10=210 \mathrm{mVp}-\mathrm{p} \\ & 11=190 \mathrm{mVp}-\mathrm{p} \end{aligned}$ <br> Note: override the SD_TH pin. |
| 0x51 | Device ID | 7:5 | VERSION | R | 0x44 | 010'b |
|  |  | 4:0 | ID |  |  | 00100'b |

## Applications Information

The DS80PCI402 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the information below and Revision 4 of the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

## PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and LPDS outputs have been optimized to work with interconnects using a controlled differential
impedance of 85-100 . It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187 for additional information on LLP packages.


FIGURE 6. Typical Routing Options

The graphic shown above depicts different transmission line topologies which can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each hole and providing for a low inductance return current path. When the via structure is associated with thick backplane PCB, further optimization such as back drilling is often used to reduce the deterimential high frequency effects of stubs on the signal path.

## POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS80PCI402 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be
connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the $\mathrm{V}_{\mathrm{DD}}$ and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A $0.1 \mu \mathrm{~F}$ bypass capacitor should be connected to each $\mathrm{V}_{\mathrm{DD}}$ pin such that the capacitor is placed as close as possible to the DS80PCI402. Smaller body size capacitors can help facilitate proper component placement. Additionally, capacitor with capacitance in the range of $1 \mu \mathrm{~F}$ to $10 \mu \mathrm{~F}$ should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

## Typical Performance Curves Characteristics



FIGURE 7. Power Dissipation (PD) vs. Output Differential Voltage (VOD)


30119828
FIGURE 8. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Supply Voltage (VDD)


30119829
FIGURE 9. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Temperature

## Typical Performance Eye Diagrams Characteristics



FIGURE 10. Test Setup Connections Diagram


FIGURE 11. TL = 20 inch 4-mil FR4 trace, DS80PCI402 settings: $E Q[1: 0]=R, R=15 ' h, D E M[1: 0]=$ float, float


30119832
FIGURE 12. TL = 35 inch 4-mil FR4 trace, DS80PCI402 settings: EQ[1:0] = float, $R=1 F^{\prime} h$, DEM[1:0] = float, float


FIGURE 13. Test Setup Connections Diagram


30119834
FIGURE 14. TL1 = 20 inch 4-mil FR4 trace, TL2 = $\mathbf{1 5}$ inch 4-mil FR4 trace, DS80PCI402 settings: $E Q[1: 0]=R, R=15 ' h, D E M[1: 0]=$ float, float


30119835
FIGURE 15. TL1 = $\mathbf{3 0}$ inch 4-mil FR4 trace, TL2 = $\mathbf{1 5}$ inch 4-mil FR4 trace, DS80PCI402 settings: $E Q[1: 0]=R, 1=0 F ' h, D E M[1: 0]=$ float, float

Physical Dimensions inches (millimeters) unless otherwise noted



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