Texas Instruments Dual EVM BoC Card - Quick Start Guide

High Density Multiprocessor DSP's

Abstract

This document is provided as a quick start guide for using the Texas Instruments BoC (Break out Card). The breakout card is intended to provide communication support between Texas Instruments EVM's which contain an AMC B+ interface. The EVM BoC is intended to support EVM to EVM communication for SRIO, PCIe, SGMII, and AIF.

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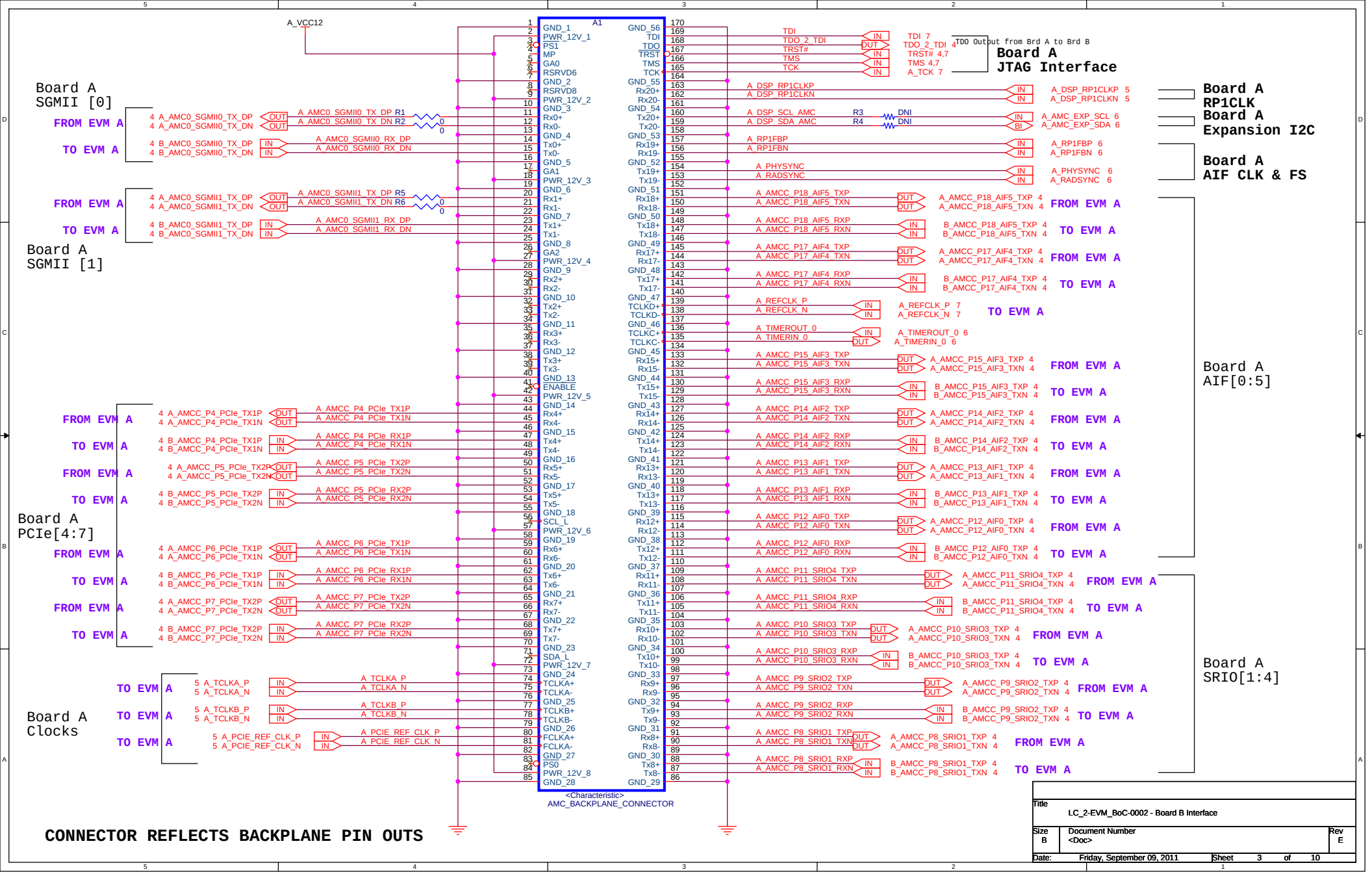
A_VCC12
A1
GND_1 PWR_12V_1 PS1 MP GA0 RSRVD6 GND_2 RSRVD8 PWR_12V_2 GND_3 Rx0+ Rx0- GND_4 Tx0+ Tx0- GND_5 GA1 PWR_12V_3 GND_6 Rx1+ Rx1- GND_7 Tx1+ Tx1- GND_8 GA2 PWR_12V_4 GND_9 Rx2+ Rx2- GND_10 Tx2+ Tx2- GND_11 Rx3+ Rx3- GND_12 Tx3+ Tx3- GND_13 ENABLE PWR_12V_5 GND_14 Rx4+ Rx4- GND_15 Tx4+ Tx4- GND_16 Rx5+ Rx5- GND_17 Tx5+ Tx5- GND_18 SCL_L PWR_12V_6 GND_19 Rx6+ Rx6- GND_20 Tx6+ Tx6- GND_21 Rx7+ Rx7- GND_22 Tx7+ Tx7- GND_23 SDA_L PWR_12V_7 GND_24 TCLKA+ TCLKA- GND_25 TCLKB+ TCLKB- GND_26 FCLKA+ FCLKA- GND_27 PS0 PWR_12V_8 GND_28
GND_56 TDI TDO TRST TMS TCK GND_55 Rx20+ Rx20- GND_54 Tx20+ Tx20- GND_53 Rx19+ Rx19- GND_52 Tx19+ Tx19- GND_51 Rx18+ Rx18- GND_50 Tx18+ Tx18- GND_49 Rx17+ Rx17- GND_48 Tx17+ Tx17- GND_47 TCLKD+ TCLKD- GND_46 TCLKC+ TCLKC- GND_45 Rx15+ Rx15- GND_44 Tx15+ Tx15- GND_43 Rx14+ Rx14- GND_42 Tx14+ Tx14- GND_41 Rx13+ Rx13- GND_40 Tx13+ Tx13- GND_39 Rx12+ Rx12- GND_38 Tx12+ Tx12- GND_37 Rx11+ Rx11- GND_36 Tx11+ Tx11- GND_35 Rx10+ Rx10- GND_34 Tx10+ Tx10- GND_33 Rx9+ Rx9- GND_32 Tx9+ Tx9- GND_31 Rx8+ Rx8- GND_30 Tx8+ Tx8- GND_29
<Characteristic>
AMC_BACKPLANE_CONNECTOR
Board A SGMII [0]
FROM EVM A
TO EVM A
A_AMC0_SGMII0_TX_DP
A_AMC0_SGMII0_TX_DN
A_AMC0_SGMII0_TX_DP R1
A_AMC0_SGMII0_TX_DN R2
A_AMC0_SGMII0_RX_DP
A_AMC0_SGMII0_RX_DN
Board A SGMII [1]
A_AMC0_SGMII1_TX_DP
A_AMC0_SGMII1_TX_DN
A_AMC0_SGMII1_TX_DP R5
A_AMC0_SGMII1_TX_DN R6
A_AMC0_SGMII1_RX_DP
A_AMC0_SGMII1_RX_DN
Board A PCIe[4:7]
A_AMCC_P4_PCIe_TX1P
A_AMCC_P4_PCIe_TX1N
A_AMCC_P4_PCIe_RX1P
A_AMCC_P4_PCIe_RX1N
A_AMCC_P5_PCIe_TX2P
A_AMCC_P5_PCIe_TX2N
A_AMCC_P5_PCIe_RX2P
A_AMCC_P5_PCIe_RX2N
A_AMCC_P6_PCIe_TX1P
A_AMCC_P6_PCIe_TX1N
A_AMCC_P6_PCIe_RX1P
A_AMCC_P6_PCIe_RX1N
A_AMCC_P7_PCIe_TX2P
A_AMCC_P7_PCIe_TX2N
A_AMCC_P7_PCIe_RX2P
A_AMCC_P7_PCIe_RX2N
Board A Clocks
A_TCLKA_P
A_TCLKA_N
A_TCLKB_P
A_TCLKB_N
A_PCIE_REF_CLK_P
A_PCIE_REF_CLK_N
TDI
TDO_2_TDI
TRST#
TMS
TCK
TDO Output from Brd A to Brd B
Board A JTAG Interface
A_DSP_RP1CLKP
A_DSP_RP1CLKN
Board A RP1CLK
A_DSP_SCL_AMC
A_DSP_SDA_AMC
R3 DNI
R4 DNI
Board A Expansion I2C
A_RP1FBP
A_RP1FBN
A_PHYSYNC
A_RADSYNC
Board A AIF CLK & FS
A_AMCC_P18_AIF5_TXP
A_AMCC_P18_AIF5_TXN
A_AMCC_P18_AIF5_RXP
A_AMCC_P18_AIF5_RXN
A_AMCC_P17_AIF4_TXP
A_AMCC_P17_AIF4_TXN
A_AMCC_P17_AIF4_RXP
A_AMCC_P17_AIF4_RXN
A_REFCLK_P
A_REFCLK_N
A_TIMEROUT_0
A_TIMERIN_0
A_AMCC_P15_AIF3_TXP
A_AMCC_P15_AIF3_TXN
A_AMCC_P15_AIF3_RXP
A_AMCC_P15_AIF3_RXN
A_AMCC_P14_AIF2_TXP
A_AMCC_P14_AIF2_TXN
A_AMCC_P14_AIF2_RXP
A_AMCC_P14_AIF2_RXN
A_AMCC_P13_AIF1_TXP
A_AMCC_P13_AIF1_TXN
A_AMCC_P13_AIF1_RXP
A_AMCC_P13_AIF1_RXN
A_AMCC_P12_AIF0_TXP
A_AMCC_P12_AIF0_TXN
A_AMCC_P12_AIF0_RXP
A_AMCC_P12_AIF0_RXN
Board A AIF[0:5]
A_AMCC_P11_SRIO4_TXP
A_AMCC_P11_SRIO4_TXN
A_AMCC_P11_SRIO4_RXP
A_AMCC_P11_SRIO4_RXN
A_AMCC_P10_SRIO3_TXP
A_AMCC_P10_SRIO3_TXN
A_AMCC_P10_SRIO3_RXP
A_AMCC_P10_SRIO3_RXN
A_AMCC_P9_SRIO2_TXP
A_AMCC_P9_SRIO2_TXN
A_AMCC_P9_SRIO2_RXP
A_AMCC_P9_SRIO2_RXN
A_AMCC_P8_SRIO1_TXP
A_AMCC_P8_SRIO1_TXN
A_AMCC_P8_SRIO1_RXP
A_AMCC_P8_SRIO1_RXN
Board A SRIO[1:4]
CONNECTOR REFLECTS BACKPLANE PIN OUTS
Title
LC_2-EVM_BoC-0002 - Board B Interface
Size B
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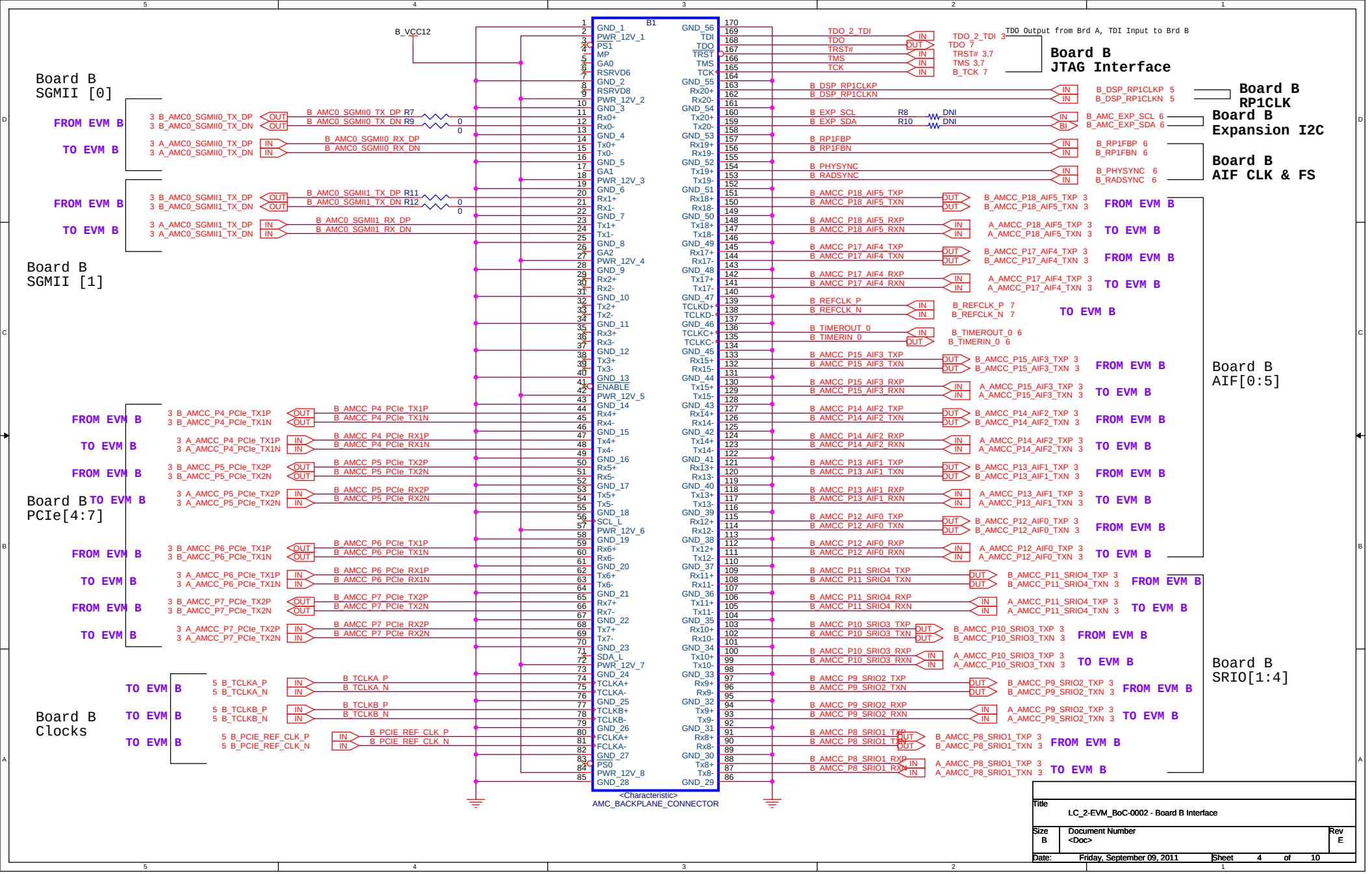
Board B SGMII [0]
FROM EVM B
TO EVM B
Board B SGMII [1]
Board B PCIe[4:7]
Board B Clocks
B_VCC12
B1
GND_1
PWR_12V_1
PS1
MP
GA0
RSRVD6
GND_2
RSRVD8
PWR_12V_2
GND_3
Rx0+
Rx0-
GND_4
Tx0+
Tx0-
GND_5
GA1
PWR_12V_3
GND_6
Rx1+
Rx1-
GND_7
Tx1+
Tx1-
GND_8
GA2
PWR_12V_4
GND_9
Rx2+
Rx2-
GND_10
Tx2+
Tx2-
GND_11
Rx3+
Rx3-
GND_12
Tx3+
Tx3-
GND_13
ENABLE
PWR_12V_5
GND_14
Rx4+
Rx4-
GND_15
Tx4+
Tx4-
GND_16
Rx5+
Rx5-
GND_17
Tx5+
Tx5-
GND_18
SCL_L
PWR_12V_6
GND_19
Rx6+
Rx6-
GND_20
Tx6+
Tx6-
GND_21
Rx7+
Rx7-
GND_22
Tx7+
Tx7-
GND_23
SDA_L
PWR_12V_7
GND_24
TCLKA+
TCLKA-
GND_25
TCLKB+
TCLKB-
GND_26
FCLKA+
FCLKA-
GND_27
PS0
PWR_12V_8
GND_28
GND_56
TDI
TDO
TRST
TMS
TCK
GND_55
Rx20+
Rx20-
GND_54
Tx20+
Tx20-
GND_53
Rx19+
Rx19-
GND_52
Tx19+
Tx19-
GND_51
Rx18+
Rx18-
GND_50
Tx18+
Tx18-
GND_49
Rx17+
Rx17-
GND_48
Tx17+
Tx17-
GND_47
TCLKD+
TCLKD-
GND_46
TCLKC+
TCLKC-
GND_45
Rx15+
Rx15-
GND_44
Tx15+
Tx15-
GND_43
Rx14+
Rx14-
GND_42
Tx14+
Tx14-
GND_41
Rx13+
Rx13-
GND_40
Tx13+
Tx13-
GND_39
Rx12+
Rx12-
GND_38
Tx12+
Tx12-
GND_37
Rx11+
Rx11-
GND_36
Tx11+
Tx11-
GND_35
Rx10+
Rx10-
GND_34
Tx10+
Tx10-
GND_33
Rx9+
Rx9-
GND_32
Tx9+
Tx9-
GND_31
Rx8+
Rx8-
GND_30
Tx8+
Tx8-
GND_29
<Characteristic>
AMC_BACKPLANE_CONNECTOR
B_AMC0_SGMII0_TX_DP R7
B_AMC0_SGMII0_TX_DN R9
B_AMC0_SGMII0_RX_DP
B_AMC0_SGMII0_RX_DN
B_AMC0_SGMII1_TX_DP R11
B_AMC0_SGMII1_TX_DN R12
B_AMC0_SGMII1_RX_DP
B_AMC0_SGMII1_RX_DN
B_AMC_P4_PCIe_TX1P
B_AMC_P4_PCIe_TX1N
B_AMC_P4_PCIe_RX1P
B_AMC_P4_PCIe_RX1N
B_AMC_P5_PCIe_TX2P
B_AMC_P5_PCIe_TX2N
B_AMC_P5_PCIe_RX2P
B_AMC_P5_PCIe_RX2N
B_AMC_P6_PCIe_TX1P
B_AMC_P6_PCIe_TX1N
B_AMC_P6_PCIe_RX1P
B_AMC_P6_PCIe_RX1N
B_AMC_P7_PCIe_TX2P
B_AMC_P7_PCIe_TX2N
B_AMC_P7_PCIe_RX2P
B_AMC_P7_PCIe_RX2N
B_TCLKA_P
B_TCLKA_N
B_TCLKB_P
B_TCLKB_N
B_PCIE_REF_CLK_P
B_PCIE_REF_CLK_N
TDO Output from Brd A, TDI Input to Brd B
Board B JTAG Interface
TDO_2_TDI
TDO
TRST#
TMS
TCK
TDO_7
TRST# 3,7
TMS 3,7
B_TCK_7
Board B RP1CLK
B_DSP_RP1CLKP
B_DSP_RP1CLKN
Board B Expansion I2C
B_EXP_SCL
B_EXP_SDA
R8
R10
DNI
B_AMC_EXP_SCL 6
B_AMC_EXP_SDA 6
Board B AIF CLK & FS
B_RP1FBP
B_RP1FBN
B_PHYSYNC
B_RADSYNC
Board B AIF[0:5]
B_AMCC_P18_AIF5_TXP
B_AMCC_P18_AIF5_TXN
B_AMCC_P18_AIF5_RXP
B_AMCC_P18_AIF5_RXN
B_AMCC_P17_AIF4_TXP
B_AMCC_P17_AIF4_TXN
B_AMCC_P17_AIF4_RXP
B_AMCC_P17_AIF4_RXN
B_REFCLK_P
B_REFCLK_N
B_TIMEROUT_0
B_TIMERIN_0
B_AMCC_P15_AIF3_TXP
B_AMCC_P15_AIF3_TXN
B_AMCC_P15_AIF3_RXP
B_AMCC_P15_AIF3_RXN
B_AMCC_P14_AIF2_TXP
B_AMCC_P14_AIF2_TXN
B_AMCC_P14_AIF2_RXP
B_AMCC_P14_AIF2_RXN
B_AMCC_P13_AIF1_TXP
B_AMCC_P13_AIF1_TXN
B_AMCC_P13_AIF1_RXP
B_AMCC_P13_AIF1_RXN
B_AMCC_P12_AIF0_TXP
B_AMCC_P12_AIF0_TXN
B_AMCC_P12_AIF0_RXP
B_AMCC_P12_AIF0_RXN
Board B SRIO[1:4]
B_AMCC_P11_SRIO4_TXP
B_AMCC_P11_SRIO4_TXN
B_AMCC_P11_SRIO4_RXP
B_AMCC_P11_SRIO4_RXN
B_AMCC_P10_SRIO3_TXP
B_AMCC_P10_SRIO3_TXN
B_AMCC_P10_SRIO3_RXP
B_AMCC_P10_SRIO3_RXN
B_AMCC_P9_SRIO2_TXP
B_AMCC_P9_SRIO2_TXN
B_AMCC_P9_SRIO2_RXP
B_AMCC_P9_SRIO2_RXN
B_AMCC_P8_SRIO1_TXP
B_AMCC_P8_SRIO1_TXN
B_AMCC_P8_SRIO1_RXP
B_AMCC_P8_SRIO1_RXN
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CLOCK INTERFACE

FULL SILK SCREENING REQUIRED

NOTE: PLACE OSCILLATOR WITH NO STUBS
-U2 is a 30.72MHz Oscillator p/n FXO-LC735R-30.72
-By default leave Disabled
-Oscillator only installed on limited board
-RPICLKP/N nets to be matched length from "T"
-R15:18, 20:23, & 25:28 must be placed close to output

**U1 Output is LVPECL
Resistors R20:R23
have been configured
for CML output (mod for LVDS swing)**

**RP1CLK SMT SMA
--Leave room for wrench--
-must be skew matched between SMA's and U10 input
-NO STUBS**

Zero stub between CON1/CON2
SMA and U2/U1 OScillator input,
Nets must be identical length

JP1 Default Settings
-Install shunt between 1-2
-Oscillator output is Hi-Z

**R24 & R29 are 0 ohm 0402 resistors,
May need to be changed to 0.01uF
Capacitors to AC couple**

**R35 MUST be
placed close
to input pins
of U6**

R30 must be across pins of U1

JP2 Default Settings
-Install shunt
-Oscillator output is Hi-Z

**U6 Output is LVPECL
Resistors R42:R45
have been configured
for CML output**

**R36 & R41 are 0 ohm 0402
resistors, May need to be
changed to 0.01uF
Capacitors to AC couple**

Board B Clocks

Board A Clocks

Zero stub between CON5/CON4
SMA and U8/U7 Crystal input,
Nets must be identical length
-U7 configured for 100MHz output
U8 is a 25MHz xtal

**Common PCIe REFCLK
SMT SMA
-Leave room for wrench
-No stubs and all "T's"
must be balanced**

JP3 Default Settings
-Install shunt between 1-2
-Output is Hi-Z

NOTE: PLACE OSCILLATOR WITH NO STUBS
-U5 is a 30.72MHz Oscillator p/n FXO-LC735R-30.72
-By default leave Disabled
-RPICLKP/N nets to be matched length from "T"
-R37:40, & 42:49 must be placed close to output

Pay attention to mounting requirements for all clock sources

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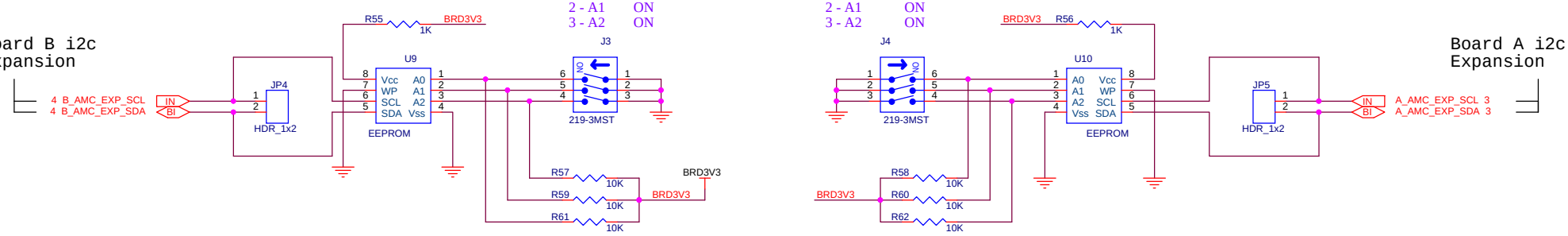
Board B i2c Expansion

J10 [ON = 0] DEFAULT
1 - A0 ON
2 - A1 ON
3 - A2 ON

J11 [ON = 0] DEFAULT
1 - A0 OFF
2 - A1 ON
3 - A2 ON

Board A i2c Expansion

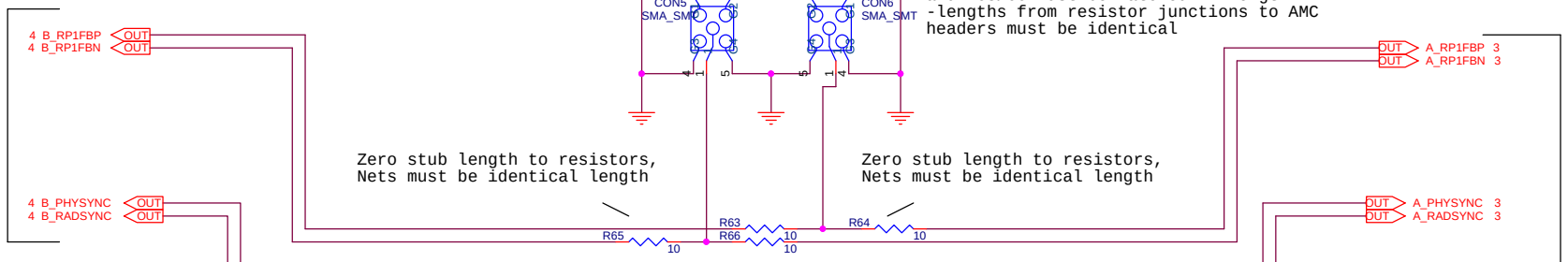


R73 &R32 are 0 ohm 0402 resistors,
May need to be changed to 0.01uF
Capacitors to AC couple

RP1FB / SMT SMA
--Leave room for wrench--

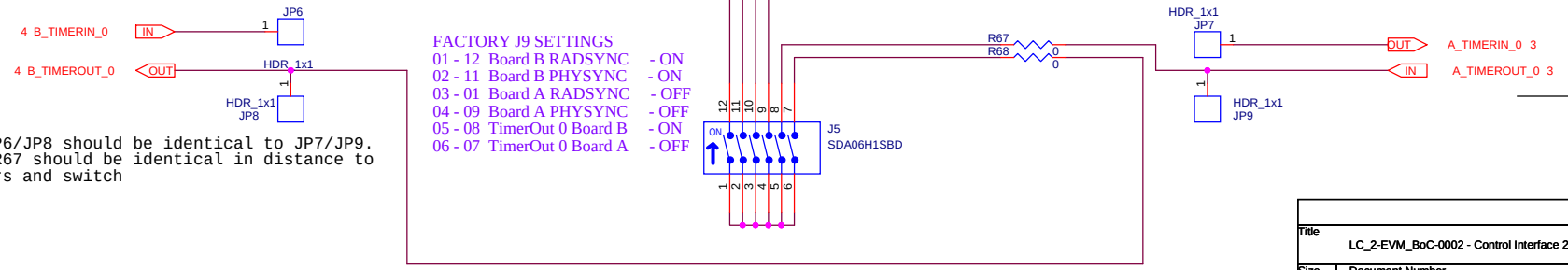
CON5 net connections to R63/64 and R65/66 must be matched in length -lengths from resistor junctions to AMC headers must be identical

Board B AIF CLK & FS



Zero stub length to resistors, Nets must be identical length

Zero stub length to resistors, Nets must be identical length



FACTORY J9 SETTINGS
01 - 12 Board B RADSYNC - ON
02 - 11 Board B PHYSYNC - ON
03 - 01 Board A RADSYNC - OFF
04 - 09 Board A PHYSYNC - OFF
05 - 08 TimerOut 0 Board B - ON
06 - 07 TimerOut 0 Board A - OFF

Board A AIF CLK & FS

Placement of JP6/JP8 should be identical to JP7/JP9.
-Placement of R67 should be identical in distance to R68 from Headers and switch

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POWER SUPPLY

REG1117-3.3 (0.8A)

U12 Output is LVPECL Resistors R71:R75 & R77:R83 have been configured for CML output.
-Resistors will need to be changed to accommodate a different swing.
-All resistors to go close to U12

BJ_MH1 & BJ_MH2
-Mounting hole to support Pamona 2142-2 (Red Banana Jack, Through hole)

J6 Default 1:2
0.100" Header
1 shunt needed

U13, C18:C19 MUST be placed close to U3

J5 Default is Not Installed
0 = Power Down (Hi-Z)
1 = Normal (Active Output)

0.100" Header
1 shunt needed

R84 must be across pins of U12

R85:R86 are 0 ohm 0402 resistors, May need to be changed to 0.01uF Capacitors to AC couple

BJ_MH3
-Mounting hole to support Pamona 2142-0 (Black Banana Jack, Through hole)

Board A & B Daisy Chain JTAG Interface

NOTE: Interface is 3.3V and requires 3.3V level translation prior to interface with DSP. This is done to comply with the current AMC specification

NOTE: Mounting holes are plated through, after plating, holes must support 6/32 mounting hardware and standoffs

TDI from Emulator to DSP
TDO from DSP to Emulator

TVD Target Power Supply for IO's

TCKRTn total length to match TCK routing on EVM's (No stubs allowed, resistor connection should be as close to header pin as possible.

EMULATION INTERFACE

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I. OVERVIEW

I. Introduction

The CI2EVM_BoC dual evm interface card is a high performance inter-communication card designed to provide DSP to DSP communication during software testing and analysis.

II. Hardware Description

The following illustrates the major components and areas of the CI2EVM_BoC breakout card.

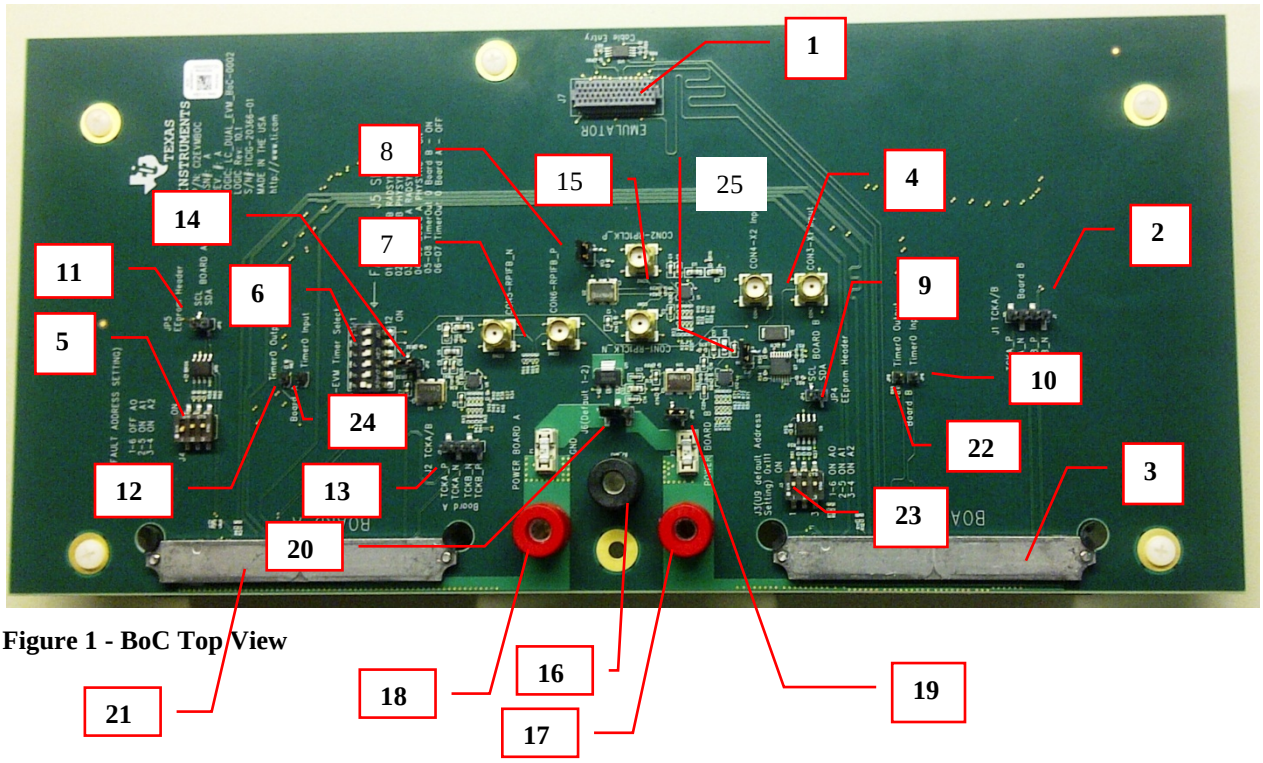


Figure 1 - BoC Top View

1) Emulation Interface – J7
2) Board B TCKA/B Header – J1
3) Board B AMC B+ EVM Interface Connector
4) Auxilluary PCIe Clock Input SMA Connectors - CON3/CON4
5) Board A EEPROM Address Configuration Switch - J4
6) Timer Sync Configuration Switch - J5
7) Auxilluary RP1FB Clock Input SMA Connectors - CON5/CON6
8) RP1CLK Source Input Clock Oscillator Enable Control – JP1
9) Board B I2C EEPROM Programming Header – JP4
10) Board B Timer0 Input Interface Header – JP6
11) Board A I2C EEPROM Programming Header – JP5
12) Board A Timer0 Output Interface Header – JP9
13) Board A TCKA/B Header – J2

14) A_TCLKB & B_TCKB Source Input Clock Oscillator Enable Control – JP2
15) Auxilluary RP1CLK Clock Input SMA Connectors – CON1/CON2
16) Common Ground Banana Jack – BJ-MH3
17) Board B Power Banana Jack – BJ-MH2
18) Board A Power Banana Jack – BJ-MH1
19) Board A & B REFCLK Source Input Clock Oscillator Enable Control – JP10
20) Primary BoC Power Selection Switch – J6
21) Board A AMC B+ EVM Interface Connector
22) Board B Timer0 Output Interface Header – JP8
23) Board B EEPROM Address Configuration Switch – J3
24) Board A Timer0 Input Interface Header – JP7
25) Board A & B PCIECLK Source Input Clock Oscillator Enable Control - JP3

The following illustration is of the assembled BoC card for reference purposes:

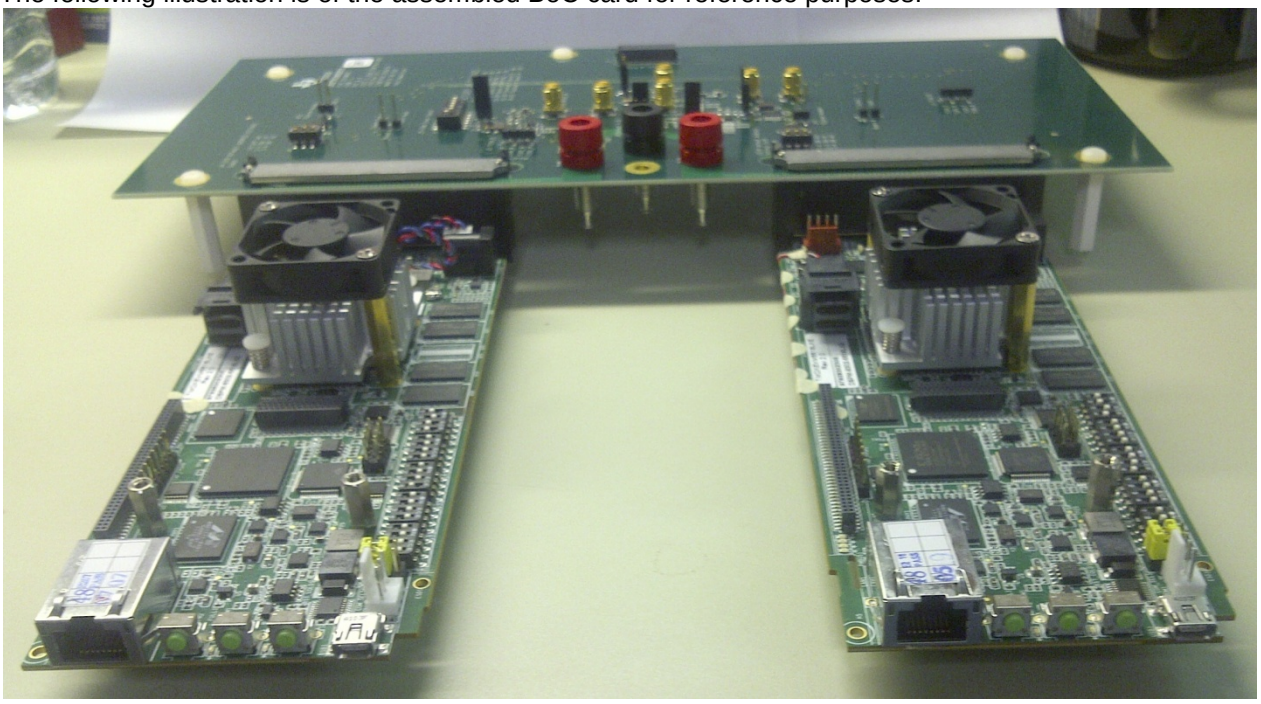


Figure 2: Front View, Assembled BoC

The following is a high level block diagram denoting the connectivity and functionality of the dual EVM BoC card.

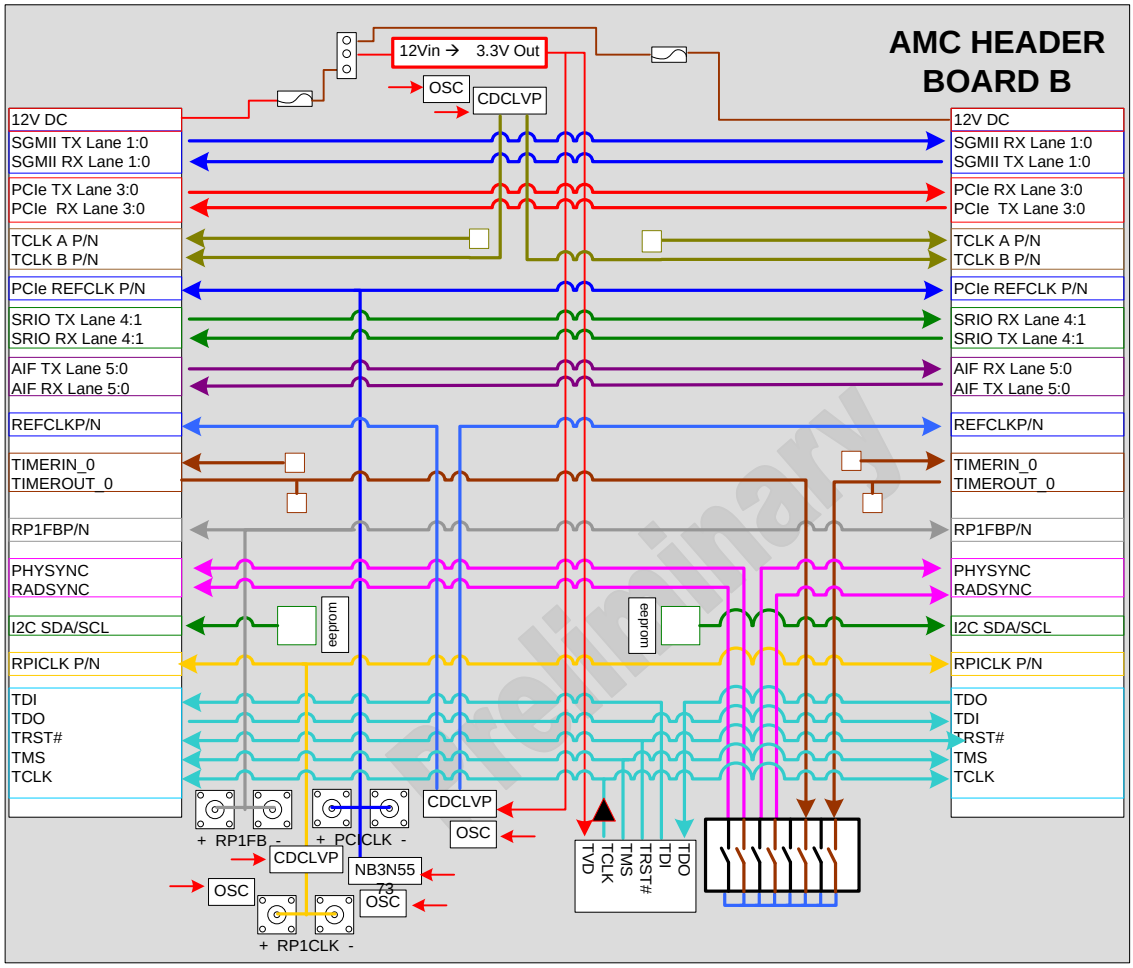


Figure 3 - Block Diagram

II. Hardware Configuration

I. Initial Installation Procedure

The following instructions define the basic minimum installation requirements for your BoC (Break out Card).

II. Default Jumper and Pin Settings

The following table defines the factory default configuration settings your BoC has been shipped with.

Table 1: Factory Configuration

Reference	Item	Description	Factory Setting
J1	2	1X4 Header	N/A
J2	13	1X4 Header	N/A
J3	23	Switch	0x111
J4	5	Switch	0x011
J5	6	Switch	0x111110
J6	20	1X3 Header	Shunt Installed [1-2]
JP1	8	1X2 Header	Shunt Installed
JP2	14	1X2 Header	Shunt Installed
JP3	25	1X2 Header	Shunt Installed
JP4	9	1X2 Header	N/A
JP5	11	1X2 Header	N/A
JP6	10	1X1 Header	N/A
JP7	24	1X1 Header	N/A
JP8	22	1X1 Header	N/A
JP9	12	1X1 Header	N/A
JP10	19	1X2 Header	Shunt Installed

III. BoC Logic Power Source Selection [20]

The BoC on board logic is capable of sourcing power from either of the EVM's (provided the EVM's are independently powered. Header J6 allows the user to select the 12V input power to the BoC on board logic. The following figure illustrates the possible configurations.

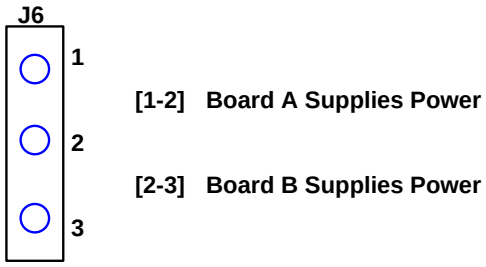


Figure 4 - BoC Logic Power Source Selection

The following figure illustrates the basic power supply logic implemented on your BoC.

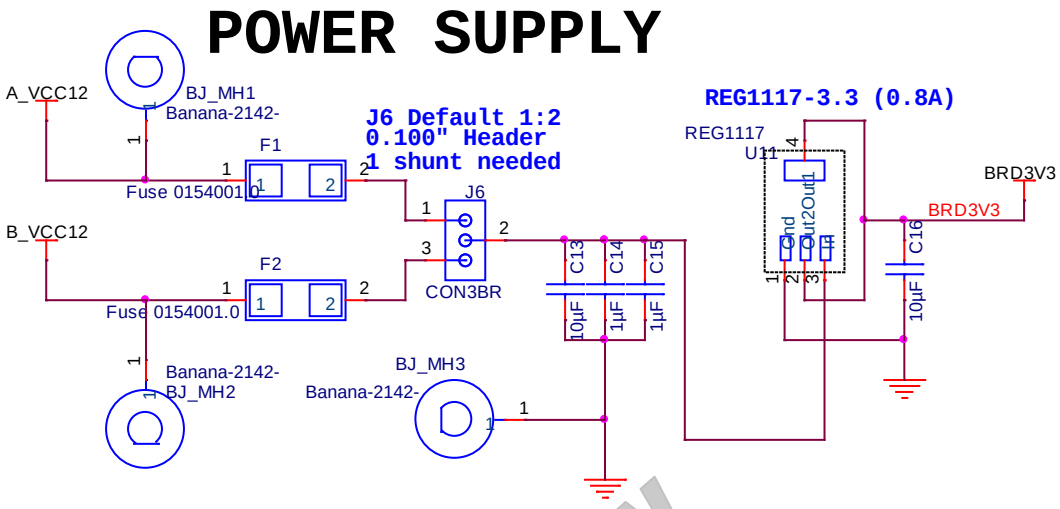


Figure 5: BoC Power Supply

IV. EVM Power Source [16, 17, 18]

Traditionally the EVM's installed into the Boc will have there own power supplies. There may be on occasion where a user needs to power both boards from the same power source. The BoC contains three mounting holes (for banana jacks) that when installed can be used to power the EVM's installed.

CAUTION: If you elect to power your EVM's through the BoC card, you MUST not use power supplies connected to your EVM's input power.

WARNING: If you elect to power your EVM's in this method, your EVM power requirements must not exceed the maximum power allowed by the design.

EVM's vary in total board power requirements. The power rating based on the current designed layout of your BoC card will accommodate up to 8 amperes per board.

The recommended banana jacks to be installed are manufactured by Pomona®, part numbers:

- 1581-2 (Red, 2 required) **[17 & 18]**
- 1581-0 (Black, 1 required) **[16]**

The mounting pads on the BoC are electrically conductive. Due to the height limitations and the need to clear any supporting surface, the bottom insulated ring must be placed on the top side of the PCB and the star washer and nut assembled from the bottom.

V. Emulation Interface [1]

Your BoC contains a traditional Texas Instruments 60-pin emulation header (item 1). It should be noted that emulation voltages across the AMCC backplane are intended for 3.3Vdc. Your BoC has been designed so that the emulation interface is also 3.3V, before using this interface it will be necessary to confirm that your EVM's can accommodate a 3.3V logic level without damage occurring.

WARNING: The Emulation Interface is intended to operate at 3.3V, Confirm that your EVM level shifts this into to correct DSP range before using this interface

The emulation interface of you BoC is daisy-chained. This means that the test data in and test data out pins are configured such that both boards are in the scan chan at all times. If you require separate control, use separate emulators directly connected to each respective EVM.

VI. SGMII Interface

Your BoC in designed to support two (2) lanes of SGMII. The SGMII interface is connected between each board (A & B) in a manner that provides intercommunication. Board A transmit (TX) lanes 1:0 are routed to the receive (RX) lanes 1:0 of Board B, and Board A receive (RX) lanes 1:0 are routed to the transmit (TX) lanes 1:0 of Board B. There are no AC coupling capacitors on your BoC, it is assume that your EVM hardware has been properly designed and contains the appropriate AC coupling capacitors on the respective AC nets.

CAUTION: Confirm that your EVM supports this interface and that the number of interfaces as well as the pinout locations is supported correctly.

VII. PCIE Interface

Your BoC in designed to support four (4) lanes of PCIe. The PCIe interface is connected between each board (A & B) in a manner that provides intercommunication. Board A transmit (TX) lanes 7:4 are routed to the receive (RX) lanes 7:4 of Board B, and Board A receive (RX) lanes 7:4 are routed to the transmit (TX) lanes 7:4 of Board B. There are no AC coupling capacitors on your BoC, it is assume that your EVM hardware has been properly designed and contains the appropriate AC coupling capacitors on the respective AC nets.

In some cases a common or alternate PCIe clock may be required, where needed the BoC has the ability to provide a common PCIe REFCLK, refer to section XVI for details and configuration options.

CAUTION: Confirm that your EVM supports this interface and that the number of interfaces as well as the pinout locations is supported correctly.

VIII. SRIO (Serial RapidIO) Interface

Your BoC in designed to support four (4) lanes of SRIO. The SRIO interface is connected between each board (A & B) in a manner that provides intercommunication. Board A transmit (TX) lanes 11:8 are routed to the receive (RX) lanes 11:8 of Board B, and Board A receive (RX) lanes 11:8 are routed to the transmit (TX) lanes 11:8 of Board B. There are no AC coupling capacitors on your BoC, it is assume that your EVM hardware has been properly designed and contains the appropriate AC coupling capacitors on the respective AC nets.

CAUTION: Confirm that your EVM supports this interface and that the number of interfaces as well as the pinout locations is supported correctly.

IX. AIF (Antenna Interface) Interface

Your BoC in designed to support six (6) lanes of AIF. The AIF interface is connected between each board (A & B) in a manner that provides intercommunication. Board A transmit (TX) lanes 18:17 & 15:12 are routed to the receive (RX) lanes 18:17 & 15:12 of Board B, and Board A receive (RX) lanes 18:17 & 15:12 are routed to the transmit (TX) lanes 18:17 & 15:12 of Board B. There are no AC coupling capacitors on your BoC, it is assume that your EVM hardware has been properly designed and contains the appropriate AC coupling capacitors on the respective AC nets.

CAUTION: Confirm that your EVM supports this interface and that the number of interfaces as well as the pinout locations is supported correctly.

X. I2C interface [5, 9, 11, 23]

Your BoC card is designed with EEPROMs sitting on the I2C bus for each EVM. Each EEPROM is isolated from the other and resides on the AMCC backplane bus to the respective EVM. From the factory, this interface to each respective EVM is electrically ready for use but not directly connected to the EVM's. Prior to use, the series termination resistors (0ohm) are required to be installed. These resistors are designed in as SMT components, 0402 in size. The following figure illustrates the pin out for both EEPROM interface headers. These headers (JP4 & JP5) can be used to program the individual on board EEPROMs. Your EEPROMS are blank from Texas Instruments. JP5 is the interface and programming header for Board A, and JP4 is the interface and programming header for Board B.

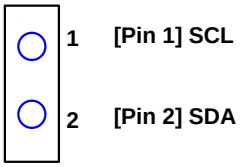


Figure 6 - I2C Programming Header

Each EEPROM contains a dedicated switch used to define the address. This feature was added to allow the end user the ability to change the EEPROM address in the event there was address contention do to something else sitting on the same bus. An on indication is denoted as "0". JP4 is default configured as 0x011, JP5 is default configured as 0x000. The following table is provided to illustrate the switch to eeprom address correlation.

Table 2: JP5 & JP4 (Board A & B) I2C Switch Configuration

	JP4		JP5		
EEPROM Address	**ON**	**OFF**	**ON**	**OFF**	**Switch**
A0	X		X		1-6
A1		X	X		2-5
A2		X	X		3-4

WARNING: The I2C Interface is intended to operate at 3.3V, Confirm that your EVM level shifts this into to correct DSP range before using this interface or connecting your EVM's.

CAUTION: Confirm that your EVM supports this interface and that the number of interfaces as well as the pinout locations is supported correctly.

XI. Common REFCLK Source

Your BoC has the capability of supplying a common REFCLK both EVM's. This common REFCLK is generated on the BoC and sourced from a dedicated differential oscillator through a high performance 1:2 low clock jitter buffer (U12). On your BoC is JP10, this header and shunt are used to enable or disable the differential oscillator on the BoC. By default the shunt is applied on this header, placing the oscillator input to the clock mux in a Hi-Z state.

Not all EVM's directly support this feature, future EVM's will incorporate this feature and have it connected to a EVM clock source (typically att the secondary clock source input) through the AMC connectors and respective nets. The clock routing is skew matched between AMC headers to within 5ps.

a. REFCLK Oscillator Enable Header [19]

The following table defines the possible configurations for JP10. JP10 is used to enable or disable the 30.72MHz differential clock source (U14) input to the CDCLVP1102 which is intended to provide a common clock source to both EVM's for the REFCLK. By default the shunt is installed and the REFCLK source is disabled.

Table 3: JP10 REFCLK Enable Header

JP10		
ON	**Disabled**	
OFF	Enabled	
	OFF	**ON**
1		X
2		X

b. REFCLK Signal Levels

The output of the low jitter 1:2 clock buffer is LVPECL (low voltage PECL). As such this logic level may not be adequate for your DSP. Consult your DSP data manual and the data manual for the CDCLVP1102 before using this hardware. Prior to proceeding it will also be necessary to confirm that the EVM clock source input (that the REFCLK is connecting to) is AC coupled and/or biased. Your BoC REFCLKp/n outputs are **not** AC

coupled, however they are biased. The current biasing scheme implemented is designed to provide the appropriate swing for most TI DSP's available today.

The following two figures illustrate the configuration for the REFCLK generation and biasing components. If a change in the output swing is needed, remove and replace the appropriate components carefully.

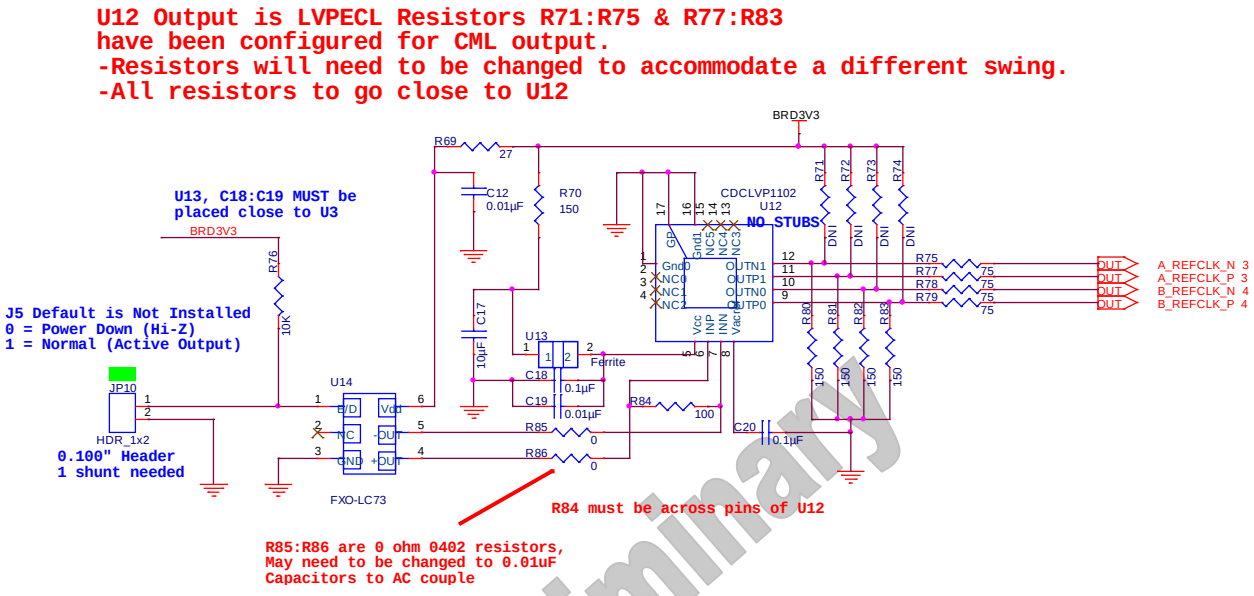


Figure 7: REFCLK Logic

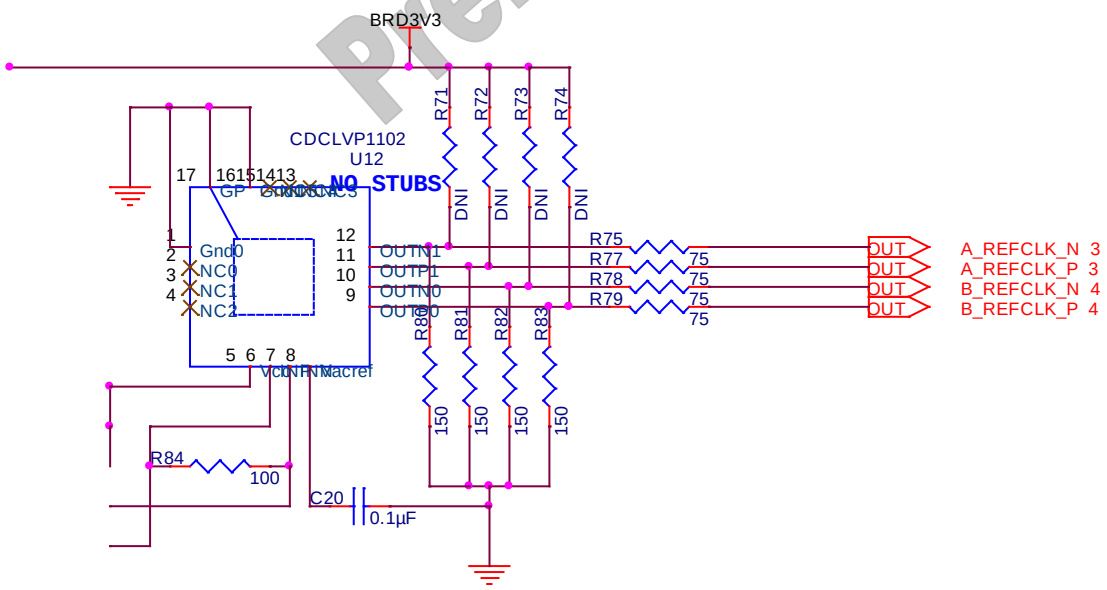


Figure 8: REFCLK Biasing Components

XII. Timer0 Output Headers [12, 22]

The BoC incorporates a separate single header connected (through the AMC B+ connector) to each EVM's DSP's Timer0 output pin [*DSP Timer0_output ➔BoC Timer0_output*]. Header JP8 [22] is connected to Board B and header JP9 [12] is connected to Board A. This timer pin can be used to initiate a trigger event which is configurable using J5. Refer to section XVIII for additional configuration details.

Your BoC is also provided with a custom 12"-14" (30.48cm – 35.46cm) jumper wire that can be used to connect between older EVM's auxillary header containing the TimerOut0 pin to the either JP8 or JP9. This jumper is specifically designed with a 0.018" (0.457mm) male pin (on one side) that if used can be inserted into the appropriate location on the EVM auxillary header of you EVM, the opposite end contains a female header that is designed to attach to either JP8 or JP9. Refer to section XVIII for detailed information on configurations options.

CAUTION: Different versions of EVM's have different pinout configurations, confirm that your EVM supports this interface and feature.

XIII. Timer0 Input Header [10, 24]

The BoC incorporates a separate single header connected (through the AMC B+ connector) to each EVM's DSP's Timer0 input pin [*DSP Timer0_input ➔BoC Timer0_input*]. Header JP6 [10] is connected to Board B and header JP7 [24] is connected to Board A. This timer input pin to each respective DSP is provided for convience in the event future connection is required.

CAUTION: Different versions of EVM's have different pinout configurations, confirm that your EVM supports this interface and feature.

XIV. Common RP1CLK Source

Your BoC has the capability of supplying a common RP1CLK both EVM's. This common RP1CLK is generated on the BoC and sourced from a dedicated differential oscillator through a high performance 1:2 low clock jitter buffer (U1). On your BoC is JP1, this header and shunt are used to enable or disable the differential oscillator on the BoC. By default the shunt is applied on this header, placing the oscillator input to the clock mux in a Hi-Z state.

Not all EVM's directly support this feature, future EVM's will incorporate this feature to allow for design debug, expandability and test. The clock routing is skew matched between AMC headers to within 5ps.

a. RP1CLK Oscillator Enable Header [8]

The following table defines the possible configurations for JP1. JP1 is used to enable or disable the 30.72MHz differential clock source (U2) input to the CDCLVP1102 which is intended to provide a common clock source to both EVM's for the RP1CLK. By default the shunt is installed and the RP1CLK source is disabled.

Table 4: JP1 RP1CLK Enable Header

JP1		
ON	**Disabled**	
OFF	Enabled	
	OFF	**ON**
1		X
2		X

b. RP1CLK Signal Levels

The output of the low jitter 1:2 clock buffer is LVPECL (low voltage PECL). As such this logic level may not be adequate for your DSP. Consult your DSP data manual and the data manual for the CDCLVP1102 before using this hardware. Prior to proceeding it will also be necessary to confirm that the EVM clock source input (that the REFCLK is connecting to) is AC coupled and/or biased. Your BoC RP1CLKp/n outputs are **not** AC coupled, however they are biased. The current biasing scheme implemented is designed to provide the appropriate swing for most TI DSP's available today.

The following two figures illustrate the configuration for the REFCLK generation and biasing components. If a change in the output swing is needed, remove and replace the appropriate components carefully.

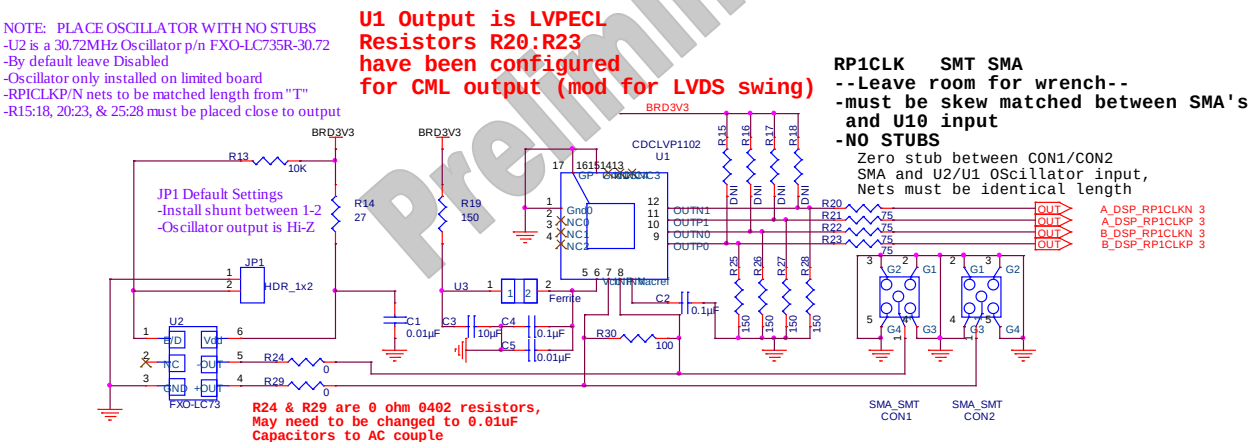


Figure 9: RP1CLK Logic

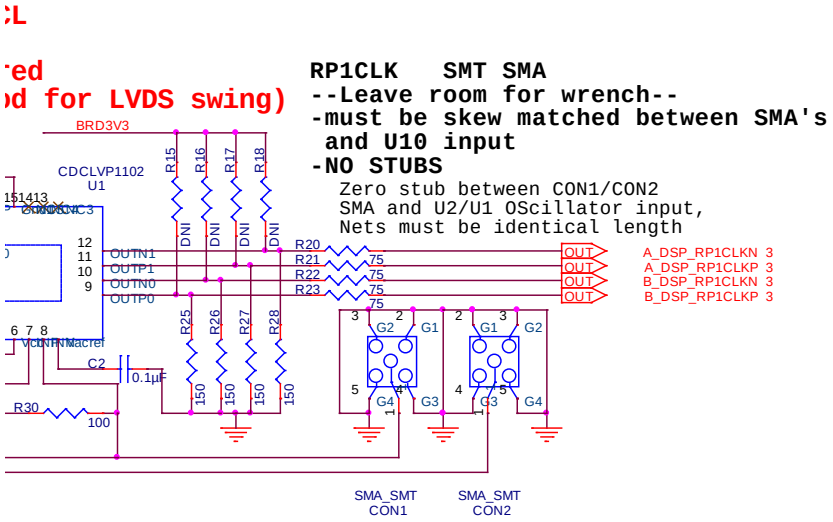


Figure 10: RP1CLK Biasing Components

CAUTION: Different versions of EVM's have different pinout configurations, confirm that your EVM supports this interface and feature.

c. Alternate RP1CLK Inputs [15]

Your BoC has been designed with auxillary SMA input connectors (CON1 & CON2) in the event a different RP1CLK frequency is desired. Should you elect to utilize this input it will be necessary to confirm that it meets the input requirements of the CDCLVP1102 and that the corresponding outputs are properly biased, and that the oscillator is disabled (install JP1 shunt). CON1 is the negative polarity differential input; CON2 is the positive polarity differential input to the CDCLVP1102.

XV. Common TCLK_B Source

Your BoC has the capability of supplying a common TCLK_B to both EVM's. This common TCLK_B is generated on the BoC and sourced from a dedicated differential oscillator through a high performance 1:2 low clock jitter buffer (U6). On your BoC is JP2; this header and shunt are used to enable or disable the differential oscillator on the BoC. By default the shunt is applied on this header, placing the oscillator input to the clock mux in a Hi-Z state.

Not all EVM's directly support this feature, future EVM's will incorporate this feature to allow for advanced clocking and test. The clock routing is skew matched between AMC headers to within 5ps.

a. TCLK_B Oscillator Enable Header [14]

The AMC standard allows for external clock sources across the backplane bus, TCLK_x are several of the clocks allowed. The following table defines the possible configurations for JP2. JP2 is used to enable or disable the 30.72MHz differential clock source (U6) input to the CDCLVP1102 which is intended to provide a common clock source of

30.72MHz to both EVM's for TCLK_B. By default the shunt is installed and the REFCLK source is disabled.

Table 5: JP2 TCLK_B Enable Header

JP2		
ON	**Disabled**	
OFF	Enabled	
	OFF	**ON**
1		X
2		X

b. TCLK_B Signal Outputs [2, 13]

There are two headers provided on your BoC; J1 & J2. Board A makes use of the 1 x 4 header whereas Board A interfaces with J2. In some current production TI EVM's these pins are connected to the AMC headers, others not – confirm proper connection before powering up or using this feature. Due to layout constrainst J1 and J2 pinouts are not identical – please refer to the following figure and the silk screen on your BoC for proper pin locations.

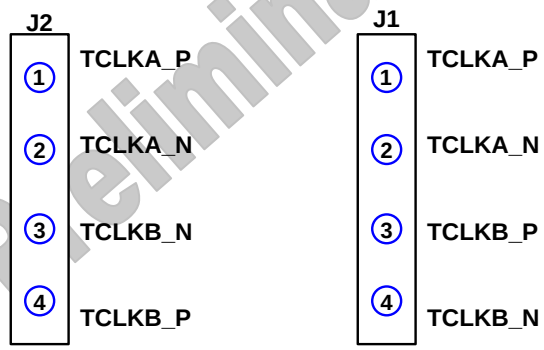


Figure 11: TCLK_B Interface

CAUTION: Different versions of EVM's have different pinout configurations, confirm that your EVM supports this interface and feature.

The oscillator source (U5) is routed into the low jitter 1:2 clock buffer (U6), the output is a biased LVPECL (low voltage PECL). Some EVM input logic levels may have to be adjusted to properly interface with your DSP, consult your DSP data manual and the data manual for the CDCLVP1102 before using this hardware or making any modifications.

Prior to proceeding it will also be necessary to confirm that the TCLK_B pins are not assigned other functions and that no contention will occur. Your BoC REFCLKp/n outputs are **not** AC coupled, however they are biased. The current biasing scheme implemented is designed to provide the appropriate swing for most TI DSP's available today.

The following two figures illustrate the configuration for the REFCLK generation and biasing components. If a change in the output swing is needed, remove and replace the appropriate components carefully.

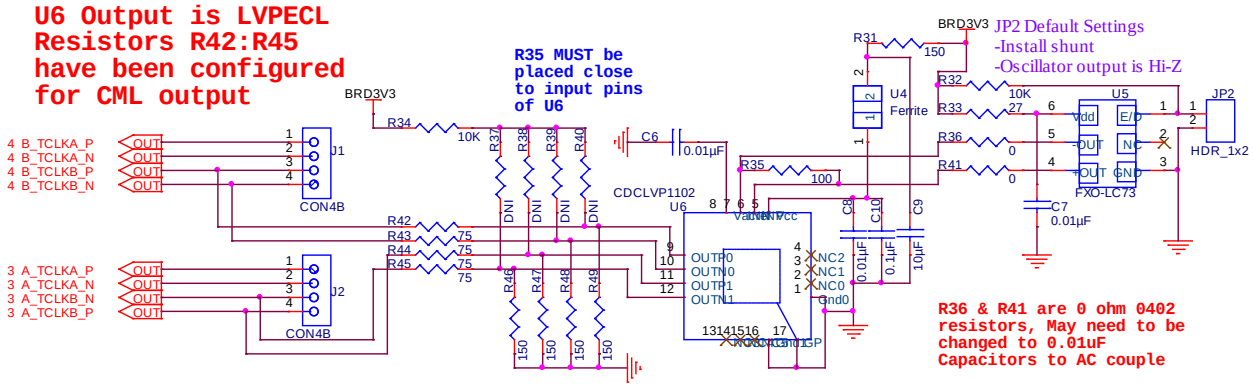


Figure 12: TCLK_B Logic

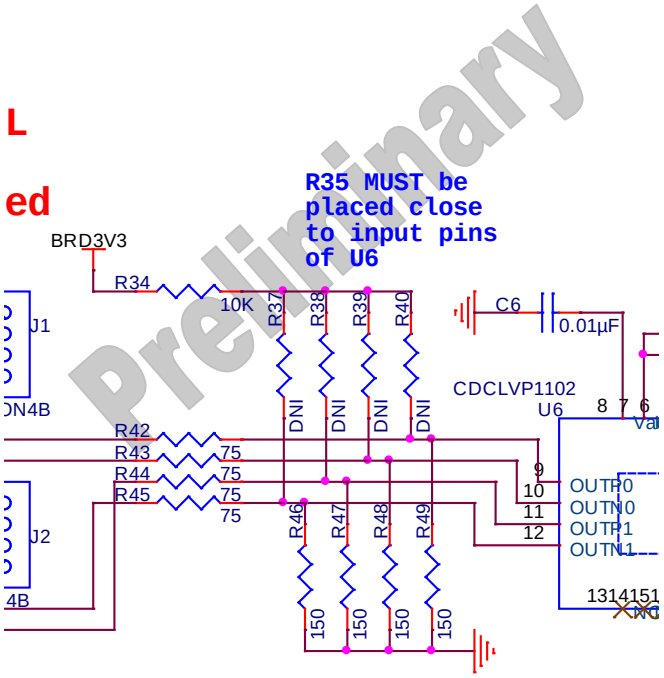


Figure 13: TCLK_B Biasing Components

c. TCLK_A Signal Outputs [2, 13]

Headers J1 & J2 are provided as a means of connecting the on board clock source to each respective DSP. TCLK_A is additionally provided on pins 1 & 2 of each header and routed to the respective pins on the AMC connectors. There is no logic attached to these pins which can be used to connect an alternate clock source into the DSP.

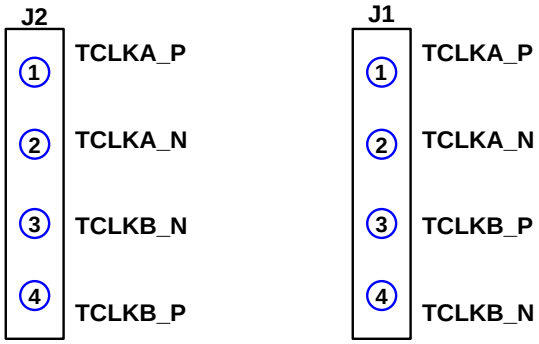


Figure 14: TCLK_B Interface

CAUTION: Different versions of EVM's have different pinout configurations, confirm that your EVM supports this interface and feature.

Before using this interface to your BoC, confirm the logic levels and terminations are correct.

XVI. Common PCIeREFCLK Source [25]

Your BoC has the capability of supplying a common PCIeREFCLK to both EVM's. This common PCIeREFCLK is generated on the BoC and sourced from a dedicated 25MHz crystal (U8) connected to a low noise crystal-to-HCSL clock generator (U7). On your BoC is JP3, this header and shunt are used to enable or disable the differential oscillator on the BoC. By default the shunt is applied on this header and the output disabled.

Not all EVM's directly support this feature, future EVM's will incorporate this feature to allow for improved functionality and testing. The clock routing is skew matched between AMC headers to within 5ps.

a. PCIeREFCLK Crystal-to-HCSL Output Enable Header [25]

The following table defines the possible configurations for JP3. JP3 is used to enable or disable the 25.00MHz differential output connected to each respective AMC header. By default the shunt is installed and the PCIEREFCLK output is disabled.

Table 6: JP3 PCIEREFCLK Enable Header

JP3		
ON	**Disabled**	
OFF	Enabled	
	OFF	**ON**
1		X
2		X

b. PCIeREFCLK Logic

The following figure illustrates the support logic for the PCIeREFCLK gerneration circuit

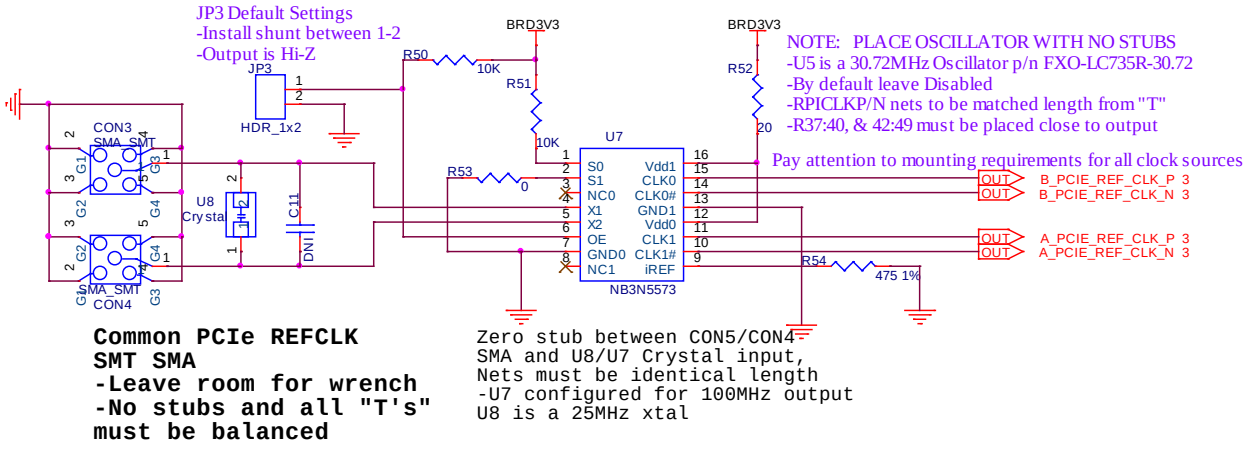


Figure 15: RP1CLK Logic

c. Alternate PCIeREFCLK Inputs [4]

Your BoC has been designed with auxillary SMA input connectors (CON3 & CON4) in the event a different PCIeREFCLK frequency is desired. Should you elect to utilize this input it will be necessary to confirm that it meets the input requirements of the crystal-to-HCSL logic and that the corresponding outputs are properly biased, and that the crystal is removed.

XVII. RP1FB Source [7]

In order to sync the RP1 clock with the RP1 frame bust interfaces to each EVM, your BoC has been designed with a direct interface. Provided are SMA connectors labeled as CON5 and CON6. Should you elect to utilize this RP1FB input it will be necessary to confirm that the signal provided meets the input requirements of the DSP and that the polarities are correct. CON5 is the negative polarity input; CON6 is the positive polarity input.

XVIII. RADSYNC & PHYSYNC Triggering [6]

Your BoC has the ability to source a trigger and redirect it to an input on one or both DSP's through the AMC header. The intention of this interface is to accept a timer event (trigger) from one EVM and redirect it to another making use of the PHYSYNC or RADSYNC pins. On future EVM's the timer pins will be routed to the AMC backplane interface, until this is implemented the trigger event must be rerouted to the switch using the jumper wire provided (as described in section XII).

Switch J5 has been included in the BoC allowing the ability to select from either DSP Timer0out signal and through various switch configurations redirecting it to either RADSYNC or PHYSYNC pin through the BoC AMC connector. The following figure illustrates the basic naming conventions assigned to the switch (J5).

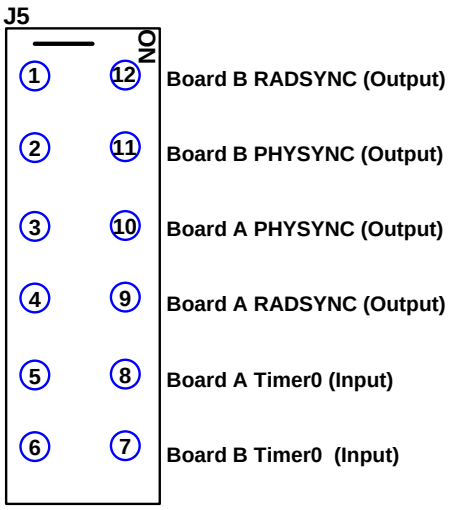


Figure 16: RADSYNC & PHYSYNC Control

The following figure illustrates the logic implemented to support this cross triggering.

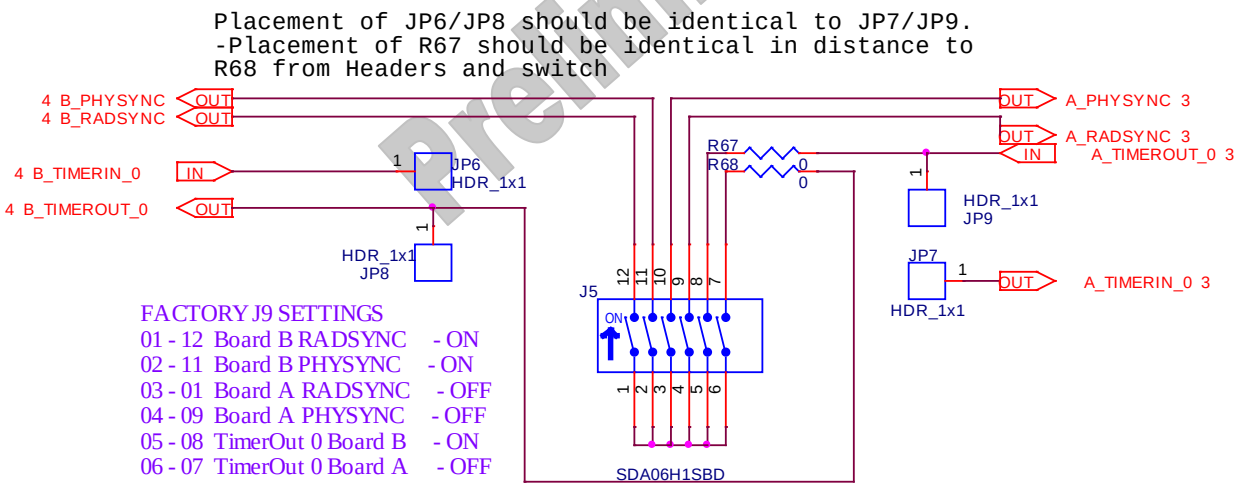


Figure 17: Cross Triggering Switch

The following table is provided for assistance in selecting the trigger souce and destination.

Table 7: RADSYNC / PHYSYNC Trigger Configuration

	SWITCH POSITION					
	1-12	2-11	3-10	4-9	5-8	6-7
TimerOut0 Board B to Board A RADSYNC	open	open	open	closed	closed	open
TimerOut0 Board B to Board A RADSYNC & PHYSYNC	open	open	closed	closed	closed	open
TimerOut0 Board B to Board A PHYSYNC	open	open	closed	open	closed	open
TimerOut0 Board A to Board B RADSYNC	closed	open	open	open	open	closed
TimerOut0 Board A to Board B RADSYNC & PHYSYNC	closed	closed	open	open	open	closed
TimerOut0 Board A to Board B PHYSYNC	open	closed	open	open	open	closed

XIX. Warnings and Cautions

The following warnings and cautions must be followed to ensure proper operation

NOTE: Your BoC Card contains ESD sensitive parts, proper ESD handling procedures are necessary

XX. Pin Assignment [Board A]

The following table is provided relative to the AMC piout assignment for your BoC card.

Table 8: AMC B+ Header Pin Assignment – Board A

Header / Pin Number	Signal		Header / Pin Number	Signal
Board A \ 1	GND		Board A \ 170	GND
Board A \ 2	12V Power		Board A \ 169	TDI
Board A \ 3	N/C		Board A \ 168	TDO_2_TDI
Board A \ 4	N/C		Board A \ 167	TRST#
Board A \ 5	N/C		Board A \ 166	TMS
Board A \ 6	N/C		Board A \ 165	TCK
Board A \ 7	GND		Board A \ 164	GND
Board A \ 8	N/C		Board A \ 163	RP1CLKp
Board A \ 9	12V Power		Board A \ 162	RP1CLKn
Board A \ 10	GND		Board A \ 161	GND
Board A \ 11	SGMII0_TXp		Board A \ 160	SCL
Board A \ 12	SGMII0_TXn		Board A \ 159	SDA
Board A \ 13	GND		Board A \ 158	GND
Board A \ 14	SGMII0_RXp		Board A \ 157	RP1FBp
Board A \ 15	SGMII0_RXn		Board A \ 156	RP1FBn
Board A \ 16	GND		Board A \ 155	GND
Board A \ 17	N/C		Board A \ 154	PHYSYNC
				Con't

Header / Pin Number	Signal		Header / Pin Number	Signal
Board A \ 18	12V Power		Board A \ 153	RADSYNC
Board A \ 19	GND		Board A \ 152	GND
Board A \ 20	SGMII1_TXp		Board A \ 151	AIF5_TXp
Board A \ 21	SGMII1_TXn		Board A \ 150	AIF5_TXn
Board A \ 22	GND		Board A \ 149	GND
Board A \ 23	SGMII1_RXp		Board A \ 148	AIF5_RXp
Board A \ 24	SGMII1_RXn		Board A \ 147	AIF5_RXn
Board A \ 25	GND		Board A \ 146	GND
Board A \ 26	N/C		Board A \ 145	AIF4_TXp
Board A \ 27	12V Power		Board A \ 144	AIF4_TXn
Board A \ 28	GND		Board A \ 143	GND
Board A \ 29	N/C		Board A \ 142	AIF4_RXp
Board A \ 30	N/C		Board A \ 141	AIF4_RXn
Board A \ 31	GND		Board A \ 140	GND
Board A \ 32	N/C		Board A \ 139	REFCLKp
Board A \ 33	N/C		Board A \ 138	REFCLKn
Board A \ 34	GND		Board A \ 137	GND
Board A \ 35	N/C		Board A \ 136	TIMER0OUT
Board A \ 36	N/C		Board A \ 135	TIMER0IN
Board A \ 37	GND		Board A \ 134	GND
Board A \ 38	N/C		Board A \ 133	AIF3_TXp
Board A \ 39	N/C		Board A \ 132	AIF3_TXn
Board A \ 40	GND		Board A \ 131	GND
Board A \ 41	N/C		Board A \ 130	AIF3_RXp
Board A \ 42	12V Power		Board A \ 129	AIF3_RXn
Board A \ 43	GND		Board A \ 128	GND
Board A \ 44	PCIe4_TXp		Board A \ 127	AIF2_TXp
Board A \ 45	PCIe4_TXn		Board A \ 126	AIF2_TXn
Board A \ 46	GND		Board A \ 125	GND
Board A \ 47	PCIe4_RXp		Board A \ 124	AIF2_RXp
Board A \ 48	PCIe4_RXn		Board A \ 123	AIF2_RXn
Board A \ 49	GND		Board A \ 122	GND
Board A \ 50	PCIe5_TXp		Board A \ 121	AIF1_TXp
Board A \ 51	PCIe5_TXn		Board A \ 120	AIF1_TXn
Board A \ 52	GND		Board A \ 119	GND
Board A \ 53	PCIe5_RXp		Board A \ 118	AIF1_RXp
Board A \ 54	PCIe5_RXn		Board A \ 117	AIF1_RXn
Board A \ 55	GND		Board A \ 116	GND
Board A \ 56	N/C		Board A \ 115	AIF0_TXp
Board A \ 57	12V Power		Board A \ 114	AIF0_TXn
Board A \ 58	GND		Board A \ 113	GND
Board A \ 59	PCIe6_TXp		Board A \ 112	AIF0_RXp
Board A \ 60	PCIe6_TXn		Board A \ 111	AIF0_RXn
Board A \ 61	GND		Board A \ 110	GND
Board A \ 62	PCIe6_RXp		Board A \ 109	SRIO4_TXp
Board A \ 63	PCIe6_RXn		Board A \ 108	SRIO4_TXn
Board A \ 64	GND		Board A \ 107	GND
Board A \ 65	PCIe7_TXp		Board A \ 106	SRIO4_RXp
Board A \ 66	PCIe7_TXn		Board A \ 105	SRIO4_RXn
Board A \ 67	GND		Board A \ 104	GND
Board A \ 68	PCIe7_RXp		Board A \ 103	SRIO3_TXp
Board A \ 69	PCIe7_RXn		Board A \ 102	SRIO3_TXn
Board A \ 70	GND		Board A \ 101	GND

Con't

Header / Pin Number	Signal		Header / Pin Number	Signal
Board A \ 71	N/C		Board A \ 100	SRIO3_RXp
Board A \ 72	12V Power		Board A \ 99	SRIO3_RXn
Board A \ 73	GND		Board A \ 98	GND
Board A \ 74	A_TCLK_Ap		Board A \ 97	SRIO2_TXp
Board A \ 75	A_TCLK_An		Board A \ 96	SRIO2_TXn
Board A \ 76	GND		Board A \ 95	GND
Board A \ 77	A_TCLK_Bp		Board A \ 94	SRIO2_RXp
Board A \ 78	A_TCLK_Bn		Board A \ 93	SRIO2_RXn
Board A \ 79	GND		Board A \ 92	GND
Board A \ 80	A_PCIEREFCLK_p		Board A \ 91	SRIO1_TXp
Board A \ 81	A_PCIEREFCLK_n		Board A \ 90	SRIO1_TXn
Board A \ 82	GND		Board A \ 89	GND
Board A \ 83	N/C		Board A \ 88	SRIO1_RXp
Board A \ 84	12V Power		Board A \ 87	SRIO1_RXn
Board A \ 85	GND		Board A \ 86	GND

XXI. Pin Assignment [Board B]

The following table is provided relative to the AMC piout assignment for your BoC card.

Table 9: AMC B+ Header Pin Assignment – Board B

Header / Pin Number	Signal		Header / Pin Number	Signal
Board B \ 1	GND		Board B \ 170	GND
Board B \ 2	12V Power		Board B \ 169	TDO_2_TDI
Board B \ 3	N/C		Board B \ 168	TDO
Board B \ 4	N/C		Board B \ 167	TRST#
Board B \ 5	N/C		Board B \ 166	TMS
Board B \ 6	N/C		Board B \ 165	TCK
Board B \ 7	GND		Board B \ 164	GND
Board B \ 8	N/C		Board B \ 163	RP1CLKp
Board B \ 9	12V Power		Board B \ 162	RP1CLKn
Board B \ 10	GND		Board B \ 161	GND
Board B \ 11	SGMII0_TXp		Board B \ 160	SCL
Board B \ 12	SGMII0_TXn		Board B \ 159	SDA
Board B \ 13	GND		Board B \ 158	GND
Board B \ 14	SGMII0_RXp		Board B \ 157	RP1FBp
Board B \ 15	SGMII0_RXn		Board B \ 156	RP1FBn
Board B \ 16	GND		Board B \ 155	GND
Board B \ 17	N/C		Board B \ 154	PHYSYNC
Board B \ 18	12V Power		Board B \ 153	RADSYNC
Board B \ 19	GND		Board B \ 152	GND
Board B \ 20	SGMII1_TXp		Board B \ 151	AIF5_TXp
Board B \ 21	SGMII1_TXn		Board B \ 150	AIF5_TXn
Board B \ 22	GND		Board B \ 149	GND
Board B \ 23	SGMII1_RXp		Board B \ 148	AIF5_RXp
Board B \ 24	SGMII1_RXn		Board B \ 147	AIF5_RXn
Board B \ 25	GND		Board B \ 146	GND
Board B \ 26	N/C		Board B \ 145	AIF4_TXp
Board B \ 27	12V Power		Board B \ 144	AIF4_TXn
Board B \ 28	GND		Board B \ 143	GND

Con't

Header / Pin Number	Signal		Header / Pin Number	Signal
Board B \ 29	N/C		Board B \ 142	AIF4_RXp
Board B \ 30	N/C		Board B \ 141	AIF4_RXn
Board B \ 31	GND		Board B \ 140	GND
Board B \ 32	N/C		Board B \ 139	REFCLKp
Board B \ 33	N/C		Board B \ 138	REFCLKn
Board B \ 34	GND		Board B \ 137	GND
Board B \ 35	N/C		Board B \ 136	TIMER0OUT
Board B \ 36	N/C		Board B \ 135	TIMER0IN
Board B \ 37	GND		Board B \ 134	GND
Board B \ 38	N/C		Board B \ 133	AIF3_TXp
Board B \ 39	N/C		Board B \ 132	AIF3_TXn
Board B \ 40	GND		Board B \ 131	GND
Board B \ 41	N/C		Board B \ 130	AIF3_RXp
Board B \ 42	12V Power		Board B \ 129	AIF3_RXn
Board B \ 43	GND		Board B \ 128	GND
Board B \ 44	PCIe4_TXp		Board B \ 127	AIF2_TXp
Board B \ 45	PCIe4_TXn		Board B \ 126	AIF2_TXn
Board B \ 46	GND		Board B \ 125	GND
Board B \ 47	PCIe4_RXp		Board B \ 124	AIF2_RXp
Board B \ 48	PCIe4_RXn		Board B \ 123	AIF2_RXn
Board B \ 49	GND		Board B \ 122	GND
Board B \ 50	PCIe5_TXp		Board B \ 121	AIF1_TXp
Board B \ 51	PCIe5_TXn		Board B \ 120	AIF1_TXn
Board B \ 52	GND		Board B \ 119	GND
Board B \ 53	PCIe5_RXp		Board B \ 118	AIF1_RXp
Board B \ 54	PCIe5_RXn		Board B \ 117	AIF1_RXn
Board B \ 55	GND		Board B \ 116	GND
Board B \ 56	N/C		Board B \ 115	AIF0_TXp
Board B \ 57	12V Power		Board B \ 114	AIF0_TXn
Board B \ 58	GND		Board B \ 113	GND
Board B \ 59	PCIe6_TXp		Board B \ 112	AIF0_RXp
Board B \ 60	PCIe6_TXn		Board B \ 111	AIF0_RXn
Board B \ 61	GND		Board B \ 110	GND
Board B \ 62	PCIe6_RXp		Board B \ 109	SRIO4_TXp
Board B \ 63	PCIe6_RXn		Board B \ 108	SRIO4_TXn
Board B \ 64	GND		Board B \ 107	GND
Board B \ 65	PCIe7_TXp		Board B \ 106	SRIO4_RXp
Board B \ 66	PCIe7_TXn		Board B \ 105	SRIO4_RXn
Board B \ 67	GND		Board B \ 104	GND
Board B \ 68	PCIe7_RXp		Board B \ 103	SRIO3_TXp
Board B \ 69	PCIe7_RXn		Board B \ 102	SRIO3_TXn
Board B \ 70	GND		Board B \ 101	GND
Board B \ 71	N/C		Board B \ 100	SRIO3_RXp
Board B \ 72	12V Power		Board B \ 99	SRIO3_RXn
Board B \ 73	GND		Board B \ 98	GND
Board B \ 74	A_TCLK_Ap		Board B \ 97	SRIO2_TXp
Board B \ 75	A_TCLK_An		Board B \ 96	SRIO2_TXn
Board B \ 76	GND		Board B \ 95	GND
Board B \ 77	A_TCLK_Bp		Board B \ 94	SRIO2_RXp
Board B \ 78	A_TCLK_Bn		Board B \ 93	SRIO2_RXn
Board B \ 79	GND		Board B \ 92	GND
Board B \ 80	A_PCIEREFCLK_p		Board B \ 91	SRIO1_TXp
Board B \ 81	A_PCIEREFCLK_n		Board B \ 90	SRIO1_TXn

Con't

Header / Pin Number	Signal		Header / Pin Number	Signal
Board B \ 82	GND		Board B \ 89	GND
Board B \ 83	N/C		Board B \ 88	SRIO1_RXp
Board B \ 84	12V Power		Board B \ 87	SRIO1_RXn
Board B \ 85	GND		Board B \ 86	GND

XXII. Header Intra-Connections

The following table is provided to indicate the electrical connections between the two headers on your BoC.

Table 10: SerDes Board2Board Connections

Board	Signal		Board	Signal
Board A \ 11	SGMII0_TXp		Board B \ 14	SGMII0_RXp
Board A \ 12	SGMII0_TXn		Board B \ 15	SGMII0_RXn
Board A \ 14	SGMII0_RXp		Board B \ 11	SGMII0_TXp
Board A \ 15	SGMII0_RXn		Board B \ 12	SGMII0_TXn
Board A \ 20	SGMII1_TXp		Board B \ 23	SGMII1_RXp
Board A \ 21	SGMII1_TXn		Board B \ 24	SGMII1_RXn
Board A \ 23	SGMII1_RXp		Board B \ 20	SGMII1_TXp
Board A \ 24	SGMII1_RXn		Board B \ 21	SGMII1_TXn

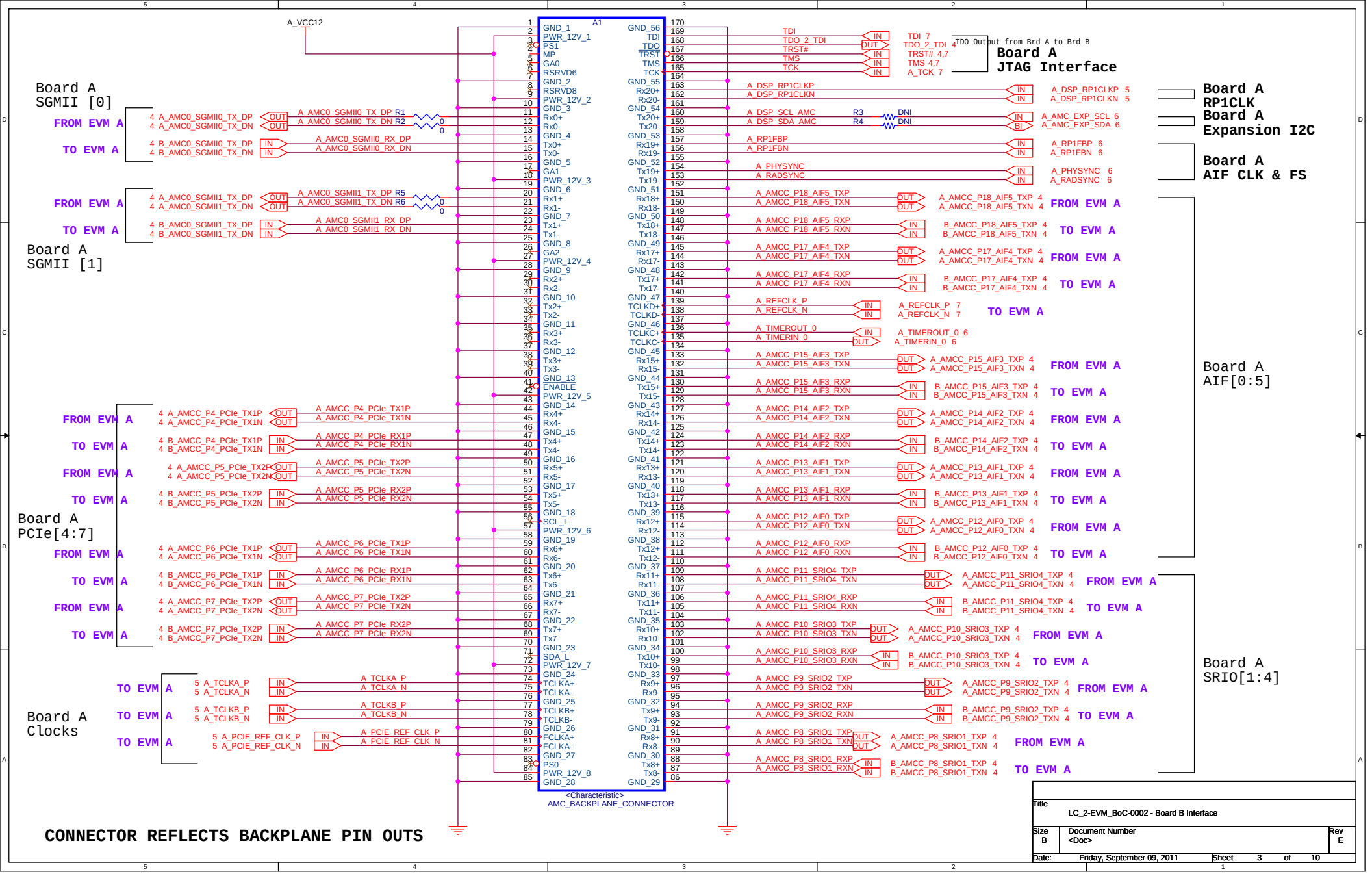
Board	Signal		Board	Signal
Board A \ 44	PCIe4_TXp		Board B \ 47	PCIe4_RXp
Board A \ 45	PCIe4_TXn		Board B \ 48	PCIe4_RXn
Board A \ 47	PCIe4_RXp		Board B \ 44	PCIe4_TXp
Board A \ 48	PCIe4_RXn		Board B \ 45	PCIe4_TXn
Board A \ 50	PCIe5_TXp		Board B \ 53	PCIe5_RXp
Board A \ 51	PCIe5_TXn		Board B \ 54	PCIe5_RXn
Board A \ 53	PCIe5_RXp		Board B \ 50	PCIe5_TXp
Board A \ 54	PCIe5_RXn		Board B \ 51	PCIe5_TXn
Board A \ 59	PCIe6_TXp		Board B \ 62	PCIe6_RXp
Board A \ 60	PCIe6_TXn		Board B \ 63	PCIe6_RXn
Board A \ 62	PCIe6_RXp		Board B \ 59	PCIe6_TXp
Board A \ 63	PCIe6_RXn		Board B \ 60	PCIe6_TXn
Board A \ 65	PCIe7_TXp		Board B \ 68	PCIe7_RXp
Board A \ 66	PCIe7_TXn		Board B \ 69	PCIe7_RXn
Board A \ 68	PCIe7_RXp		Board B \ 65	PCIe7_TXp
Board A \ 69	PCIe7_RXn		Board B \ 66	PCIe7_TXn
				Con't

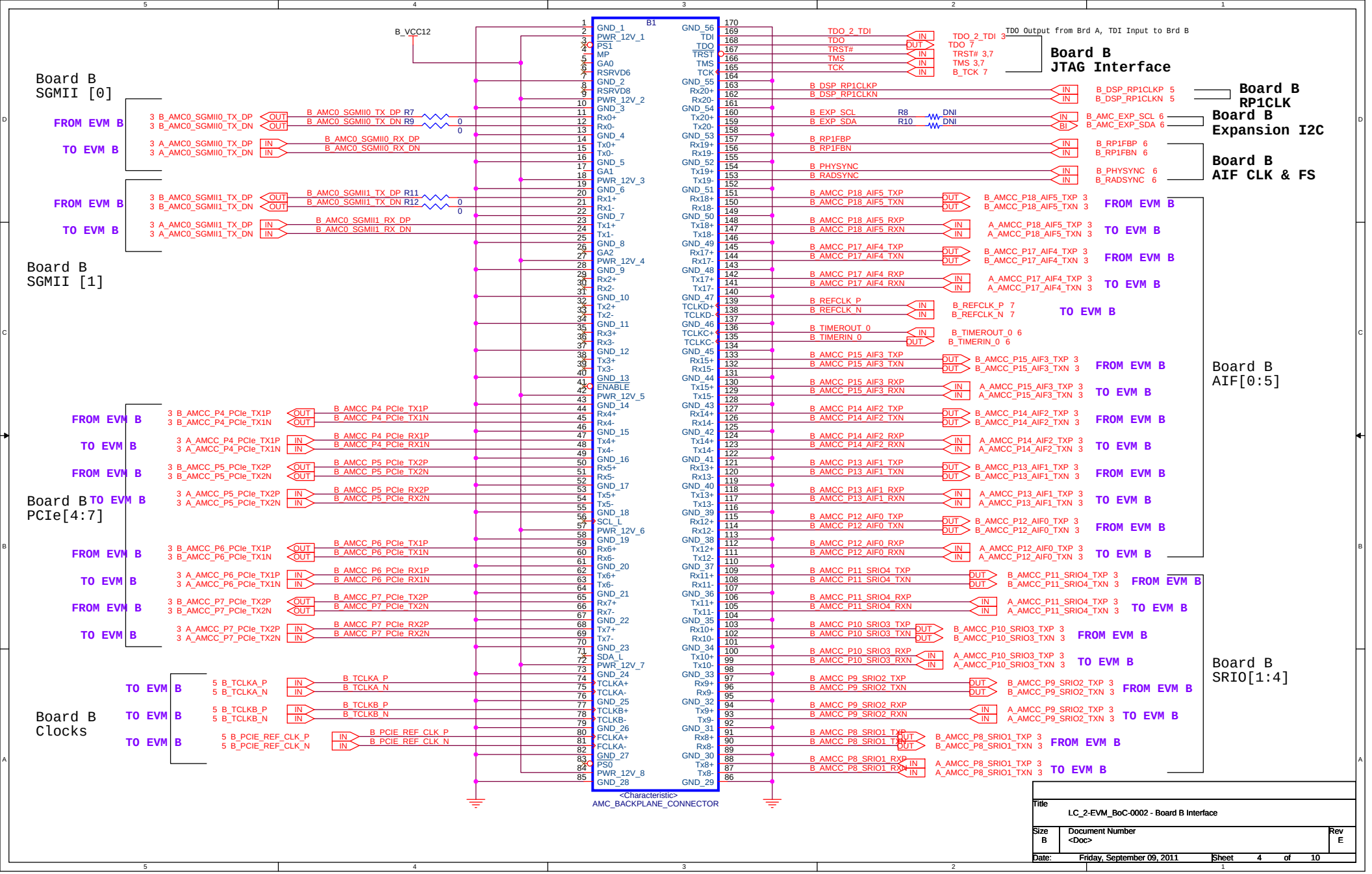
Board	Signal		Board	Signal
Board A \ 151	AIF5_TXp		Board B \ 148	AIF5_RXp
Board A \ 150	AIF5_TXn		Board B \ 147	AIF5_RXn
Board A \ 148	AIF5_RXp		Board B \ 151	AIF5_TXp
Board A \ 147	AIF5_RXn		Board B \ 150	AIF5_TXn
Board A \ 145	AIF4_TXp		Board B \ 142	AIF4_RXp
Board A \ 144	AIF4_TXn		Board B \ 141	AIF4_RXn
Board A \ 142	AIF4_RXp		Board B \ 145	AIF4_TXp
Board A \ 141	AIF4_RXn		Board B \ 144	AIF4_TXn
Board A \ 133	AIF3_TXp		Board B \ 130	AIF3_RXp
Board A \ 132	AIF3_TXn		Board B \ 129	AIF3_RXn
Board A \ 130	AIF3_RXp		Board B \ 133	AIF3_TXp
Board A \ 129	AIF3_RXn		Board B \ 132	AIF3_TXn
Board A \ 127	AIF2_TXp		Board B \ 124	AIF2_RXp
Board A \ 126	AIF2_TXn		Board B \ 123	AIF2_RXn
Board A \ 124	AIF2_RXp		Board B \ 127	AIF2_TXp
Board A \ 123	AIF2_RXn		Board B \ 126	AIF2_TXn
Board A \ 121	AIF1_TXp		Board B \ 118	AIF1_RXp
Board A \ 120	AIF1_TXn		Board B \ 117	AIF1_RXn
Board A \ 118	AIF1_RXp		Board B \ 121	AIF1_TXp
Board A \ 117	AIF1_RXn		Board B \ 120	AIF1_TXn
Board A \ 115	AIF0_TXp		Board B \ 112	AIF0_RXp
Board A \ 114	AIF0_TXn		Board B \ 111	AIF0_RXn
Board A \ 112	AIF0_RXp		Board B \ 115	AIF0_TXp
Board A \ 111	AIF0_RXn		Board B \ 114	AIF0_TXn

Board	Signal		Board	Signal
Board A \ 109	SRIO4_TXp		Board B \ 106	SRIO4_RXp
Board A \ 108	SRIO4_TXn		Board B \ 105	SRIO4_RXn
Board A \ 106	SRIO4_RXp		Board B \ 109	SRIO4_TXp
Board A \ 105	SRIO4_RXn		Board B \ 108	SRIO4_TXn
Board A \ 103	SRIO3_TXp		Board B \ 100	SRIO3_RXp
Board A \ 102	SRIO3_TXn		Board B \ 99	SRIO3_RXn
Board A \ 100	SRIO3_RXp		Board B \ 103	SRIO3_TXp
Board A \ 99	SRIO3_RXn		Board B \ 102	SRIO3_TXn
Board A \ 97	SRIO2_TXp		Board B \ 94	SRIO2_RXp

Con't

Board	Signal		Board	Signal
Board A \ 96	SRIO2_TXn		Board B \ 93	SRIO2_RXn
Board A \ 94	SRIO2_RXp		Board B \ 97	SRIO2_TXp
Board A \ 93	SRIO2_RXn		Board B \ 96	SRIO2_TXn
Board A \ 91	SRIO1_TXp		Board B \ 88	SRIO1_RXp
Board A \ 90	SRIO1_TXn		Board B \ 87	SRIO1_RXn
Board A \ 88	SRIO1_RXp		Board B \ 91	SRIO1_TXp
Board A \ 87	SRIO1_RXn		Board B \ 90	SRIO1_TXn


A_VCC12
A1
GND_1 PWR_12V_1 PS1 MP GA0 RSRVD6 GND_2 RSRVD8 PWR_12V_2 GND_3 Rx0+ Rx0- GND_4 Tx0+ Tx0- GND_5 GA1 PWR_12V_3 GND_6 Rx1+ Rx1- GND_7 Tx1+ Tx1- GND_8 GA2 PWR_12V_4 GND_9 Rx2+ Rx2- GND_10 Tx2+ Tx2- GND_11 Rx3+ Rx3- GND_12 Tx3+ Tx3- GND_13 ENABLE PWR_12V_5 GND_14 Rx4+ Rx4- GND_15 Tx4+ Tx4- GND_16 Rx5+ Rx5- GND_17 Tx5+ Tx5- GND_18 SCL_L PWR_12V_6 GND_19 Rx6+ Rx6- GND_20 Tx6+ Tx6- GND_21 Rx7+ Rx7- GND_22 Tx7+ Tx7- GND_23 SDA_L PWR_12V_7 GND_24 TCLKA+ TCLKA- GND_25 TCLKB+ TCLKB- GND_26 FCLKA+ FCLKA- GND_27 PS0 PWR_12V_8 GND_28
GND_56 TDI TDO TRST TMS TCK GND_55 Rx20+ Rx20- GND_54 Tx20+ Tx20- GND_53 Rx19+ Rx19- GND_52 Tx19+ Tx19- GND_51 Rx18+ Rx18- GND_50 Tx18+ Tx18- GND_49 Rx17+ Rx17- GND_48 Tx17+ Tx17- GND_47 TCLKD+ TCLKD- GND_46 TCLKC+ TCLKC- GND_45 Rx15+ Rx15- GND_44 Tx15+ Tx15- GND_43 Rx14+ Rx14- GND_42 Tx14+ Tx14- GND_41 Rx13+ Rx13- GND_40 Tx13+ Tx13- GND_39 Rx12+ Rx12- GND_38 Tx12+ Tx12- GND_37 Rx11+ Rx11- GND_36 Tx11+ Tx11- GND_35 Rx10+ Rx10- GND_34 Tx10+ Tx10- GND_33 Rx9+ Rx9- GND_32 Tx9+ Tx9- GND_31 Rx8+ Rx8- GND_30 Tx8+ Tx8- GND_29
<Characteristic>
AMC_BACKPLANE_CONNECTOR
Board A SGMII [0]
FROM EVM A
TO EVM A
A_AMC0_SGMII0_TX_DP
A_AMC0_SGMII0_TX_DN
A_AMC0_SGMII0_TX_DP R1
A_AMC0_SGMII0_TX_DN R2
A_AMC0_SGMII0_RX_DP
A_AMC0_SGMII0_RX_DN
Board A SGMII [1]
A_AMC0_SGMII1_TX_DP
A_AMC0_SGMII1_TX_DN
A_AMC0_SGMII1_TX_DP R5
A_AMC0_SGMII1_TX_DN R6
A_AMC0_SGMII1_RX_DP
A_AMC0_SGMII1_RX_DN
Board A PCIe[4:7]
A_AMCC_P4_PCIe_TX1P
A_AMCC_P4_PCIe_TX1N
A_AMCC_P4_PCIe_RX1P
A_AMCC_P4_PCIe_RX1N
A_AMCC_P5_PCIe_TX2P
A_AMCC_P5_PCIe_TX2N
A_AMCC_P5_PCIe_RX2P
A_AMCC_P5_PCIe_RX2N
A_AMCC_P6_PCIe_TX1P
A_AMCC_P6_PCIe_TX1N
A_AMCC_P6_PCIe_RX1P
A_AMCC_P6_PCIe_RX1N
A_AMCC_P7_PCIe_TX2P
A_AMCC_P7_PCIe_TX2N
A_AMCC_P7_PCIe_RX2P
A_AMCC_P7_PCIe_RX2N
Board A Clocks
A_TCLKA_P
A_TCLKA_N
A_TCLKB_P
A_TCLKB_N
A_PCIE_REF_CLK_P
A_PCIE_REF_CLK_N
TDI
TDO_2_TDI
TRST#
TMS
TCK
TDO Output from Brd A to Brd B
Board A JTAG Interface
A_DSP_RP1CLKP
A_DSP_RP1CLKN
Board A RP1CLK
A_DSP_SCL_AMC
A_DSP_SDA_AMC
R3 DNI
R4 DNI
Board A Expansion I2C
A_RP1FBP
A_RP1FBN
A_PHYSYNC
A_RADSYNC
Board A AIF CLK & FS
A_AMCC_P18_AIF5_TXP
A_AMCC_P18_AIF5_TXN
A_AMCC_P18_AIF5_RXP
A_AMCC_P18_AIF5_RXN
A_AMCC_P17_AIF4_TXP
A_AMCC_P17_AIF4_TXN
A_AMCC_P17_AIF4_RXP
A_AMCC_P17_AIF4_RXN
A_REFCLK_P
A_REFCLK_N
A_TIMEROUT_0
A_TIMERIN_0
A_AMCC_P15_AIF3_TXP
A_AMCC_P15_AIF3_TXN
A_AMCC_P15_AIF3_RXP
A_AMCC_P15_AIF3_RXN
A_AMCC_P14_AIF2_TXP
A_AMCC_P14_AIF2_TXN
A_AMCC_P14_AIF2_RXP
A_AMCC_P14_AIF2_RXN
A_AMCC_P13_AIF1_TXP
A_AMCC_P13_AIF1_TXN
A_AMCC_P13_AIF1_RXP
A_AMCC_P13_AIF1_RXN
A_AMCC_P12_AIF0_TXP
A_AMCC_P12_AIF0_TXN
A_AMCC_P12_AIF0_RXP
A_AMCC_P12_AIF0_RXN
Board A AIF[0:5]
A_AMCC_P11_SRIO4_TXP
A_AMCC_P11_SRIO4_TXN
A_AMCC_P11_SRIO4_RXP
A_AMCC_P11_SRIO4_RXN
A_AMCC_P10_SRIO3_TXP
A_AMCC_P10_SRIO3_TXN
A_AMCC_P10_SRIO3_RXP
A_AMCC_P10_SRIO3_RXN
A_AMCC_P9_SRIO2_TXP
A_AMCC_P9_SRIO2_TXN
A_AMCC_P9_SRIO2_RXP
A_AMCC_P9_SRIO2_RXN
A_AMCC_P8_SRIO1_TXP
A_AMCC_P8_SRIO1_TXN
A_AMCC_P8_SRIO1_RXP
A_AMCC_P8_SRIO1_RXN
Board A SRIO[1:4]
CONNECTOR REFLECTS BACKPLANE PIN OUTS
Title
LC_2-EVM_BoC-0002 - Board B Interface
Size B
Document Number <Doc>
Rev E
Date: Friday, September 09, 2011
Sheet 3 of 10


Board B SGMII [0]
FROM EVM B
TO EVM B
Board B SGMII [1]
Board B PCIe[4:7]
Board B Clocks
B_VCC12
B1
GND_1
PWR_12V_1
PS1
MP
GA0
RSRVD6
GND_2
RSRVD8
PWR_12V_2
GND_3
Rx0+
Rx0-
GND_4
Tx0+
Tx0-
GND_5
GA1
PWR_12V_3
GND_6
Rx1+
Rx1-
GND_7
Tx1+
Tx1-
GND_8
GA2
PWR_12V_4
GND_9
Rx2+
Rx2-
GND_10
Tx2+
Tx2-
GND_11
Rx3+
Rx3-
GND_12
Tx3+
Tx3-
GND_13
ENABLE
PWR_12V_5
GND_14
Rx4+
Rx4-
GND_15
Tx4+
Tx4-
GND_16
Rx5+
Rx5-
GND_17
Tx5+
Tx5-
GND_18
SCL_L
PWR_12V_6
GND_19
Rx6+
Rx6-
GND_20
Tx6+
Tx6-
GND_21
Rx7+
Rx7-
GND_22
Tx7+
Tx7-
GND_23
SDA_L
PWR_12V_7
GND_24
TCLKA+
TCLKA-
GND_25
TCLKB+
TCLKB-
GND_26
FCLKA+
FCLKA-
GND_27
PS0
PWR_12V_8
GND_28
GND_56
TDI
TDO
TRST
TMS
TCK
GND_55
Rx20+
Rx20-
GND_54
Tx20+
Tx20-
GND_53
Rx19+
Rx19-
GND_52
Tx19+
Tx19-
GND_51
Rx18+
Rx18-
GND_50
Tx18+
Tx18-
GND_49
Rx17+
Rx17-
GND_48
Tx17+
Tx17-
GND_47
TCLKD+
TCLKD-
GND_46
TCLKC+
TCLKC-
GND_45
Rx15+
Rx15-
GND_44
Tx15+
Tx15-
GND_43
Rx14+
Rx14-
GND_42
Tx14+
Tx14-
GND_41
Rx13+
Rx13-
GND_40
Tx13+
Tx13-
GND_39
Rx12+
Rx12-
GND_38
Tx12+
Tx12-
GND_37
Rx11+
Rx11-
GND_36
Tx11+
Tx11-
GND_35
Rx10+
Rx10-
GND_34
Tx10+
Tx10-
GND_33
Rx9+
Rx9-
GND_32
Tx9+
Tx9-
GND_31
Rx8+
Rx8-
GND_30
Tx8+
Tx8-
GND_29
<Characteristic>
AMC_BACKPLANE_CONNECTOR
B_AMC0_SGMII0_TX_DP R7
B_AMC0_SGMII0_TX_DN R9
B_AMC0_SGMII0_RX_DP
B_AMC0_SGMII0_RX_DN
B_AMC0_SGMII1_TX_DP R11
B_AMC0_SGMII1_TX_DN R12
B_AMC0_SGMII1_RX_DP
B_AMC0_SGMII1_RX_DN
B_AMC_P4_PCIe_TX1P
B_AMC_P4_PCIe_TX1N
B_AMC_P4_PCIe_RX1P
B_AMC_P4_PCIe_RX1N
B_AMC_P5_PCIe_TX2P
B_AMC_P5_PCIe_TX2N
B_AMC_P5_PCIe_RX2P
B_AMC_P5_PCIe_RX2N
B_AMC_P6_PCIe_TX1P
B_AMC_P6_PCIe_TX1N
B_AMC_P6_PCIe_RX1P
B_AMC_P6_PCIe_RX1N
B_AMC_P7_PCIe_TX2P
B_AMC_P7_PCIe_TX2N
B_AMC_P7_PCIe_RX2P
B_AMC_P7_PCIe_RX2N
B_TCLKA_P
B_TCLKA_N
B_TCLKB_P
B_TCLKB_N
B_PCIE_REF_CLK_P
B_PCIE_REF_CLK_N
TDO Output from Brd A, TDI Input to Brd B
Board B JTAG Interface
TDO_2_TDI
TDO
TRST#
TMS
TCK
TDO_7
TRST# 3,7
TMS 3,7
B_TCK_7
Board B RP1CLK
B_DSP_RP1CLKP
B_DSP_RP1CLKN
Board B Expansion I2C
B_EXP_SCL
B_EXP_SDA
R8
R10
DNI
B_AMC_EXP_SCL 6
B_AMC_EXP_SDA 6
Board B AIF CLK & FS
B_RP1FBP
B_RP1FBN
B_PHYSYNC
B_RADSYNC
Board B AIF[0:5]
B_AMCC_P18_AIF5_TXP
B_AMCC_P18_AIF5_TXN
B_AMCC_P18_AIF5_RXP
B_AMCC_P18_AIF5_RXN
B_AMCC_P17_AIF4_TXP
B_AMCC_P17_AIF4_TXN
B_AMCC_P17_AIF4_RXP
B_AMCC_P17_AIF4_RXN
B_REFCLK_P
B_REFCLK_N
B_TIMEROUT_0
B_TIMERIN_0
B_AMCC_P15_AIF3_TXP
B_AMCC_P15_AIF3_TXN
B_AMCC_P15_AIF3_RXP
B_AMCC_P15_AIF3_RXN
B_AMCC_P14_AIF2_TXP
B_AMCC_P14_AIF2_TXN
B_AMCC_P14_AIF2_RXP
B_AMCC_P14_AIF2_RXN
B_AMCC_P13_AIF1_TXP
B_AMCC_P13_AIF1_TXN
B_AMCC_P13_AIF1_RXP
B_AMCC_P13_AIF1_RXN
B_AMCC_P12_AIF0_TXP
B_AMCC_P12_AIF0_TXN
B_AMCC_P12_AIF0_RXP
B_AMCC_P12_AIF0_RXN
Board B SRIO[1:4]
B_AMCC_P11_SRIO4_TXP
B_AMCC_P11_SRIO4_TXN
B_AMCC_P11_SRIO4_RXP
B_AMCC_P11_SRIO4_RXN
B_AMCC_P10_SRIO3_TXP
B_AMCC_P10_SRIO3_TXN
B_AMCC_P10_SRIO3_RXP
B_AMCC_P10_SRIO3_RXN
B_AMCC_P9_SRIO2_TXP
B_AMCC_P9_SRIO2_TXN
B_AMCC_P9_SRIO2_RXP
B_AMCC_P9_SRIO2_RXN
B_AMCC_P8_SRIO1_TXP
B_AMCC_P8_SRIO1_TXN
B_AMCC_P8_SRIO1_RXP
B_AMCC_P8_SRIO1_RXN
Title
LC_2-EVM_BoC-0002 - Board B Interface
Size B
Document Number <Doc>
Rev E
Date: Friday, September 09, 2011
Sheet 4 of 10

CLOCK INTERFACE

FULL SILK SCREENING REQUIRED

NOTE: PLACE OSCILLATOR WITH NO STUBS
-U2 is a 30.72MHz Oscillator p/n FXO-LC735R-30.72
-By default leave Disabled
-Oscillator only installed on limited board
-RPICLKP/N nets to be matched length from "T"
-R15:18, 20:23, & 25:28 must be placed close to output

**U1 Output is LVPECL
Resistors R20:R23
have been configured
for CML output (mod for LVDS swing)**

**RP1CLK SMT SMA
--Leave room for wrench--
-must be skew matched between SMA's and U10 input
-NO STUBS**

Zero stub between CON1/CON2
SMA and U2/U1 OScillator input,
Nets must be identical length

JP1 Default Settings
-Install shunt between 1-2
-Oscillator output is Hi-Z

**R24 & R29 are 0 ohm 0402 resistors,
May need to be changed to 0.01uF
Capacitors to AC couple**

**R35 MUST be
placed close
to input pins
of U6**

R30 must be across pins of U1

JP2 Default Settings
-Install shunt
-Oscillator output is Hi-Z

**U6 Output is LVPECL
Resistors R42:R45
have been configured
for CML output**

**R36 & R41 are 0 ohm 0402
resistors, May need to be
changed to 0.01uF
Capacitors to AC couple**

Board B Clocks

Board A Clocks

Zero stub between CON5/CON4
SMA and U8/U7 Crystal input,
Nets must be identical length
-U7 configured for 100MHz output
U8 is a 25MHz xtal

**Common PCIe REFCLK
SMT SMA
-Leave room for wrench
-No stubs and all "T's"
must be balanced**

JP3 Default Settings
-Install shunt between 1-2
-Output is Hi-Z

NOTE: PLACE OSCILLATOR WITH NO STUBS
-U5 is a 30.72MHz Oscillator p/n FXO-LC735R-30.72
-By default leave Disabled
-RPICLKP/N nets to be matched length from "T"
-R37:40, & 42:49 must be placed close to output

Pay attention to mounting requirements for all clock sources

Title: LC_2-EVM_BoC-0002 - Control Interface 1		
Size: B	Document Number: <Doc>	Rev: F
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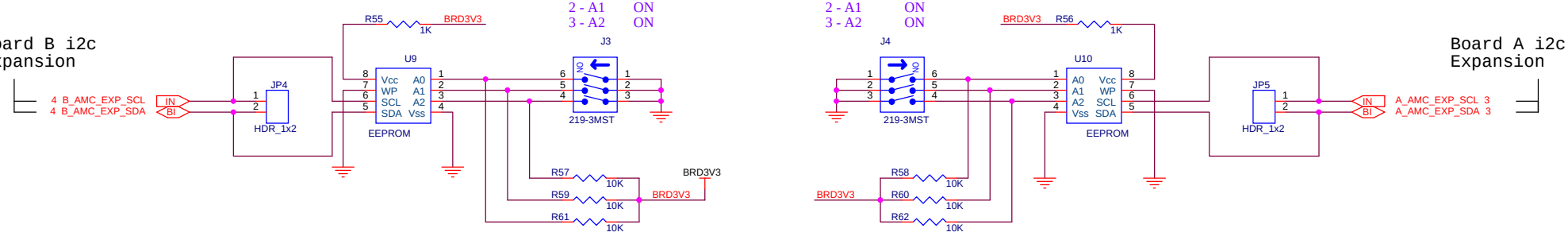
Board B i2c Expansion

J10 [ON = 0] DEFAULT
1 - A0 ON
2 - A1 ON
3 - A2 ON

J11 [ON = 0] DEFAULT
1 - A0 OFF
2 - A1 ON
3 - A2 ON

Board A i2c Expansion

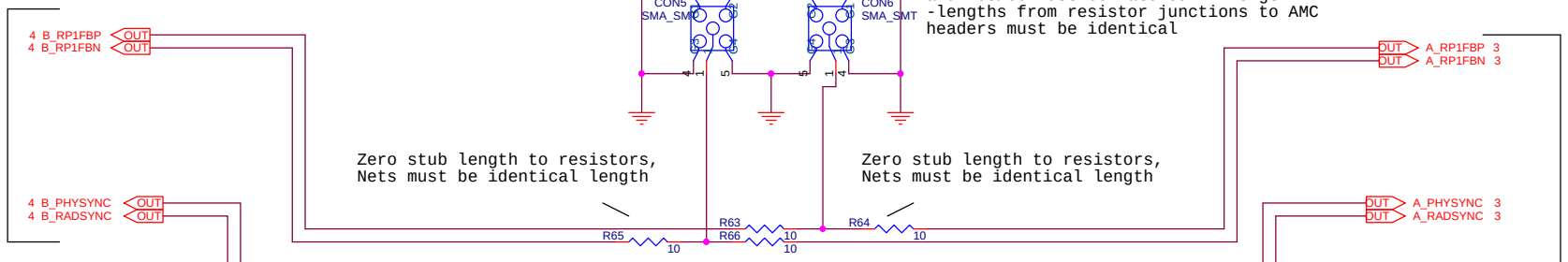


R73 &R32 are 0 ohm 0402 resistors,
May need to be changed to 0.01uF
Capacitors to AC couple

RP1FB / SMT SMA
--Leave room for wrench--

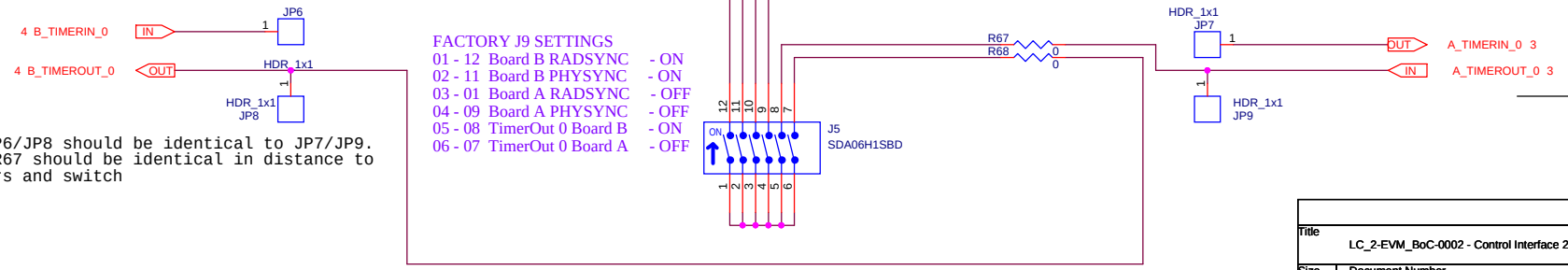
CON5 net connections to R63/64 and R65/66 must be matched in length -lengths from resistor junctions to AMC headers must be identical

Board B AIF CLK & FS



Zero stub length to resistors, Nets must be identical length

Zero stub length to resistors, Nets must be identical length



FACTORY J9 SETTINGS
01 - 12 Board B RADSYNC - ON
02 - 11 Board B PHYSYNC - ON
03 - 01 Board A RADSYNC - OFF
04 - 09 Board A PHYSYNC - OFF
05 - 08 TimerOut 0 Board B - ON
06 - 07 TimerOut 0 Board A - OFF

Board A AIF CLK & FS

Placement of JP6/JP8 should be identical to JP7/JP9.
-Placement of R67 should be identical in distance to R68 from Headers and switch

Title	LC_2-EVM_BoC-0002 - Control Interface 2	
Size B	Document Number <Doc>	Rev A
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POWER SUPPLY

REG1117-3.3 (0.8A)

U12 Output is LVPECL Resistors R71:R75 & R77:R83 have been configured for CML output.
-Resistors will need to be changed to accommodate a different swing.
-All resistors to go close to U12

BJ_MH1 & BJ_MH2
-Mounting hole to support Pamona 2142-2 (Red Banana Jack, Through hole)

J6 Default 1:2
0.100" Header
1 shunt needed

U13, C18:C19 MUST be placed close to U3

J5 Default is Not Installed
0 = Power Down (Hi-Z)
1 = Normal (Active Output)

0.100" Header
1 shunt needed

R84 must be across pins of U12

R85:R86 are 0 ohm 0402 resistors, May need to be changed to 0.01uF Capacitors to AC couple

BJ_MH3
-Mounting hole to support Pamona 2142-0 (Black Banana Jack, Through hole)

Board A & B Daisy Chain JTAG Interface

NOTE: Interface is 3.3V and requires 3.3V level translation prior to interface with DSP. This is done to comply with the current AMC specification

NOTE: Mounting holes are plated through, after plating, holes must support 6/32 mounting hardware and standoffs

TDI from Emulator to DSP
TDO from DSP to Emulator

TVD Target Power Supply for IO's

TCKRTn total length to match TCK routing on EVM's (No stubs allowed, resistor connection should be as close to header pin as possible.

EMULATION INTERFACE

Title	LC_2-EVM_BoC-0002 - Control Interface 3 - JTAG		
Size B	Document Number <Doc>		Rev D
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