

DC MOTOR DRIVER IC

Check for Samples: DRV8814

FEATURES

- **Dual H-Bridge Current-Control Motor Driver**
 - Drives Two DC Motors
 - Brake Mode
 - Two-Bit Winding Current Control Allows Up to 4 Current Levels
 - Low MOSFET On-Resistance
- 2.5-A Maximum Drive Current at 24 V, 25°C
- **Built-In 3.3-V Reference Output**
- **Industry Standard Parallel Digital Control** Interface

- 8-V to 45-V Operating Supply Voltage Range
- **Thermally Enhanced Surface Mount Package APPLICATIONS**
 - **Printers**
 - **Scanners**
- Office Automation Machines
- **Gaming Machines**
- **Factory Automation**
- **Robotics**

DESCRIPTION

The DRV8814 provides an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device has two H-bridge drivers, and is intended to drive DC motors. The output driver block for each consists of N-channel power MOSFET's configured as H-bridges to drive the motor windings. The DRV8814 can supply up to 2.5-A peak or 1.75-A RMS output current (with proper heatsinking at 24 V and 25°C) per H-bridge.

A simple parallel digital control interface is compatible with industry-standard devices. Decay mode is programmable to allow braking or coasting of the motor when disabled.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature.

TheDRV8814 is available in a 28-pin HTSSOP package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

ORDERING INFORMATION(1)

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PowerPAD™ (HTSSOP) - PWP	Reel of 2000	DRV8814PWPR	8814

⁽¹⁾ For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet. PowerPAD is a trademark of Texas Instruments.



DEVICE INFORMATION

Functional Block Diagram

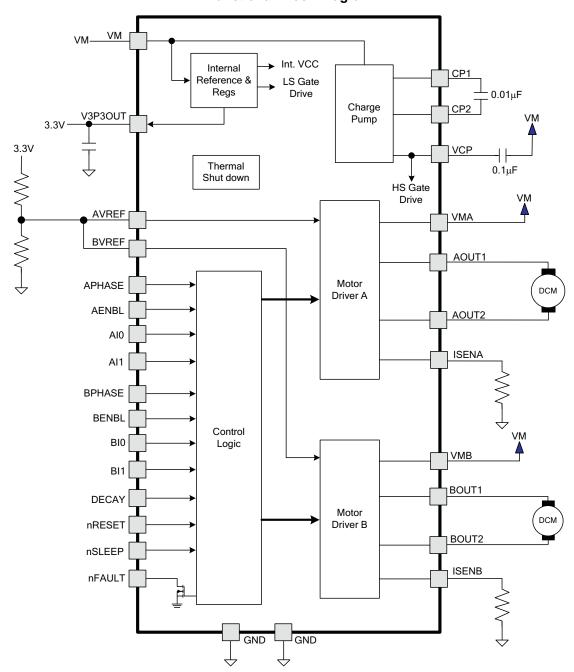




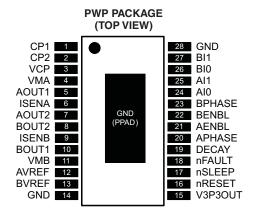
Table 1. TERMINAL FUNCTIONS

NAME	PIN	I/O ⁽¹⁾	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS			
POWER AND	GROUND						
GND	14, 28	-	Device ground				
VMA	4	-	Bridge A power supply	Connect to motor supply (8 - 45 V). Both pins			
VMB	11	-	Bridge B power supply	must be connected to same supply.			
V3P3OUT	15	0	3.3-V regulator output	Bypass to GND with a 0.47-µF 6.3-V ceramic capacitor. Can be used to supply VREF.			
CP1	1	Ю	Charge pump flying capacitor	Connect a 0.01-µF 50-V capacitor between			
CP2	2	Ю	Charge pump flying capacitor	CP1 and CP2.			
VCP	3	Ю	High-side gate drive voltage	Connect a 0.1-µF 16-V ceramic capacitor to VM.			
CONTROL							
AENBL	21	I	Bridge A enable	Logic high to enable bridge A			
APHASE	20	Į	Bridge A phase (direction)	Logic high sets AOUT1 high, AOUT2 low			
AI0	24	I	Pridge A current set	Sets bridge A current: 00 = 100%,			
Al1	25	1	Bridge A current set	01 = 71%, 10 = 38%, 11 = 0			
BENBL	22	I	Bridge B enable	Logic high to enable bridge B			
BPHASE	23	I	Bridge B phase (direction)	Logic high sets BOUT1 high, BOUT2 low			
BIO	26	Į	Bridge B current set	Sets bridge B current: 00 = 100%,			
BI1	27	I	Bridge B current set	01 = 71%, 10 = 38%, 11 = 0			
DECAY	19	I	Decay (brake) mode	Low = brake (slow decay), high = coast (fast decay)			
nRESET	16	I	Reset input	Active-low reset input initializes internal logic and disables the H-bridge outputs			
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode			
AVREF	12	Į	Bridge A current set reference input	Reference voltage for winding current set.			
BVREF	13	1	Bridge B current set reference input	Can be driven individually with an external DAC for microstepping, or tied to a reference (e.g., V3P3OUT).			
STATUS							
nFAULT	18	OD	Fault	Logic low when in fault condition (overtemp, overcurrent)			
OUTPUT							
ISENA	6	Ю	Bridge A ground / Isense	Connect to current sense resistor for bridge A			
ISENB	9	Ю	Bridge B ground / Isense	Connect to current sense resistor for bridge B			
AOUT1	5	0	Bridge A output 1	Connect to motor winding A			
AOUT2	7	0	Bridge A output 2	Connect to motor winding A			
BOUT1	10	0	Bridge B output 1	Connect to motor winding B			
BOUT2	8	0	Bridge B output 2	Connect to motor winding B			

⁽¹⁾ Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

Product Folder Link(s): DRV8814





ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) $^{(1)}$ $^{(2)}$

		VALUE	UNIT
VMx	Power supply voltage range	-0.3 to 47	V
	Digital pin voltage range	–0.5 to 7	V
VREF	Input voltage	-0.3 to 4	V
	ISENSEx pin voltage	-0.3 to 0.8	V
	Peak motor drive output current, t < 1 μS	Internally limited	А
	Continuous motor drive output current ⁽³⁾	2.5	Α
	Continuous total power dissipation	See Dissipation Ratin	igs table
TJ	Operating virtual junction temperature range	-40 to 150	°C
T _A	Operating ambient temperature range	-40 to 85	°C
T _{stg}	Storage temperature range	-60 to 150	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute—maximum—rated conditions for extended periods may affect device reliability.

⁽²⁾ All voltage values are with respect to network ground terminal.

⁽³⁾ Power dissipation and thermal limits must be observed.



THERMAL INFORMATION

		DRV8814	
	THERMAL METRIC ⁽¹⁾	PWP	UNITS
		28 PINS	
θ_{JA}	Junction-to-ambient thermal resistance (2)	31.6	
θ_{JCtop}	Junction-to-case (top) thermal resistance (3)	15.9	
θ_{JB}	Junction-to-board thermal resistance (4)	5.6	8000
Ψлт	Junction-to-top characterization parameter ⁽⁵⁾	0.2	°C/W
ΨЈВ	Junction-to-board characterization parameter ⁽⁶⁾	5.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	1.4	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT
V _M	Motor power supply voltage range ⁽¹⁾	8	45	V
V_{REF}	VREF input voltage (2)	1	3.5	V
I _{V3P3}	V3P3OUT load current	0	1	mA
f _{PWM}	Externally applied PWM frequency	0	100	kHz

- (1) All V_M pins must be connected to the same supply voltage.
- (2) Operational at VREF between 0 V and 1 V, but accuracy is degraded.



ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
POWER S	SUPPLIES						
l _{VM}	VM operating supply current	V _M = 24 V, f _{PWM} < 50 kHz		5	8	mA	
I_{VMQ}	VM sleep mode supply current	V _M = 24 V		10	20	μA	
V _{UVLO}	VM undervoltage lockout voltage	V _M rising		7.8	8.2	V	
V3P3OUT	REGULATOR				1		
V_{3P3}	V3P3OUT voltage	IOUT = 0 to 1 mA	3.2	3.3	3.4	V	
LOGIC-LE	EVEL INPUTS				"		
V _{IL}	Input low voltage			0.6	0.7	V	
V _{IH}	Input high voltage		2		5.25	V	
V _{HYS}	Input hysteresis		0.3	0.45	0.6	V	
I _{IL}	Input low current	VIN = 0	-20		20	μΑ	
l _{IH}	Input high current	VIN = 3.3 V		33	100	μΑ	
nFAULT (OUTPUT (OPEN-DRAIN OUTPUT)						
V _{OL}	Output low voltage	I _O = 5 mA			0.5	V	
I _{OH}	Output high leakage current	V _O = 3.3 V			1	μΑ	
DECAY IN							
V _{IL}	Input low threshold voltage	For slow decay (brake) mode	0		0.8	V	
V _{IH}	Input high threshold voltage	For fast decay (coast) mode	2			V	
I _{IN}	Input current	VIN = 0 V to 3.3 V			±40	μA	
H-BRIDG	E FETS				Į.		
n	110 557	V _M = 24 V, I _O = 1 A, T _J = 25°C		0.2			
$R_{DS(ON)}$	HS FET on resistance	V _M = 24 V, I _O = 1 A, T _J = 85°C		0.25	0.32	Ω	
_		V _M = 24 V, I _O = 1 A, T _J = 25°C		0.2			
$R_{DS(ON)}$	LS FET on resistance	V _M = 24 V, I _O = 1 A, T _J = 85°C		0.25	0.32	Ω	
l _{OFF}	Off-state leakage current		-20		20	μA	
MOTOR D	DRIVER						
f _{PWM}	Internal current control PWM frequency			50		kHz	
t _{BLANK}	Current sense blanking time			3.75		μs	
t _R	Rise time		50		300	ns	
t _F	Fall time		50		300	ns	
PROTECT	TION CIRCUITS						
I _{OCP}	Overcurrent protection trip level		3			Α	
t _{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C	
	T CONTROL						
I _{REF}	VREF input current	VREF = 3.3 V	-3		3	μΑ	
		xVREF = 3.3 V, 100% current setting	635	660	685		
V_{TRIP}	xISENSE trip voltage	xVREF = 3.3 V, 71% current setting	445	469	492	mV	
		xVREF = 3.3 V, 38% current setting	225	251	276		
	Current sense amplifier gain	Reference only		5		V/V	

Submit Documentation Feedback

Copyright © 2010–2011, Texas Instruments Incorporated



FUNCTIONAL DESCRIPTION

PWM Motor Drivers

The DRV8814 contains two H-bridge motor drivers with current-control PWM circuitry. A block diagram of the motor control circuitry is shown in Figure 1.

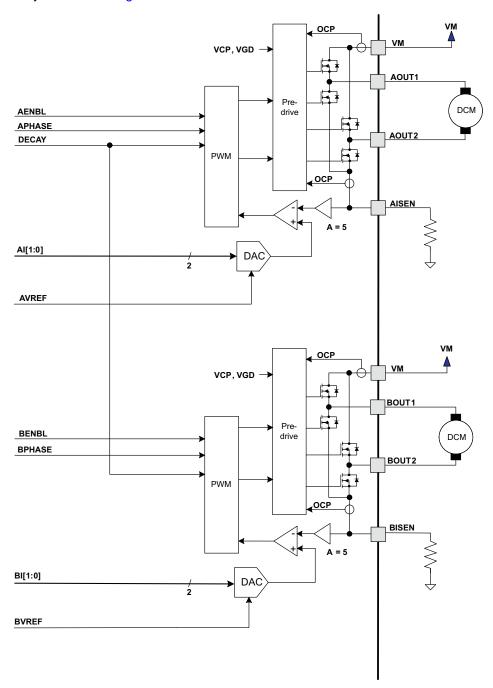


Figure 1. Motor Control Circuitry

Note that there are multiple VM pins. All VM pins must be connected together to the motor supply voltage.



Bridge Control

The xPHASE input pins control the direction of current flow through each H-bridge, and hence the direction of rotation of a DC motor. The xENBL input pins enable the H-bridge outputs when active high, and can also be used for PWM speed control of the motor. Note that the state of the DECAY pin selects the behavior of the bridge when xENBL = 0, allowing the selection of slow decay (brake) or fast decay (coast). Table 2 shows the logic.

Table 2. H-Bridge Logic

DECAY	xENBL	xPHASE	xOUT1	xOUT2
0	0	X	L	L
1	0	X	Z	Z
Х	1	1	Н	L
Х	1	0	L	Н

Current Regulation

The maximum current through the motor winding is regulated by a fixed-frequency PWM current regulation, or current chopping. When the H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

For DC motors, current regulation is used to limit the start-up and stall current of the motor. Speed control is typically performed by providing an external PWM signal to the ENBLx input pins.

If the current regulation feature is not needed, it can be disabled by connecting the xISENSE pins directly to ground, and connecting the xVREF pins to V3P3.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF pins, and is scaled by a 2-bit DAC that allows current settings of 100%, 71%, 38% of full-scale, plus zero.

The full-scale (100%) chopping current is calculated in Equation 1.

$$I_{CHOP} = \frac{V_{REFX}}{5 \cdot R_{ISENSE}} \tag{1}$$

Example:

If a $0.25-\Omega$ sense resistor is used and the VREFx pin is 2.5 V, the full-scale (100%) chopping current will be 2.5 V / (5 x 0.25Ω) = 2 A.

Two input pins per H-bridge (xl1 and xl0) are used to scale the current in each bridge as a percentage of the full-scale current set by the VREF input pin and sense resistance. The function of the pins is shown in Table 3.

Table 3. H-Bridge Pin Functions

xl1	xI0	RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)
1	1	0% (Bridge disabled)
1	0	38%
0	1	71%
0	0	100%

Note that when both xI bits are 1, the H-bridge is disabled and no current flows.

Example:

If a $0.25-\Omega$ sense resistor is used and the VREF pin is 2.5 V, the chopping current will be 2 A at the 100% setting (xI1, xI0 = 00). At the 71% setting (xI1, xI0 = 01) the current will be 2 A x 0.71 = 1.42 A, and at the 38% setting (xI1, xI0 = 10) the current will be 2 A x 0.38 = 0.76 A. If (xI1, xI0 = 11) the bridge will be disabled and no current will flow.



Decay Mode and Braking

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 2 as case 1. The current flow direction shown indicates the state when the xENBL pin is high.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 2 as case 2.

In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 2 as case 3.

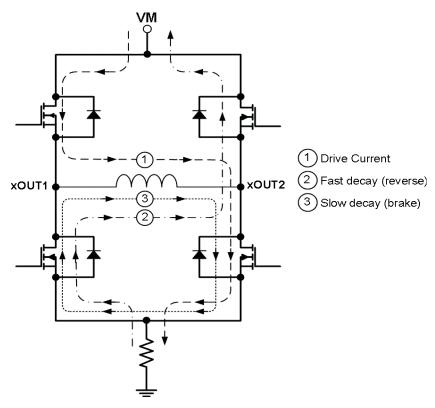


Figure 2. Decay Mode

The DRV8814 supports fast decay and slow decay mode. Slow or fast decay mode is selected by the state of the DECAY pin - logic low selects slow decay, and logic high sets fast decay mode. Note that the DECAY pin sets the decay mode for both H-bridges.

DECAY mode also affects the operation of the bridge when it is disabled (by taking the ENBL pin inactive). This applies if the ENABLE input is being used for PWM speed control of the motor, or if it is simply being used to start and stop motor rotation.

If the DECAY pin is high (fast decay), when the bridge is disabled fast decay mode will be entered until the current through the bridge reaches zero. Once the current is at zero, the bridge is disabled to prevent the motor from reversing direction. This allows the motor to coast to a stop.

If the DECAY pin is low (slow decay), both low-side FETs will be turned on when ENBL is made inactive. This essentially shorts out the back EMF of the motor, causing the motor to brake, and stop quickly. The low-side FETs will stay in the ON state even after the current reaches zero.



Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. Note that the blanking time also sets the minimum on time of the PWM.

nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge drivers. All inputs are ignored while nRESET is active.

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational.

Protection Circuits

The DRV8814 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The device will remain disabled until either nRESET pin is applied, or VM is removed and re-applied.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the I_{SENSE} resistor value or VREF voltage.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when V_M rises above the UVLO threshold.

dback Copyright © 2010–2011, Texas Instruments Incorporated

Product Folder Link(s): DRV8814



THERMAL INFORMATION

Thermal Protection

The DRV8814 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8814 is dominated by the power dissipated in the output FET resistance, or RDS(ON). Average power dissipation of each H-bridge when running a DC motor can be roughly estimated by Equation 2.

$$P = 2 \bullet R_{DS(ON)} \bullet (I_{OUT})^2 \tag{2}$$

where P is the power dissipation of one H-bridge, $R_{DS(ON)}$ is the resistance of each FET, and I_{OUT} is the RMS output current being applied to each winding. I_{OUT} is equal to the average current drawn by the DC motor. Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also need to be taken into consideration. The factor of 2 comes from the fact that at any instant two FETs are conducting winding current (one high-side and one low-side).

The total device dissipation will be the power dissipated in each of the two H-bridges added together.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, " PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, " PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

Copyright © 2010–2011, Texas Instruments Incorporated



PACKAGE OPTION ADDENDUM

28-Mar-2011

PACKAGING INFORMATION

www.ti.com

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
DRV8814PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DRV8814PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

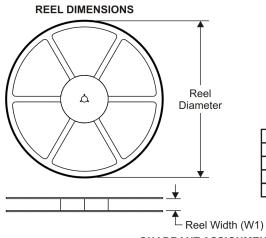
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

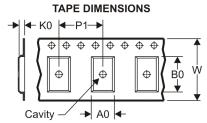
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 5-May-2011

TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8814PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

www.ti.com 5-May-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8814PWPR	HTSSOP	PWP	28	2000	346.0	346.0	33.0

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com www.ti.com.

 E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.



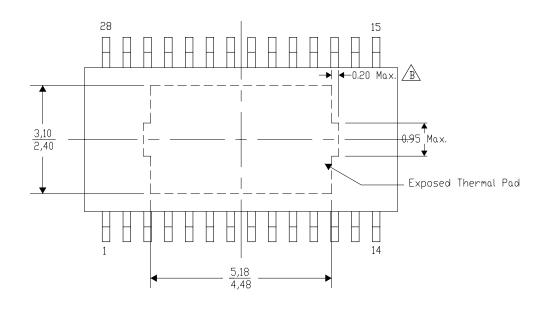
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD $^{\text{TM}}$ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-38/Y 10/11

NOTE: A. All linear dimensions are in millimeters

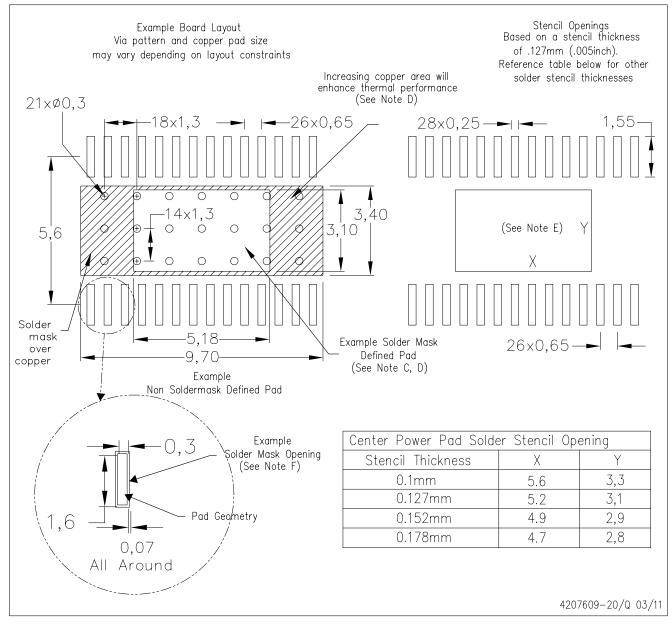
🛕 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments



PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
- E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products Applications

Audio www.ti.com/audio Communications and Telecom www.ti.com/communications **Amplifiers** amplifier.ti.com Computers and Peripherals www.ti.com/computers dataconverter.ti.com Consumer Electronics www.ti.com/consumer-apps **Data Converters DLP® Products** www.dlp.com **Energy and Lighting** www.ti.com/energy DSP dsp.ti.com Industrial www.ti.com/industrial Clocks and Timers www.ti.com/clocks Medical www.ti.com/medical Interface interface.ti.com Security www.ti.com/security

Logic Space, Avionics and Defense <u>www.ti.com/space-avionics-defense</u>

Power Mgmt power.ti.com Transportation and Automotive www.ti.com/automotive
Microcontrollers microcontroller.ti.com Video and Imaging www.ti.com/video

RFID <u>www.ti-rfid.com</u>
OMAP Mobile Processors www.ti.com/omap

Wireless Connectivity <u>www.ti.com/wirelessconnectivity</u>

TI E2E Community Home Page <u>e2e.ti.com</u>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated