# LM25066

*LM25066 System Power Management and Protection IC with PMBus*

Texas Instruments

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National Semiconductor

# LM25066

# System Power Management and Protection IC with PMBus™

## General Description

The LM25066 combines a high performance hot-swap controller with a PMBus™ compliant SMBus/I2C interface to accurately measure, protect and control the electrical operating conditions of computing and storage blades connected to a backplane power bus. The LM25066 continuously supplies real-time power, voltage, current, temperature and fault data to the system management host via the SMBus interface.

The LM25066 control block includes a unique hot-swap architecture that provides current and power limiting to protect sensitive circuitry during insertion of boards into a live system backplane, or any other "hot" power source. A fast acting circuit breaker prevents damage in the event of a short circuit on the output. The input under-voltage and over-voltage levels and hysteresis are configurable, as well as the insertion delay time and fault detection time. A temperature monitoring block on the LM25066 interfaces with a low-cost external diode for monitoring the temperature of the external MOSFET or other thermally sensitive components. The POWER GOOD output provides a fast indicator when the input and/or output voltages are outside their programmed range. LM25066 current measurement accuracy is ±2.4% over temperature.

The LM25066 monitoring block computes both the real-time and average values of subsystem operating parameters ($V_{IN}$, $I_{IN}$, $P_{IN}$, $V_{OUT}$) as well as the peak power. Accurate power averaging is accomplished by averaging the product of the input voltage and current. A black box (Telemetry/Fault Snapshot) function captures and stores telemetry data and device status in the event of a warning or a fault.

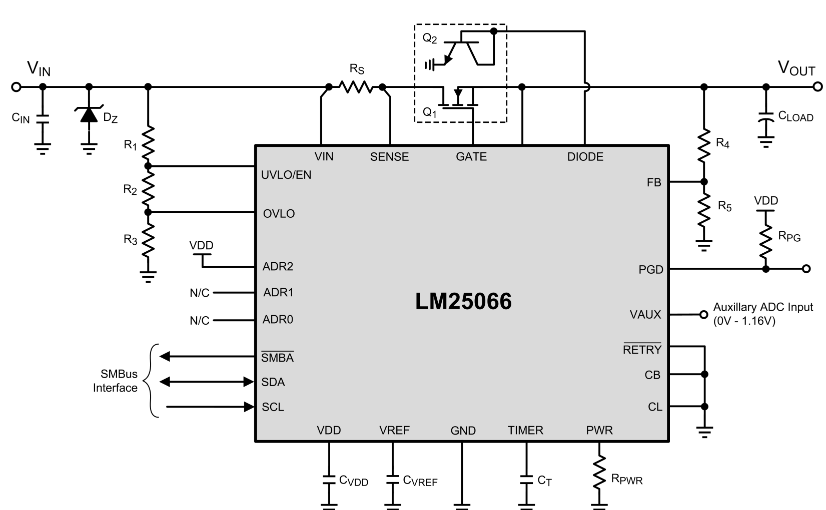
## Features

- Input voltage range: 2.9V to 17V
- I2C/SMBus interface and PMBus™ compliant command structure
- Programmable 25mV or 46mV current limit threshold
- Configurable circuit breaker protection for hard shorts
- Configurable under- and over-voltage lockouts with hysteresis
- Remote temperature sensing with programmable warning and shutdown thresholds
- Detection and notification of damaged MOSFET condition
- Real time monitoring of $V_{IN}$, $V_{OUT}$, $I_{IN}$, $P_{IN}$, $V_{AUX}$ with 12-bit resolution and 1 kHz sampling rate
- Current measurement accuracy: ±2.4% over temperature
- Power measurement accuracy: ±3.0% over temperature
- True input power measurement using simultaneous sampling of $V_{IN}$ and $I_{IN}$ accurately averages dynamic power readings
- Averaging of $V_{IN}$, $I_{IN}$, $P_{IN}$, and $V_{OUT}$ over programmable interval ranging from 0.001 to 4 seconds
- Programmable WARN and FAULT thresholds with $\overline{\text{SMBA}}$ notification
- Blackbox capture of telemetry measurements and device status triggered by WARN or FAULT condition
- Full-featured application design and development GUI
- 24-lead LLP package

## Applications

- Server backplane systems
- Basestation power distribution systems
- Solid state circuit breaker

## Typical Application Schematic

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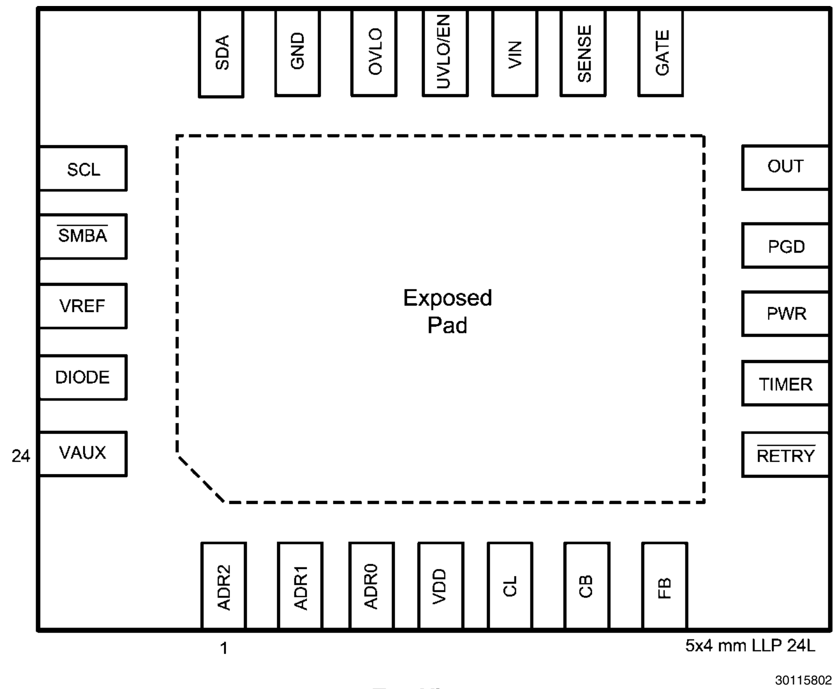
## Connection Diagram

Solder exposed pad to ground.




**Top View**
**LLP-24**

## Ordering Information

| Order Number | Package Type | Package Drawing | Supplied As |
|---|---|---|---|
| LM25066PSQ | LLP-24 | SQA24B | 1,000 units in tape and reel |
| LM25066PSQE | LLP-24 | SQA24B | 250 units in tape and reel |
| LM25066PSQX | LLP-24 | SQA24B | 4,500 units in tape and reel |

## Pin Descriptions

| Pin No. | Name | Description | Applications Information |
|---|---|---|---|
| Pad | Exposed Pad | Exposed pad of LLP package. | No internal electrical connections. Solder to the ground plane to reduce thermal resistance. |
| 1 | ADR2 | SMBUS address line 2 | 3 - state address line. Should be connected to GND, VDD, or left floating. |
| 2 | ADR1 | SMBUS address line 1 | 3 - state address line. Should be connected to GND, VDD, or left floating. |
| 3 | ADR0 | SMBUS address line 0 | 3 - state address line. Should be connected to GND, VDD, or left floating. |
| 4 | VDD | Internal sub-regulator output | Internally sub-regulated 4.5V bias supply. Connect a 1 µF capacitor on this pin to ground for bypassing. |
| 5 | CL | Current limit range | Connect this pin to GND to set the nominal over-current threshold at 25mV. Connecting CL to VDD will set the over-current threshold to be 46mV. |
| 6 | CB | Circuit breaker range | This pin sets the circuit breaker protection point in relation to the over-current trip point. When connected to GND, this pin will set the circuit breaker point to be 1.8 times the over-current threshold. Connecting this pin to VDD sets the circuit breaker trip point to be 3.6 times the over-current threshold. |
| 7 | FB | Power Good feedback | An external resistor divider from OUT sets the output voltage at which the PGD pin switches. The threshold at the pin is 1.167V. An internal 24 µA current source provides hysteresis. |
| 8 | $\overline{\text{RETRY}}$ | Fault retry input | This pin configures the power up fault retry behavior. When this pin is grounded, the device will continually try to engage power during a fault. If the pin is connected to VDD, the device will latch off during a fault. |
| 9 | TIMER | Timing capacitor | An external capacitor connected to this pin sets the insertion time delay, fault timeout period and restart timing. |
| 10 | PWR | Power limit set | An external resistor connected to this pin, in conjunction with the current sense resistor ($R_S$), sets the maximum power dissipation allowed in the external series pass MOSFET. |
| 11 | PGD | Power Good indicator | An open drain output. This output is high when the voltage at the FB pin is above 1.167V and the input supply is within its under-voltage and over-voltage thresholds. Connect via a pullup resistor to the output rail (external MOSFET source) or any other voltage to be monitored. |
| 12 | OUT | Output feedback | Connect to the output rail (external MOSFET source). Internally used to determine the MOSFET $V_{DS}$ voltage for power limiting, and to monitor the output voltage. |
| 13 | GATE | Gate drive output | Connect to the external MOSFET's gate. |
| 14 | SENSE | Current sense input | The voltage across the current sense resistor ($R_S$) is measured from VIN to this pin. If the voltage across $R_S$ reaches over-current threshold, the load current is limited and the fault timer activates. |
| 15 | VIN | Positive supply input | A small ceramic bypass capacitor close to this pin is recommended to suppress transients which occur when the load current is switched off. |
| 16 | UVLO/EN | Under-voltage lockout | An external resistor divider from the system input voltage sets the under-voltage turn-on threshold. An internal 23 µA current source provides hysteresis. The enable threshold at the pin is 1.16V. This pin can also be used for remote shutdown control. |
| 17 | OVLO | Over-voltage lockout | An external resistor divider from the system input voltage sets the over-voltage turn-off threshold. An internal 23 µA current source provides hysteresis. The disable threshold at the pin is 1.16V. |
| 18 | GND | Circuit ground | |
| 19 | SDA | SMBus data pin | Data pin for SMBus. |
| 20 | SCL | SMBus clock | Clock pin for SMBus. |
| 21 | $\overline{\text{SMBA}}$ | SMBus alert line | Alert pin for SMBus, active low. |
| 22 | VREF | Internal Reference | Internally generated precision 2.73V reference used for analog to digital conversion. Connect a 1 µF capacitor on this pin to ground for bypassing. |
| 23 | DIODE | External diode | Connect this to a diode-configured NPN transistor for temperature monitoring. |
| 24 | VAUX | Auxiliary voltage input | Auxiliary pin allows voltage telemetry from an external source. Full scale input of 1.16V. |

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| VIN, SENSE to GND (Note 6) | -0.3V to 24V |
| GATE, FB, UVLO/EN, OVLO, PGD, OUT to GND (Note 6) | -0.3V to 20V |
| SCL, SDA, SMBA, CL, CB, ADR0, ADR1, ADR2, VDD, VAUX, DIODE, RETRY to GND | -0.3V to 6V |
| VIN to SENSE | -0.3V to +0.3V |
| ESD Rating (Note 2) Human Body Model | 2kV |
| Storage Temperature | -65°C to +150°C |
| Junction Temperature | +150°C |

## Operating Ratings

| | |
|---|---|
| VIN, SENSE, OUT voltage | 2.9V to 17V |
| VDD | 2.9V to 5.5V |
| Junction Temperature | –40°C to +125°C |

## Electrical Characteristics

Limits in standard type are for $T_J$ = 25°C only; limits in boldface type apply over the junction temperature ($T_J$) range of -40°C to +85°C unless otherwise stated. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 12V. See (Note 3) and (Note 7).

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Input (VIN Pin)** | | | | | | |
| $I_{IN-EN}$ | Input Current, enabled | UVLO = 2V and OVLO = 0.7V | | 5.8 | **8** | mA |
| POR | Power On Reset threshold at VIN | VIN increasing | | 2.6 | **2.8** | V |
| $POR_{HYS}$ | $POR_{EN}$ Hysteresis | VIN decreasing | | 150 | | mV |
| **VDD Regulator (VDD pin)** | | | | | | |
| $V_{DD}$ | | $I_{VDD}$ = 5mA, VIN = 12V | **4.3** | 4.5 | **4.7** | V |
| | | $I_{VDD}$ = 5mA, VIN = 4.5V | **3.5** | 3.9 | **4.3** | V |
| $V_{DDILIM}$ | VDD Current Limit | | **25** | 45 | | mA |
| **UVLO/EN, OVLO Pins** | | | | | | |
| $UVLO_{TH}$ | UVLO threshold | $V_{UVLO}$ Falling | **1.147** | 1.16 | **1.173** | V |
| $UVLO_{HYS}$ | UVLO hysteresis current | UVLO = 1V | **18** | 23 | **28** | µA |
| $UVLO_{DEL}$ | UVLO delay | Delay to GATE high | | 8 | | µs |
| | | Delay to GATE low | | 20 | | |
| $UVLO_{BIAS}$ | UVLO bias current | UVLO = 3V | | | **1** | µA |
| $OVLO_{TH}$ | OVLO threshold | $V_{OVLO}$ rising | **1.141** | 1.16 | **1.185** | V |
| $OVLO_{HYS}$ | OVLO hysteresis current | OVLO = 1V | **-28** | -23 | **-18** | µA |
| $OVLO_{DEL}$ | OVLO delay | Delay to GATE high | | 19 | | µs |
| | | Delay to GATE low | | 9 | | |
| $OVLO_{BIAS}$ | OVLO bias current | OVLO = 1V | | | **1** | µA |
| **Power Good (PGD pin)** | | | | | | |
| $PGD_{VOL}$ | Output low voltage | $I_{SINK}$ = 2 mA | | 25 | **60** | mV |
| $PGD_{IOH}$ | Off leakage current | $V_{PGD}$ = 17V | | | **1** | µA |
| $PGD_{DELAY}$ | Power Good Delay | $V_{FB}$ to $V_{PG}$ | | 115 | | ns |
| **FB Pin** | | | | | | |
| $FB_{TH}$ | FB Threshold | $V_{FB}$ rising | **1.141** | 1.167 | **1.19** | V |
| $FB_{HYS}$ | FB Hysteresis Current | | **-31** | -24 | **-18** | µA |
| $FB_{LEAK}$ | Off Leakage Current | $V_{FB}$ = 1V | | | **1** | µA |
| **Power Limit (PWR Pin)** | | | | | | |
| $PWR_{LIM}$ | Power limit sense voltage (VIN-SENSE) | SENSE-OUT = 12V, $R_{PWR}$ = 25 kΩ | **9** | 12.5 | **15** | mV |
| $I_{PWR}$ | PWR pin current | $V_{PWR}$ = 2.5V | | -10 | | µA |
| $R_{SAT(PWR)}$ | PWR pin impedance when disabled | UVLO = 0.7V | | 180 | | Ω |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Gate Control (GATE Pin)** | | | | | | |
| $I_{GATE}$ | Source current | Normal operation | **-28** | -22 | **-16** | µA |
| | Fault Sink current | UVLO = 1V | **1.5** | 2 | **2.5** | mA |
| | POR Circuit Breaker sink current | VIN - SENSE = 150 mV or VIN < $R_{POR}$, $V_{GATE}$ = 5V | **105** | 190 | **275** | mA |
| $V_{GATE}$ | Gate output voltage in normal operation | GATE voltage with respect to ground | **17** | 18.8 | **20.3** | V |
| **OUT Pin** | | | | | | |
| $I_{OUT-EN}$ | OUT bias current, enabled | OUT = VIN, normal operation | | 16 | | µA |
| $I_{OUT-DIS}$ | OUT bias current, disabled (*Note 4*) | Disabled, OUT = 0V, SENSE = VIN | | -12 | | µA |
| **Current Limit** | | | | | | |
| $V_{CL}$ | Threshold voltage | CL = GND | **22.5** | 25 | **27** | mV |
| | | CL = GND, $T_J$ = 10°C to 85°C | **23** | 25 | **27** | |
| | | CL = VDD | **42.3** | 46 | **49.7** | |
| $t_{CL}$ | Response time | VIN-SENSE stepped from 0 mV to 80 mV | | 1.2 | | µs |
| $I_{SENSE}$ | SENSE input current | Enabled, SENSE = OUT | | 33 | | µA |
| | | Disabled, OUT = 0V | | 46 | | |
| | | Enabled, OUT = 0V | | 45 | | |
| **Circuit Breaker** | | | | | | |
| $V_{CB}$ | Threshold voltage x 1.8 | VIN - SENSE, CL = GND, CB = GND | **35** | 45 | **55** | mV |
| | CB:CL Ratio | CB = GND | **1.6** | 1.8 | **2** | |
| $V_{CB}$ | Threshold voltage x 3.6 | VIN - SENSE, CL = GND, CB = VDD | **70** | 90 | **110** | mV |
| | CB:CL Ratio | CB = VDD | **3.1** | 3.6 | **4** | |
| $t_{CB}$ | Response time | VIN - SENSE stepped from 0 mV to 150 mV, time to GATE low, no load | | 0.6 | **1.2** | µs |
| **Timer (TIMER pin)** | | | | | | |
| $V_{TMRH}$ | Upper threshold | | **1.54** | 1.7 | **1.85** | V |
| $V_{TMRL}$ | Lower threshold | Restart cycles | **0.85** | 1.0 | **1.07** | V |
| | | End of 8th cycle | | 0.3 | | V |
| | | Re-enable threshold | | 0.3 | | V |
| $I_{TIMER}$ | Insertion time current | TIMER pin = 2V | **-3** | -5.5 | **-8** | µA |
| | Sink current, end of insertion time | | **1.4** | 1.9 | **2.4** | mA |
| | Fault detection current | | **-120** | -90 | **-60** | µA |
| | Fault sink current | | | 2.8 | | µA |
| $DC_{FAULT}$ | Fault Restart Duty Cycle | | | 0.67 | | % |
| $t_{FAULT\_DELAY}$ | Fault to GATE low delay | TIMER pin reaches the upper threshold | | 17 | | µs |
| **Internal Reference** | | | | | | |
| $V_{REF}$ | Reference Voltage | | **2.703** | 2.73 | **2.757** | V |
| **ADC and MUX** | | | | | | |
| | Resolution | | | 12 | | Bits |
| INL | Integral Non-Linearity | ADC only | | +/-1 | | LSB |
| $t_{AQUIRE}$ | Acquisition + Conversion Time | Any channel | | 100 | | µs |
| $t_{RR}$ | Acquisition Round Robin Time | Cycle all channels | | 1 | | ms |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Telemetry Accuracy** | | | | | | |
| $IIN_{FSR}$ | Current input full scale range | CL = GND | | 30.2 | | mV |
| | | CL = VDD | | 60.4 | | mV |
| $IIN_{LSB}$ | Current input LSB | CL = GND | | 7.32 | | µV |
| | | CL = VDD | | 14.64 | | µV |
| $VAUX_{FSR}$ | VAUX input full scale range | | | 1.16 | | V |
| $VAUX_{LSB}$ | VAUX input LSB | | | 283.2 | | µV |
| $VIN_{FSR}$ | Input voltage full scale range | | | 18.7 | | V |
| $VIN_{LSB}$ | Input voltage LSB | | | 4.54 | | mV |
| $IIN_{ACC}$ | Input Current Accuracy | VIN – SENSE = 25mV, CL = GND | **-2.7** | | **+2.4** | % |
| | | VIN – SENSE = 25mV, CL = GND<br>$T_J$ = 10°C to 85°C | **-2.4** | | **+2.4** | |
| $V_{ACC}$ | VAUX, VIN, VOUT Accuracy | VIN, VOUT = 12V<br>VAUX = 1V | **-1.6** | | **+1.4** | % |
| | | VIN, VOUT = 12V<br>VAUX = 1V<br>$T_J$ = 10°C to 85°C | **-1.4** | | **+1.4** | |
| $PIN_{ACC}$ | Input Power Accuracy | VIN = 12V, VIN – SENSE = 25mV, CL = GND | **-3.0** | | **+3.0** | % |
| **Remote Diode Temperature Sensor** | | | | | | |
| $T_{ACC}$ | Temperature Accuracy Using Local Diode | $T_A$ = 10°C to 85°C | | 2 | **10** | °C |
| | Remote Diode Resolution | | | 9 | | bits |
| $I_{DIODE}$ | External Diode Current Source | High level | | 250 | **300** | µA |
| | | Low level | | 9.4 | | µA |
| | Diode Current Ratio | | | 26 | | |
| **PMBus Pin Thresholds ($\overline{SMBA}$, SDA, SCL)** | | | | | | |
| $V_{IL}$ | Data, Clock Input Low Voltage | | | | **0.8** | V |
| $V_{IH}$ | Data, Clock Input High Voltage | | **2.1** | | **5.5** | V |
| $V_{OL}$ | Data Output Low Voltage | $I_{PULLUP}$ = 500 µA | **0** | | **0.4** | V |
| $I_{LEAK}$ | Input Leakage Current | SDA, $\overline{SMBA}$, SCL = 5V | | | **1** | µA |
| **Configuration Pin Thresholds (CB, CL, $\overline{RETRY}$)** | | | | | | |
| $V_{IH}$ | Threshold Voltage | | **3** | | | V |
| $I_{LEAK}$ | Input Leakage Current | CL, CB, $\overline{RETRY}$ = 5V | | | **1** | mA |
| **Thermal** (*Note 5*) | | | | | | |
| $\theta_{JA}$ | Junction to Ambient | | | 42.3 | | °C/W |
| $\theta_{JC}$ | Junction to Case | | | 9.5 | | °C/W |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and conditions see the Electrical Characteristics.

**Note 2:** The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

**Note 3:** Current out of a pin is indicated as a negative value.

**Note 4:** OUT bias current (disabled) due to leakage current through an internal 0.9 MΩ resistance from SENSE to VOUT.

**Note 5:** Junction-to-ambient thermal resistance is highly application and board layout dependent. Specified thermal resistance values for the package specified is based on a 4-layer, 4"x3", 2/1/1/2 oz. Cu board as per JEDEC standards is used.

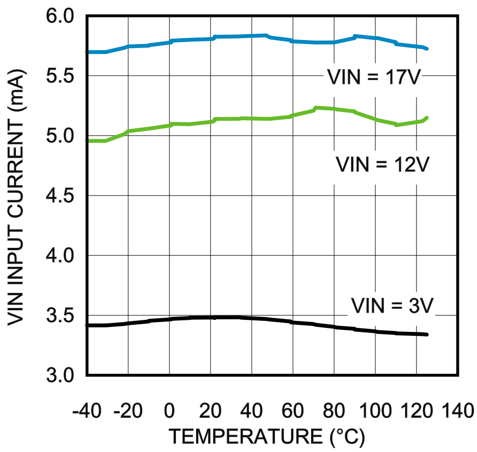
**Note 6:** The GATE pin voltage is typically 7.5V above VIN when the LM25066 is enabled. Therefore, the Absolute Maximum Rating of 24V for VIN and SENSE apply only when the LM25066 is disabled or for a momentary surge to that voltage since the Absolute Maximum Rating for the GATE pin is 20V.

**Note 7:** All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production at $T_A$ = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

## Typical Performance Characteristics

Unless otherwise specified the following conditions apply: $T_J$ = 25°C, $V_{IN}$ = 12V. All graphs show junction temperature.

**VIN Pin Current**

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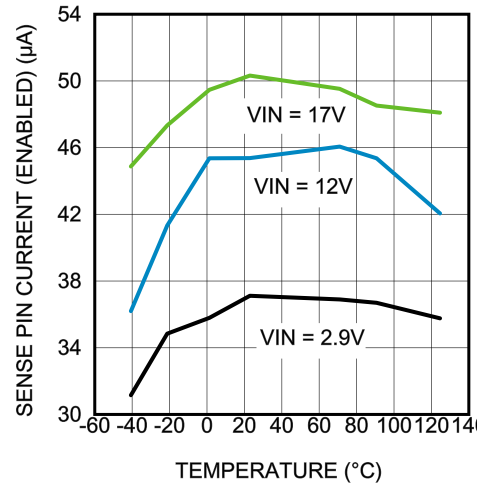
**SENSE Pin Current (Enabled)**

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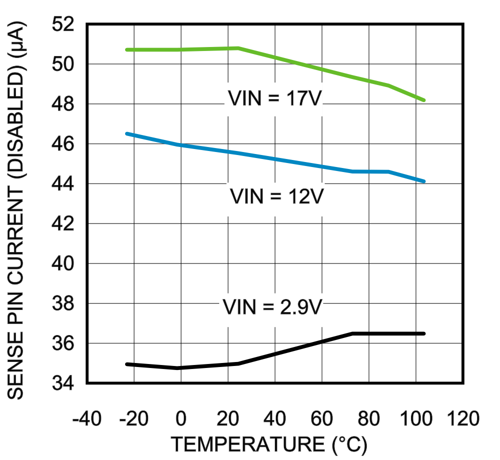
**SENSE Pin Current (Disabled)**

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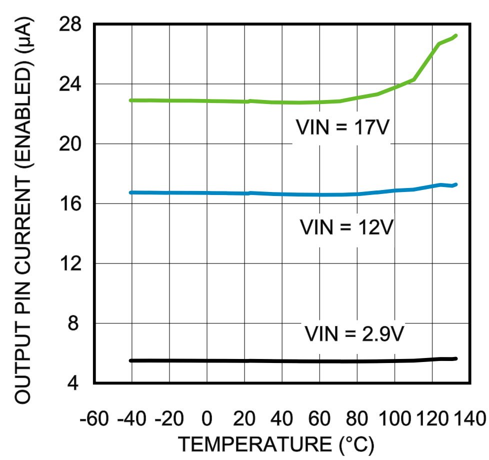
**OUT Pin Current (Enabled)**

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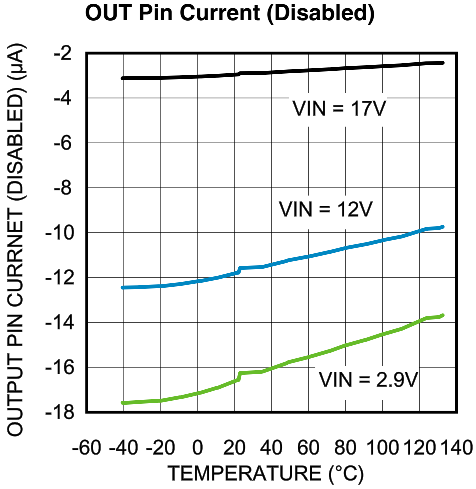
**OUT Pin Current (Disabled)**

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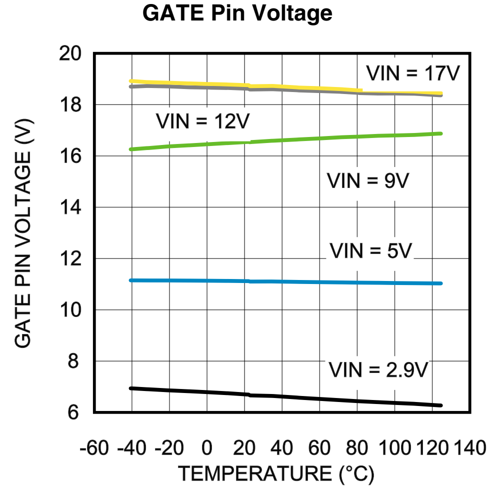
**GATE Pin Voltage**

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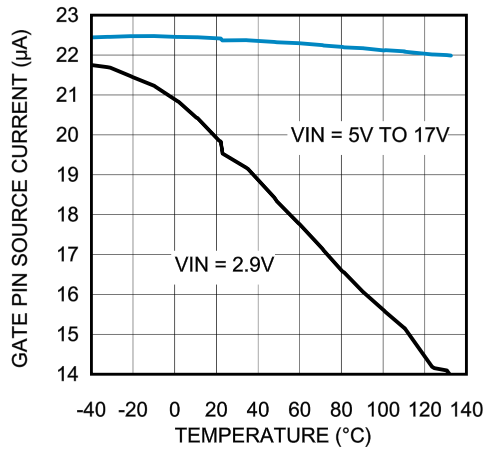
**GATE Pin Source Current**

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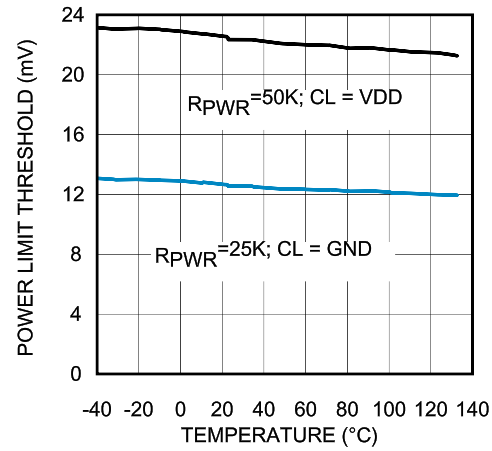
**Power Limit Threshold**

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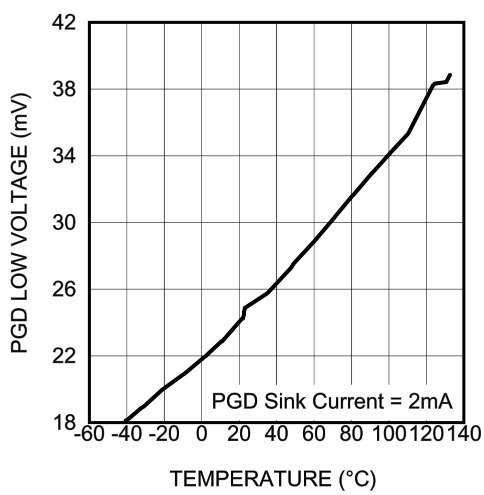
**PGD Low Voltage**

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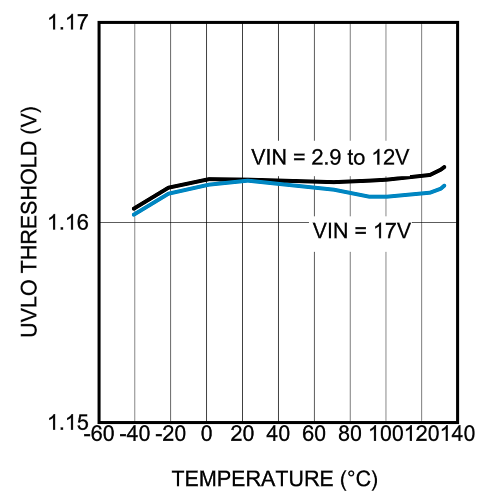
**UVLO Threshold**

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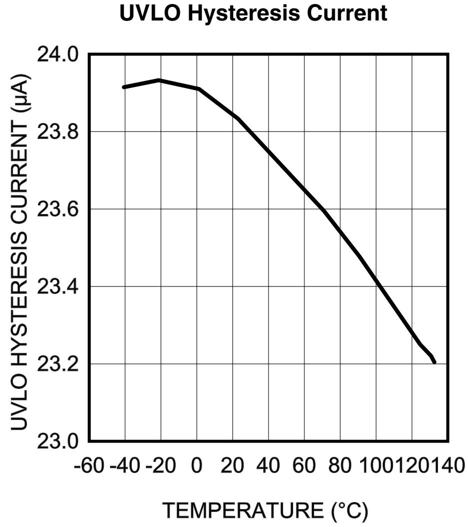
**UVLO Hysteresis Current**

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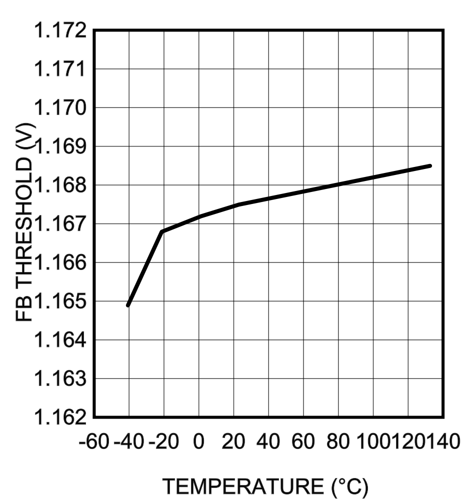
**FB Threshold**

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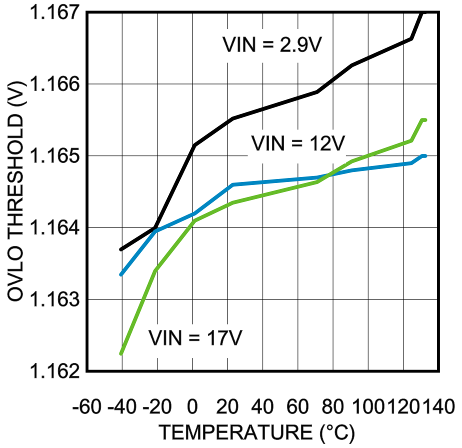
**OVLO Threshold**

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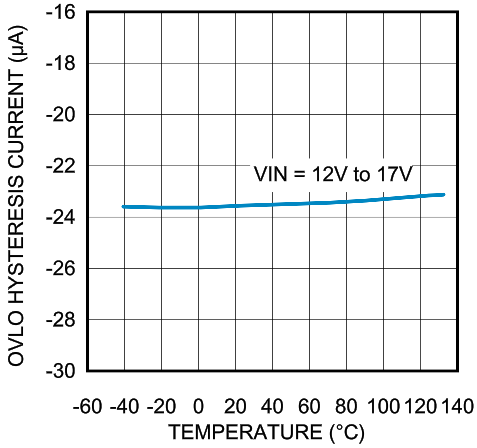
**OVLO Hysteresis**

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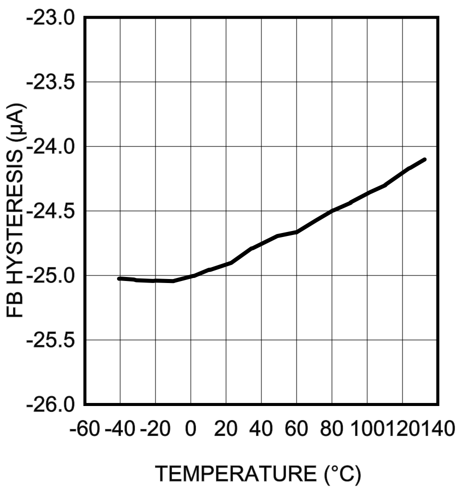
**FB Pin Hysteresis**

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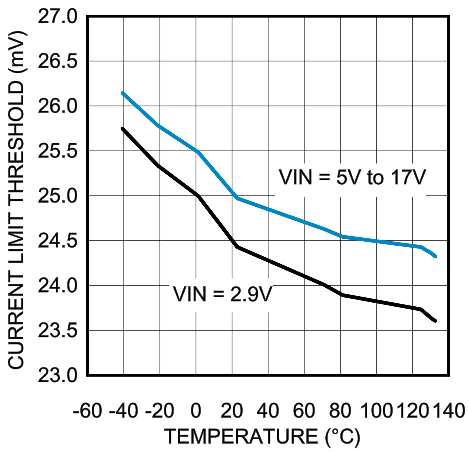
**Current Limit Threshold**

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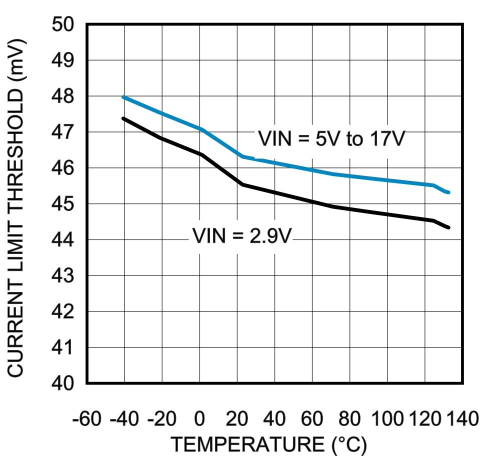
**Current Limit Threshold**

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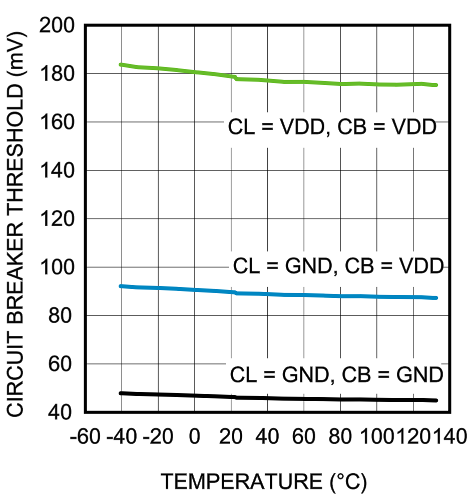
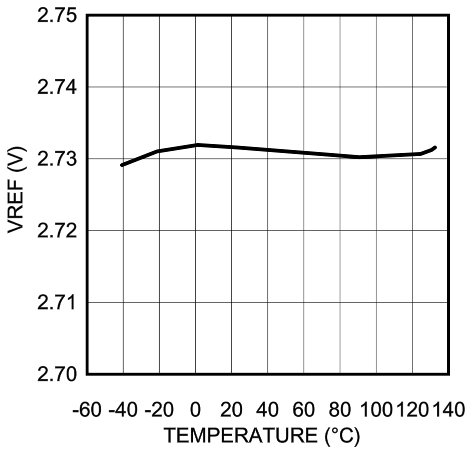
**Circuit Breaker Threshold (CL = VDD)**



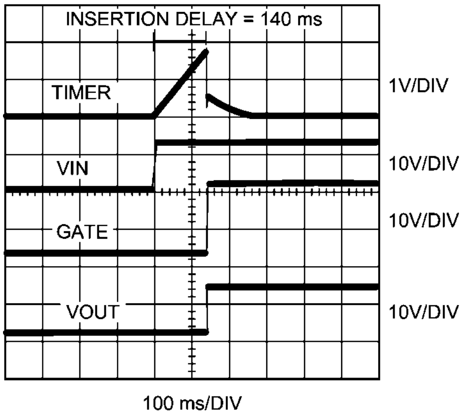

30115888

**Reference Voltage**



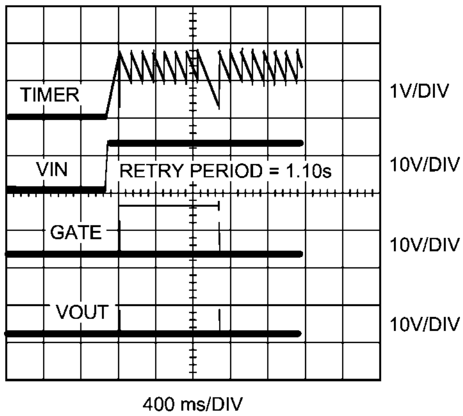

30115890

**Startup (Insertion Delay)**



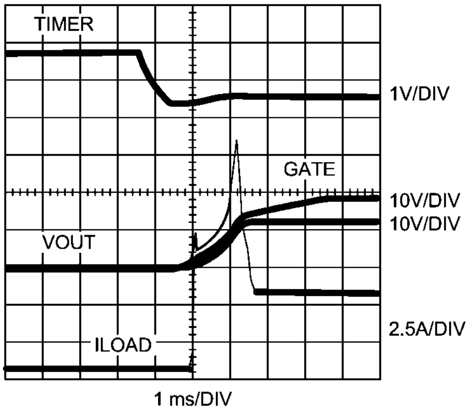

30115891

**Startup (Short circuit $V_{OUT}$)**



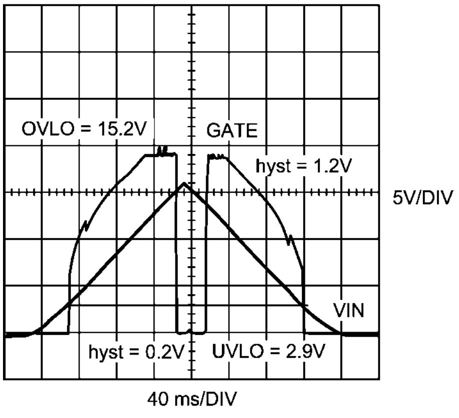

30115892

**Startup (5A Load)**



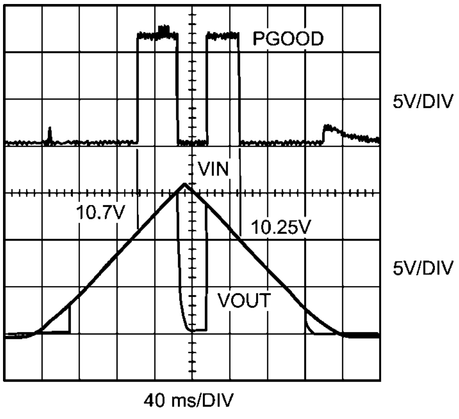

30115893

**Startup (UVLO, OVLO)**



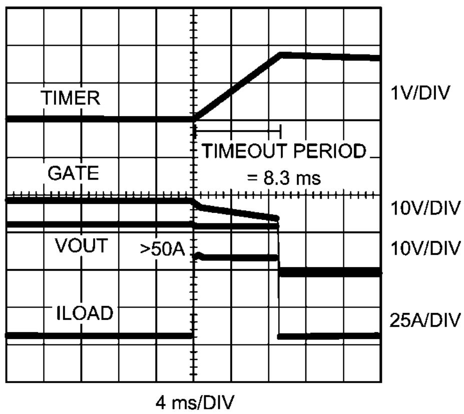

30115894

**Startup (PGOOD)**



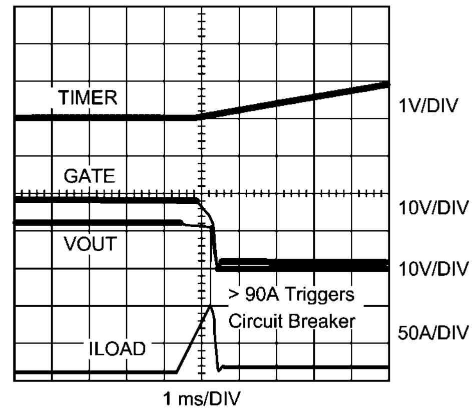

30115895

**Current Limit Event (CL = GND)**



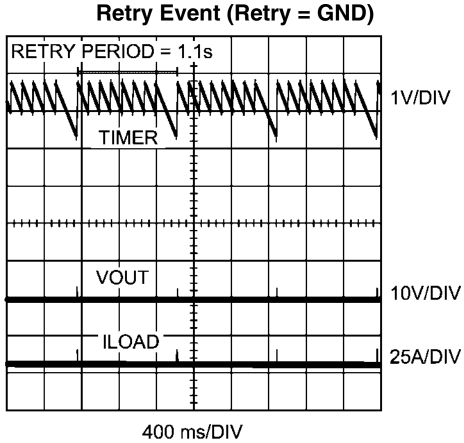

30115896

**Circuit Breaker Event (CL = CB = GND)**



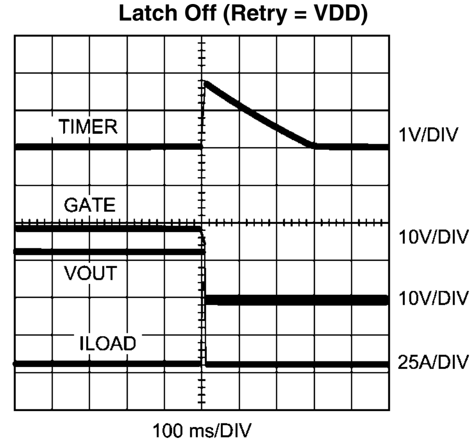

30115897

**Retry Event (Retry = GND)**



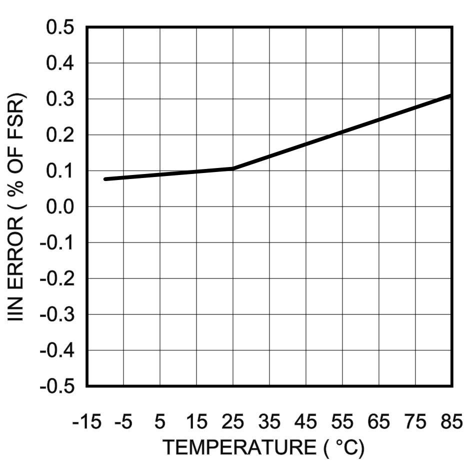

30115898

**Latch Off (Retry = VDD)**



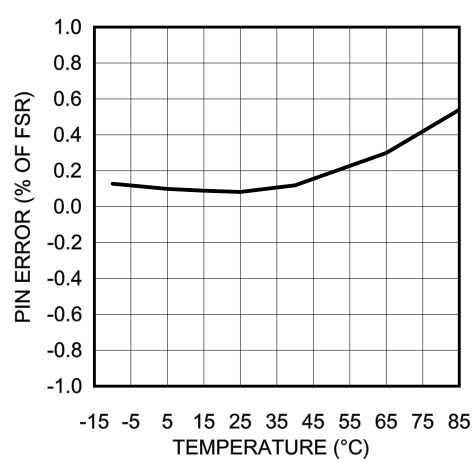

30115899

**IIN Measurement Accuracy (VIN - SENSE = 25 mV)**



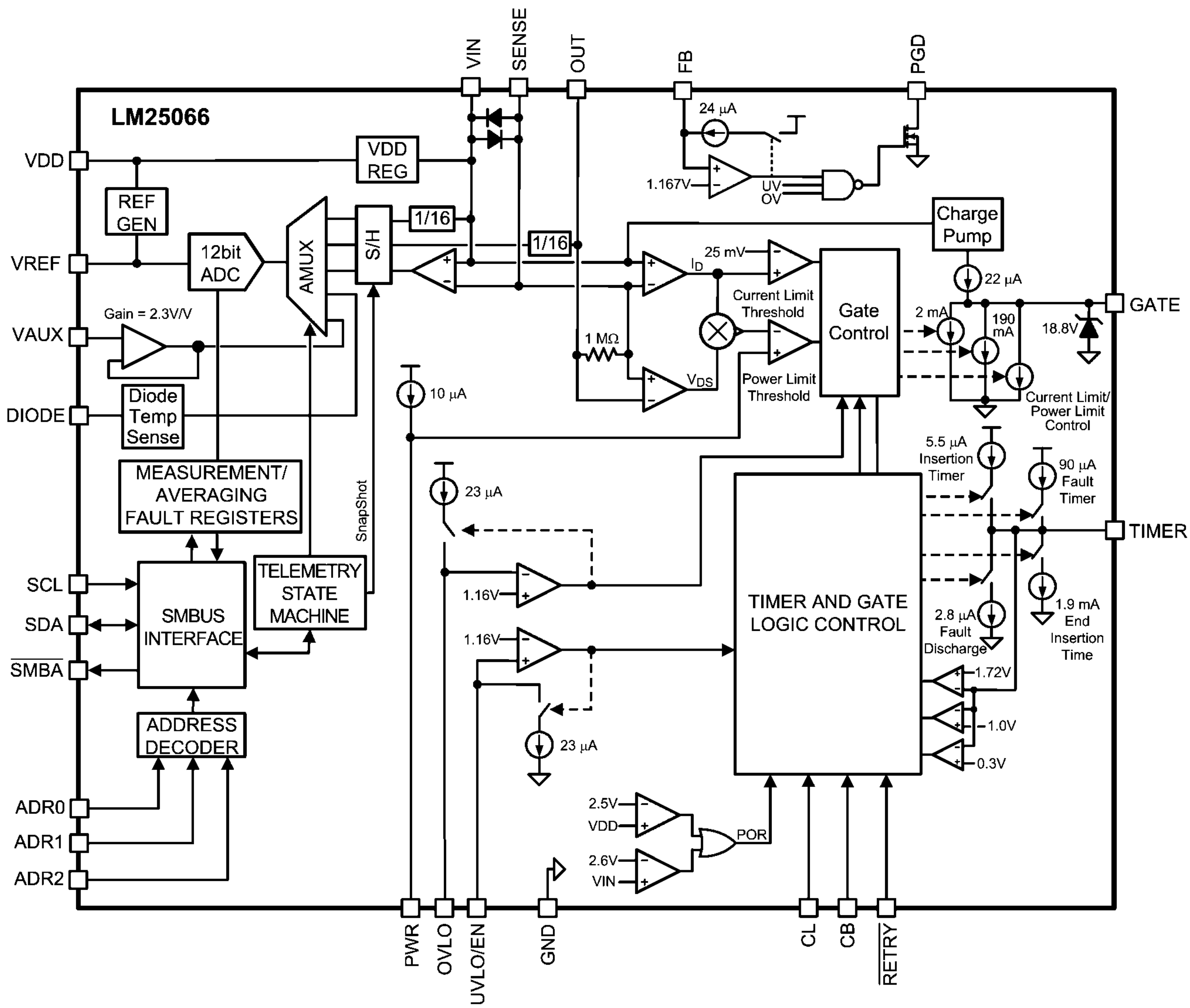

301158a8

**PIN Measurement Accuracy (VIN - SENSE = 25 mV)**




301158a9

## Block Diagram




30115810

## Functional Description

The inline protection functionality of the LM25066 is designed to control the in-rush current to the load upon insertion of a circuit card into a live backplane or other "hot" power source, thereby limiting the voltage sag on the backplane's supply voltage and the dV/dt of the voltage applied to the load. Effects on other circuits in the system are minimized, preventing possible unintended resets. A controlled shutdown when the circuit card is removed can also be implemented using the LM25066.

In addition to a programmable current limit, the LM25066 monitors and limits the maximum power dissipation in the series pass device to maintain operation within the device Safe Operating Area (SOA). Either current limiting or power limiting for an extended period of time results in the shutdown of the series pass device. In this event, the LM25066 can latch off or repetitively retry based on the hardware setting of the RETRY pin. Once started, the number of retries can be set to none, 1, 2, 4, 8, 16, or infinite. The circuit breaker function quickly switches off the series pass device upon detection of a severe over-current condition. Programmable under-voltage lockout (UVLO) and over-voltage lockout (OVLO) circuits shut down the LM25066 when the system input voltage is outside the desired operating range.

The telemetry capability of the LM25066 provides intelligent monitoring of the input voltage, output voltage, input current, input power, temperature, and an auxiliary input. The LM25066 also provides a peak capture of the input power and programmable hardware averaging of the input voltage, current, power, and output voltage. Warning thresholds which trigger the SMBA pin may be programmed for input and output voltage, current, power and temperature via the PMBus interface. Additionally, the LM25066 is capable of detecting damage to the external MOSFET, $Q_1$.

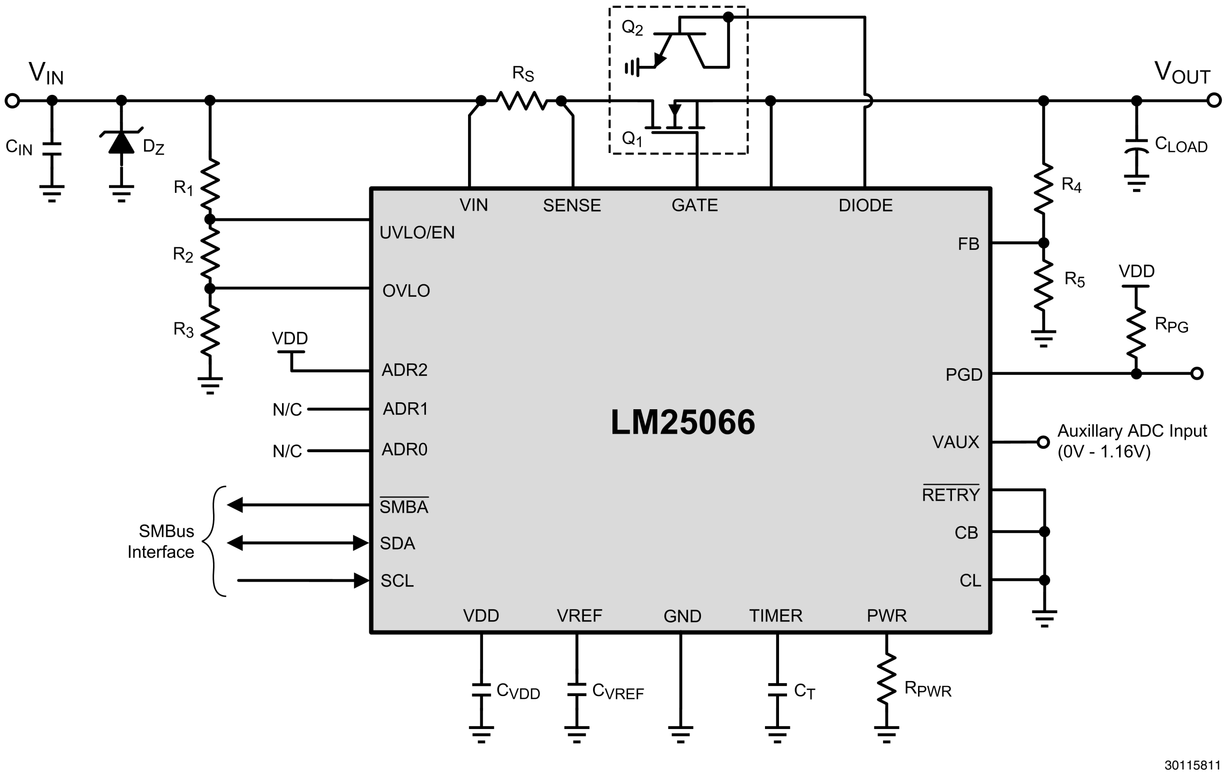



**FIGURE 1. Typical Application Circuit**

## Power Up Sequence

The VIN operating range of the LM25066 is +2.9V to +17V, with transient capability to +24V. Referring to *Figure 1* and *Figure 2*, as the voltage at VIN initially increases, the external N-channel MOSFET ($Q_1$) is held off by an internal 190 mA pull-down current at the GATE pin. The strong pull-down current at the GATE pin prevents an inadvertent turn-on as the MOSFET's gate-to-drain (Miller) capacitance is charged. Additionally, the TIMER pin is initially held at ground. When the $V_{IN}$ voltage reaches the POR threshold, the insertion time begins. During the insertion time, the capacitor at the TIMER pin ($C_T$) is charged by a 5.5 µA current source and $Q_1$ is held off by a 2 mA pull-down current at the GATE pin regardless of the input voltage. The insertion time delay allows ringing and transients at VIN to settle before $Q_1$ is enabled. The insertion time ends when the TIMER pin voltage reaches 1.7V. $C_T$ is then quickly discharged by an internal 1.9 mA pull-down current. The GATE pin then switches on $Q_1$ when $V_{SYS}$, the input supply voltage, exceeds the UVLO threshold. If $V_{SYS}$ is above the UVLO threshold at the end of the insertion time, $Q_1$ switches on at that time. The GATE pin charge pump sources 22 µA to charge the gate capacitance of $Q_1$. The maximum voltage at the GATE pin with respect to ground is limited by an internal 18.8V zener diode.

As the voltage at the OUT pin increases, the LM25066 monitors the drain current and power dissipation of MOSFET $Q_1$. Inrush current limiting and/or power limiting circuits actively control the current delivered to the load. During the inrush limiting interval ($t_2$ in *Figure 2*), an internal 90 µA fault timer current source charges $C_T$. If $Q_1$'s power dissipation and the input current reduce below their respective limiting thresholds before the TIMER pin reaches 1.7V, the 90 µA current source is switched off and $C_T$ is discharged by the internal 2.8 µA current sink ($t_3$ in *Figure 2*). The PGD pin switches high when FB exceeds its rising threshold of 1.167V.

If the TIMER pin voltage reaches 1.7V before inrush current limiting or power limiting ceases during $t_2$, a fault is declared and $Q_1$ is turned off. See the Fault Timer & Restart section for a complete description of the fault mode.

The LM25066 will pull the $\overline{\text{SMBA}}$ pin low after the input voltage has exceeded its POR threshold to indicate that the volatile memory and device settings are in their default state. The CONFIG_PRESET bit within the STATUS_MFR_SPECIFIC register (80h) indicates default configuration of warning thresholds and device operation and will remain set until a CLEAR_FAULTS command is received.

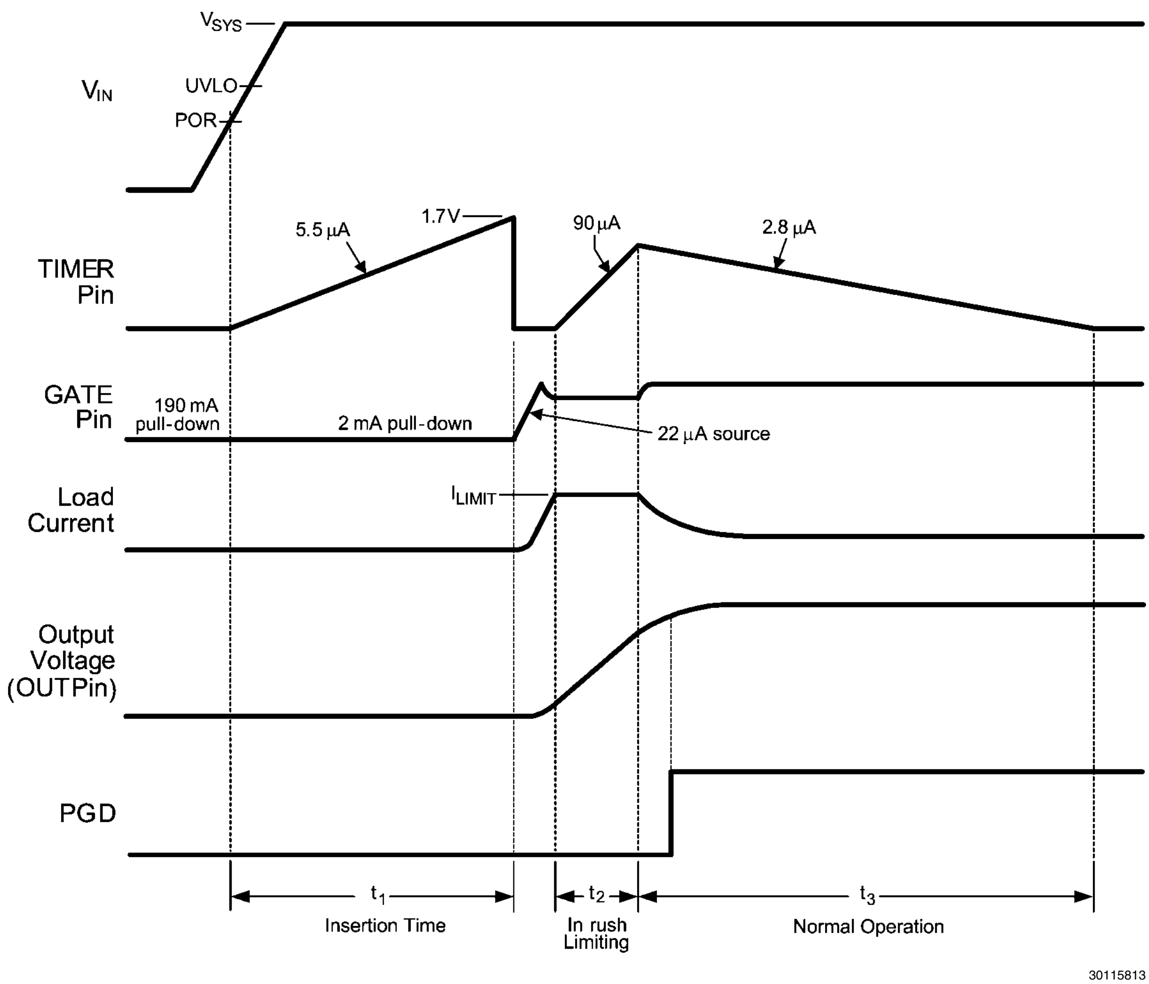



**FIGURE 2. Power Up Sequence (Current Limit Only)**

## Gate Control

A charge pump provides the voltage at the GATE pin to enhance the N-Channel MOSFET's gate. During normal operating conditions ($t_3$ in *Figure 2*) the gate of $Q_1$ is held charged by an internal 22 µA current source. The voltage at the GATE pin (with respect to ground) is limited by an internal 18.8 V zener diode. See the graph "GATE Pin Voltage" shown previously. Since the gate-to-source voltage applied to $Q_1$ could be as high as 18.8 V during various conditions, a zener diode with the appropriate voltage rating must be added between the GATE and OUT pins if the maximum $V_{GS}$ rating of the selected MOSFET is less than 18.8 V. The external zener diode must have a forward current rating of at least 190 mA. When the system voltage is initially applied, the GATE pin is held low by a 190 mA pull-down current. This helps prevent an inadvertent turn-on of the MOSFET through its drain-gate capacitance as the applied system voltage increases.

During the insertion time ($t_1$ in *Figure 2*) the GATE pin is held low by a 2 mA pull-down current. This maintains $Q_1$ in the off-state until the end of $t_1$, regardless of the voltage at VIN or UVLO. Following the insertion time ($t_2$ in *Figure 2*), the gate voltage of $Q_1$ is controlled to keep the current or power dissipation level from exceeding the programmed levels. While in the current or power limiting mode, the TIMER pin capacitor is charging. If the current and power limiting cease before the TIMER pin reaches 1.7V, the TIMER pin capacitor then discharges, and the circuit begins normal operation. If the inrush limiting condition persists such that the TIMER pin reached 1.7V during $t_2$, the GATE pin is then pulled low by the 190 mA pull-down current. The GATE pin is then held low until either a power up sequence is initiated ($\overline{\text{RETRY}}$ pin to VDD), or an automatic retry is attempted ($\overline{\text{RETRY}}$ pin to GROUND). See the Fault Timer & Restart section. If the system input voltage falls below the UVLO threshold or rises above the OVLO threshold, the GATE pin is pulled low by the 2 mA pull-down current to switch off $Q_1$.

## Current Limit

The current limit threshold is reached when the voltage across the sense resistor $R_S$ (VIN to SENSE) exceeds the internal voltage limit of 25 mV or 46 mV depending on whether the CL pin is connected to GND or VDD, respectively. In the current limiting condition, the GATE voltage is controlled to limit the current in MOSFET $Q_1$. While the current limit circuit is active, the fault timer is active as described in the Fault Timer & Restart section. If the load current falls below the current limit threshold before the end of the Fault Timeout Period, the LM25066 resumes normal operation. If the current limit condition persists for longer than the Fault Timeout Period set by the timer capacitor, $C_T$, the IIN OC FAULT bit in the

STATUS_INPUT (7Ch) register, the INPUT bit in the STATUS_WORD (79h) register, and the IIN_OC/PFET_OP_FAULT bit in the DIAGNOSTIC_WORD (E1h) register will be toggled high and SMBA pin will be pulled low unless this feature is disabled using the ALERT_MASK (D8h) register. For proper operation, the $R_S$ resistor value should be less than 200 mΩ. Higher values may create instability in the current limit control loop. The current limit threshold pin value may be overridden by setting appropriate bits in the DEVICE_SETUP register (D9h).

## Circuit Breaker

If the load current increases rapidly (e.g. the load is short circuited), the current in the sense resistor ($R_S$) may exceed the current limit threshold before the current limit control loop is able to respond. If the current exceeds 1.8 or 3.6 times (user settable) the current limit threshold, $Q_1$ is quickly switched off by the 190 mA pull-down current at the GATE pin, and a Fault Timeout Period begins. When the voltage across $R_S$ falls below the threshold the 190 mA pull-down current at the GATE pin is switched off and the gate voltage of $Q_1$ is then determined by the current limit or power limit functions. If the TIMER pin reaches 1.7V before the current limiting or power limiting condition ceases, $Q_1$ is switched off by the 2 mA pull-down current at the GATE pin as described in the Fault Timer & Restart section. A circuit breaker event will cause the CIRCUIT BREAKER FAULT bit in the STATUS_MFR_SPECIFIC (80h) and DIAGNOSTIC_WORD (E1h) registers to be toggled high and SMBA pin will be pulled low unless this feature is disabled using the ALERT_MASK (D8h) register. The circuit breaker pin configuration may be overridden by setting appropriate bits in the DEVICE_SETUP (D9h) register.

## Power Limit

An important feature of the LM25066 is the MOSFET power limiting. The Power Limit function can be used to maintain the maximum power dissipation of MOSFET $Q_1$ within the device SOA rating. The LM25066 determines the power dissipation in $Q_1$ by monitoring its drain-source voltage (SENSE to OUT), and the drain current through $R_S$ (VIN to SENSE). The product of the current and voltage is compared to the power limit threshold programmed by the resistor at the PWR pin. If the power dissipation reaches the limiting threshold, the GATE voltage is controlled to regulate the current in $Q_1$. While the power limiting circuit is active, the fault timer is active as described in the Fault Timer & Restart section. If the power limit condition persists for longer than the Fault Timeout Period set by the timer capacitor, $C_T$, the IIN_OC_FAULT bit in the STATUS_INPUT (7Ch) register, the INPUT bit in the STATUS_WORD (79h) register, and the IIN_OC/PFET_OP_FAULT bit in the DIAGNOSTIC_WORD (E1h) register will be toggled high and SMBA pin will be pulled low unless this feature is disabled using the ALERT_MASK (D8h) register.

## Fault Timer & Restart

When the current limit or power limit threshold is reached during turn-on, or as a result of a fault condition, the gate-to-source voltage of $Q_1$ is controlled to regulate the load current and power dissipation in $Q_1$. When either limiting function is active, a 90 µA fault timer current source charges the external capacitor ($C_T$) at the TIMER pin as shown in *Figure 2* (Fault Timeout Period). If the fault condition subsides during the Fault Timeout Period before the TIMER pin reaches 1.7V, the LM25066 returns to the normal operating mode and $C_T$ is discharged by the 1.9 mA current sink. If the TIMER pin reaches 1.7V during the Fault Timeout Period, $Q_1$ is switched off by a 2 mA pull-down current at the GATE pin. The subsequent restart procedure then depends on the selected retry configuration.

If the RETRY pin is high, the LM25066 latches the GATE pin low at the end of the Fault Timeout Period. $C_T$ is then discharged to ground by the 2.8 µA fault current sink. The GATE pin is held low by the 2 mA pull-down current until a power up sequence is externally initiated by cycling the input voltage ($V_{SYS}$), or momentarily pulling the UVLO/EN pin below its threshold with an open-collector or open-drain device as shown in *Figure 3*. The voltage at the TIMER pin must be <0.3V for the restart procedure to be effective. The TIMER_LATCHED_OFF bit in the DIAGNOSTIC_WORD (E1h) register will remain high while the latched off condition persists.

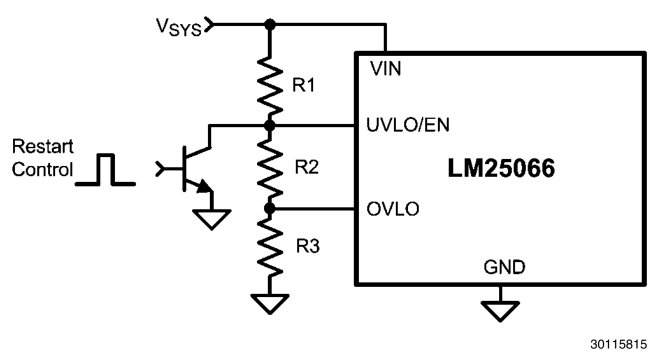



**FIGURE 3. Latched Fault Restart Control**

The LM25066 provides an automatic restart sequence which consists of the TIMER pin cycling between 1.7V and 1V seven times after the Fault Timeout Period, as shown in *Figure 4*. The period of each cycle is determined by the 90 µA charging current, and the 2.8 µA discharge current, and the value of the capacitor $C_T$. When the TIMER pin reaches 0.3V during the eighth high-to-low ramp, the 22 µA current source at the GATE pin turns on $Q_1$. If the fault condition is still present, the Fault Timeout Period and the restart sequence repeat. The RETRY pin allows selecting no retries or infinite retries. Finer control of the retry behavior can be achieved through the DEVICE_SETUP (D9h) register. Retry counts of 0, 1, 2, 4, 8, 16 or infinite may be selected by setting the appropriate bits in the DEVICE_SETUP (D9h) register.

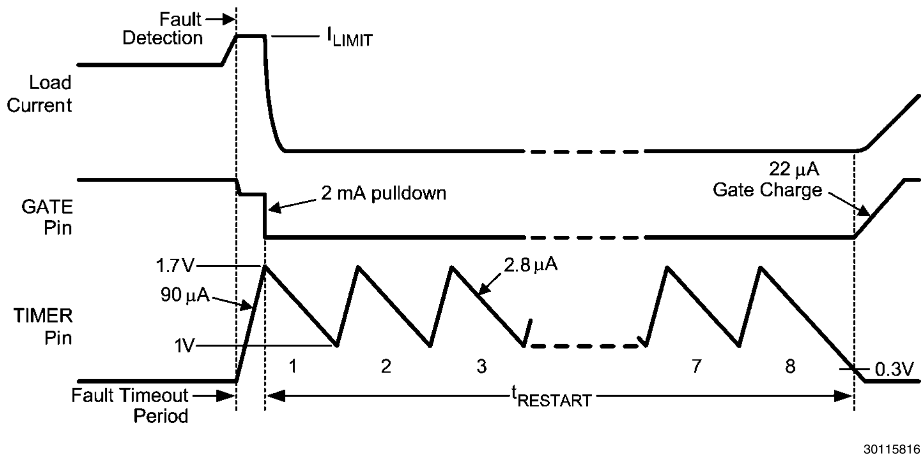



FIGURE 4. Restart Sequence

## Under-Voltage Lockout (UVLO)

The series pass MOSFET ($Q_1$) is enabled when the input supply voltage ($V_{SYS}$) is within the operating range defined by the programmable under-voltage lockout (UVLO) and over-voltage lockout (OVLO) levels. Typically the UVLO level at $V_{SYS}$ is set with a resistor divider (R1-R3) as shown in *Figure 5*. Refering to the Block Diagram when $V_{SYS}$ is below the UVLO level, the internal 23 µA current source at UVLO is enabled, the current source at OVLO is off, and $Q_1$ is held off by the 2 mA pull-down current at the GATE pin. As $V_{SYS}$ is increased, raising the voltage at UVLO above its threshold the 23 µA current source at UVLO is switched off, increasing the voltage at UVLO, providing hysteresis for this threshold. With the UVLO/EN pin above its threshold, $Q_1$ is switched on by the 22 µA current source at the GATE pin if the insertion time delay has expired.

See the Applications Section for a procedure to calculate the values of the threshold setting resistors (R1-R3). The minimum possible UVLO level at $V_{SYS}$ can be set by connecting the UVLO/EN pin to VIN. In this case, $Q_1$ is enabled after the insertion time when the voltage at VIN reaches the POR threshold. After power up, an UVLO condition will toggle high the VIN UV FAULT bit in the STATUS_INPUT (7Ch), the INPUT bit in the STATUS_WORD register, and the VIN_UNDERVOLTAGE_FAULT bit in the DIAGNOSTIC_WORD (E1h) register, and $\overline{SMBA}$ pin will be pulled low unless this feature is disabled using the ALERT_MASK (D8h) register.

## Over-Voltage Lockout (OVLO)

The series pass MOSFET ($Q_1$) is enabled when the input supply voltage ($V_{SYS}$) is within the operating range defined by the programmable under-voltage lockout (UVLO) and over-voltage lockout (OVLO) levels. If $V_{SYS}$ raises the OVLO pin voltage above its threshold, $Q_1$ is switched off by the 2 mA pull-down current at the GATE pin, denying power to the load. When the OVLO pin is above its threshold, the internal 23 µA current source at OVLO is switched on, raising the voltage at OVLO to provide threshold hysteresis. When $V_{SYS}$ is reduced below the OVLO level, $Q_1$ is re-enabled. An OVLO condition will toggle high the VIN OV FAULT bit in the STATUS_INPUT (7Ch), the INPUT bit in the STATUS_WORD register, and the VIN_OVERVOLTAGE_FAULT bit in the DIAGNOSTIC_WORD (E1h) register, and the $\overline{SMBA}$ pin will be pulled low unless this feature is disabled using the ALERT_MASK (D8h) register.

See the Applications Section for a procedure to calculate the threshold setting resistor values.

## Shutdown Control

The load current can be remotely switched off by taking the UVLO/EN pin below its threshold with an open collector or open drain device, as shown in *Figure 5*. Upon releasing the UVLO/EN pin, the LM25066 switches on the load current with inrush current and power limiting.

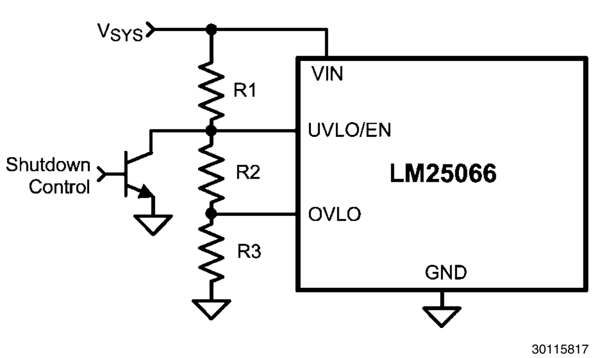



FIGURE 5. Shutdown Control

## Power Good

The Power Good indicator (PGD) is connected to the drain of an internal N-channel MOSFET capable of sustaining 17V in the off-state, and transients up to 20V. An external pull-up resistor is required at PGD to an appropriate voltage to indicate the status to downstream circuitry. The off-state voltage at the PGD pin can be higher or lower than the voltages at VIN and OUT. PGD is switched high when the voltage at the FB pin exceeds the PGD threshold voltage. Typically, the output voltage threshold is set with a resistor divider from output to feedback, although the monitored voltage need not be the output voltage. Any other voltage can be monitored as long as the voltage at the FB pin does not exceed its maximum rating. Referring to the Block Diagram, when the voltage at the FB pin is below its threshold, the 24 µA current source at FB is disabled. As the output voltage increases, taking FB above its threshold, the current source is enabled, sourcing current out of the pin, raising the voltage at FB to provide threshold hysteresis. The PGD output is forced low when either the UVLO/EN pin is below its threshold or the OVLO pin is above its threshold. The status of the PGD pin can be read via the PMBus interface in either the STATUS_WORD (79h) or DIAGNOSTIC_WORD (E1h) registers.

## VDD Sub-Regulator

The LM25066 contains an internal linear sub-regulator which steps down the input voltage to generate a 4.5V rail used for powering low voltage circuitry. When the input voltage is below 4.5V, VDD will track VIN. For input voltages 3.3V and below, VDD should be tied directly to VIN to avoid the dropout of the sub-regulator. The VDD sub-regulator should be used as the pull-up supply for the CL, CB, $\overline{\text{RETRY}}$, ADR2, ADR1, ADR0 pins if they are to be tied high. It may also be used as the pull-up supply for the PGD and the SMBus signals (SDA, SCL, $\overline{\text{SMBA}}$). The VDD sub-regulator is not designed to drive high currents and should not be loaded with other integrated circuits. The VDD pin is current limited to 45mA in order to protect the LM25066 in the event of a short. The sub-regulator requires a bypass capacitance having a value between 1 µF and 4.7 µF to be placed as close to the VDD pin as the PCB layout allows.

## Remote Temperature Sensing

The LM25066 is designed to measure temperature remotely using an MMBT3904 NPN transistor. The base and collector of the MMBT3904 is connected to the DIODE pin and the emitter is grounded. Place the MMBT3904 near the device whose temperature is to be monitored. If the temperature of the hot-swap pass MOSFET, $Q_1$, is to be measured, the MMBT3904 should be placed as close to $Q_1$ as the layout allows. The temperature is measured by means of a change in the diode voltage in response to a step in current supplied by the DIODE pin. The DIODE pin sources a constant 9.4 µA but pulses 250 µA once every millisecond in order to measure the diode temperature. Care must be taken in the PCB layout to keep the parasitic resistance between the DIODE pin and the MMBT3904 low so as not to degrade the measurement. Additionally, a small 1000 pF bypass capacitor should be placed in parallel with the MMBT3904 to reduce the effects of noise. The temperature can be read using the READ_TEMPERATURE_1 PMBus command (8Dh). The default limits of the LM25066 will cause $\overline{\text{SMBA}}$ pin to be pulled low if the measured temperature exceeds 125°C and will disable the hot-swap pass MOSFET if the temperature exceeds 150°C. These thresholds can be reprogrammed via the PMBus interface using the OT_WARN_LIMIT (51h) and OT_FAULT_LIMIT (4Fh) commands. If the temperature measurement and protection capability of the LM25066 is not used, the DIODE pin should be grounded.

## Damaged MOSFET Detection

The LM25066 is able to detect whether the external MOSFET, $Q_1$, is damaged under certain conditions. If the voltage across the sense resistor exceeds 4mV while the GATE voltage is low or the internal logic indicates that the GATE should be low, the EXT_MOSFET_SHORTED bit in the STATUS_MFR_SPECIFIC (80h) and DIAGNOSTIC_WORD (E1h) registers will be toggled high and the $\overline{\text{SMBA}}$ pin will be pulled low unless this feature is disabled using the ALERT_MASK register (D8h). This method effectively determines whether $Q_1$ is shorted because of damage present between the drain and gate and/or drain and source of the external MOSFET.

## Enabling/Disabling and Resetting

The output can be disabled at any time during normal operation by either pulling the UVLO/EN pin to below its threshold or the OVLO pin above its threshold, causing the GATE voltage to be forced low with a pull-down strength of 2mA. Toggling the UVLO/EN pin will also reset the LM25066 from a latched-off state due to an over-current or over-power limit condition which has caused the maximum allowed number of retries to be exceeded. While the UVLO/EN or OVLO pins can be used to disable the output, they have no effect on the volatile memory or address location of the LM25066. User stored values for address, device operation, and warning and fault levels programmed via the SMBus are preserved while the LM25066 is powered regardless of the state of the UVLO/EN and OVLO pins. The output may also be enabled or disabled by writing 80h or 0h to the OPERATION (03h) register. To re-enable after a fault, the fault condition should be cleared and the OPERATION (03h) register should be written to 0h and then 80h.

The SMBus address of the LM25066 is captured based on the states of the ADR0, ADR1, and ADR2 pins (GND, NC, VDD) during turn-on and is latched into a volatile register once VDD has exceeded its POR threshold of 2.6V. Reassigning or postponing the address capture is accomplished by holding the VREF pin to ground. Pulling the VREF pin low will also reset the logic and erase the volatile memory of the LM25066. Once released, the VREF pin will charge up to its final value and the address will be latched into a volatile register once the voltage at the VREF exceeds 2.4V.

## Applications Section

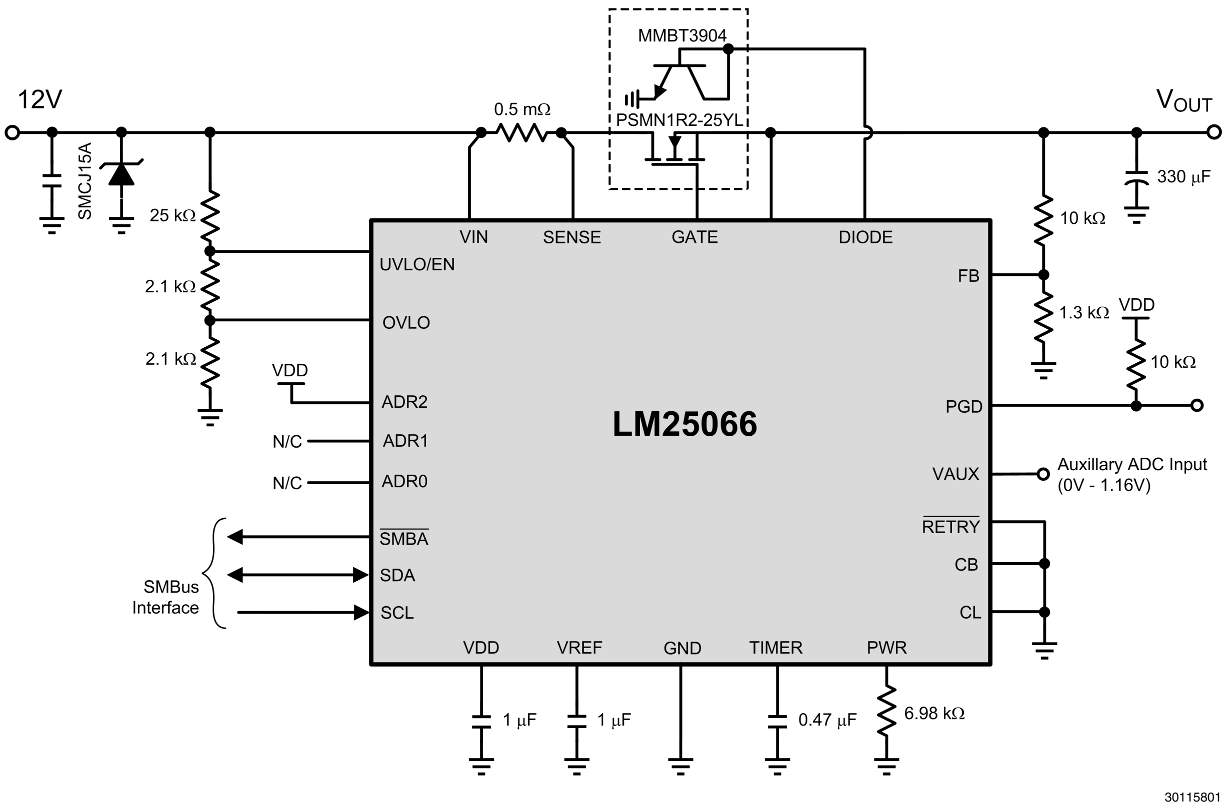



**FIGURE 6. Typical Application Circuit**

### DESIGN-IN PROCEDURE

(Refer to *Figure 6* for Typical Application Circuit) Shown here is the step-by-step procedure for hardware design of the LM25066. This procedure refers to section numbers that provide detailed information on the following design steps. The recommended design-in procedure is as follows:

**MOSFET Selection:** Determine MOSFET value based on breakdown voltage, current and power ratings.

**Current Limit, $R_S$:** Determine the current limit threshold ($I_{LIM}$). This threshold must be higher than the normal maximum load current, allowing for tolerances in the current sense resistor value and the LM25066 Current Limit threshold voltage. Use equation 1 to determine the value for $R_S$.

**Power Limit Threshold:** Determine the maximum allowable power dissipation for the series pass MOSFET ($Q_1$) using the device's SOA information. Use equation 2 to determine the value for $R_{PWR}$.

**Turn-On Time and TIMER Capacitor, $C_T$:** Determine the value for the timing capacitor at the TIMER pin ($C_T$) using equation 8. The fault timeout period ($t_{FAULT}$) **MUST** be longer than the circuit's turn-on-time. The turn-on time can be estimated using the equations in the TURN-ON TIME section of this data sheet, but should be verified experimentally. Review the resulting insertion time, and the restart timing if retry is enabled.

**UVLO, OVLO:** Choose option A, B, C, or D from the UVLO, OVLO section of the Application Information to set the UVLO and OVLO thresholds and hysteresis. Use the procedure for the appropriate option to determine the resistor values at the UVLO/EN and OVLO pins.

**Power Good:** Choose the appropriate output voltage and calculate the required resistor divider from the output voltage to the FB pin. Choose either VDD or OUT to connect properly sized pull-up resistor for the Power Good output (PGD).

**Refer to Programming Guide section:** After all hardware design is complete, refer to the programming guide for a step by step procedure regarding software.

### MOSFET SELECTION

It is recommended that the external MOSFET ($Q_1$) selection be based on the following criteria:

- The $BV_{DSS}$ rating should be greater than the maximum system voltage ($V_{SYS}$), plus ringing and transients which can occur at $V_{SYS}$ when the circuit card, or adjacent cards, are inserted or removed.

- The maximum continuous current rating should be based on the current limit threshold (e.g. 25 mV/$R_S$), not the maximum load current, since the circuit can operate near the current limit threshold continuously.

- The Pulsed Drain Current spec ($I_{DM}$) must be greater than the current threshold for the circuit breaker function (45 mV/$R_S$ when CL = CB = GND).

- The SOA (Safe Operating Area) chart of the device and its thermal properties should be used to determine the maximum power dissipation threshold set by the $R_{PWR}$ resistor. The programmed maximum power dissipation should have a reasonable margin from the maximum power defined by the MOSFET's SOA curve (if the device is set to infinitely retry, the MOSFET will be repeatedly stressed during fault restart cycles). The MOSFET manufacturer should be consulted for guidelines.

- $R_{DS(on)}$ should be sufficiently low such that the power dissipation at maximum load current ($I_{LIM}^2$ x $R_{DS(on)}$) does not raise its junction temperature above the manufacturer's recommendation.

- The gate-to-source voltage provided by the LM25066 can be as high as 18.8V at turn-on when the output voltage is zero. At turn-off, the reverse gate-to-source voltage will be equal to the output voltage at the instant the GATE pin is pulled low. If the device chosen for $Q_1$ is not rated for these voltages, an external zener diode must be added from its gate to source, with the zener voltage less than the device maximum $V_{GS}$ rating. The zener diode's working voltage protects the MOSFET during turn-on, and its forward voltage protects the MOSFET during shutoff. The zener diode's forward current rating must be at least 190 mA to conduct the GATE pull-down current when a circuit breaker condition is detected.

### CURRENT LIMIT ($R_S$)

The LM25066 monitors the current in the external MOSFET $Q_1$ by measuring the voltage across the sense resistor ($R_S$), connected from VIN to SENSE. The required resistor value is calculated from:

$$R_S = \frac{V_{CL}}{I_{LIM}} \quad (1)$$

where $I_{LIM}$ is the desired current limit threshold. If the voltage across $R_S$ reaches $V_{CL}$, the current limit circuit modulates the gate of $Q_1$ to regulate the current at $I_{LIM}$. While the current limiting circuit is active, the fault timer is active as described in the Fault Timer & Restart section. For proper operation, $R_S$ must be less than 200 mΩ.

$V_{CL}$ can be set to either 25mV or 46mV via hardware and/or software. This setting defaults to use of CL pin which when grounded is 25mV or high is 46mV. The value when powered can be set via PMBus™ with the MFR_SPECIFIC_DEVICE_SETUP command, which defaults to the 25mV setting.

Once the desired setting is known, calculate the shunt based on that input voltage and maximum current. While the maximum load current in normal operation can be used to determine the required power rating for resistor $R_S$, basing it on the current limit value provides a more reliable design since the circuit can operate near the current limit threshold continuously. The resistor's surge capability must also be considered since the circuit breaker threshold is 1.8 or 3.6 times the current limit threshold.

Connections from $R_S$ to the LM25066 should be made using Kelvin techniques. In the suggested layout of *Figure 7*, the small pads at the lower corners of the sense resistor connect only to the sense resistor terminals and not to the traces carrying the high current. With this technique, only the voltage across the sense resistor is applied to VIN and SENSE, eliminating the voltage drop across the high current solder connections.

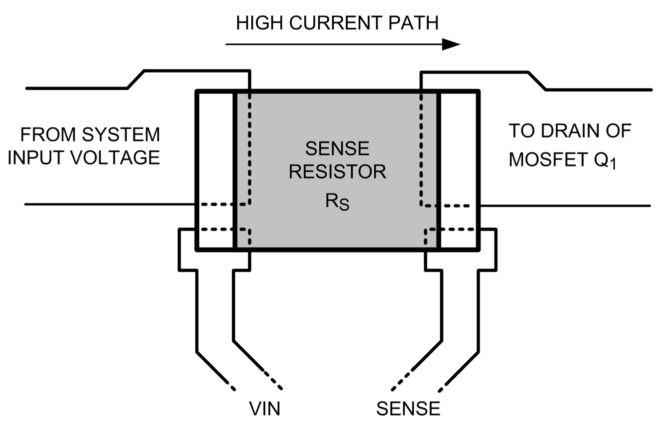



**FIGURE 7. Sense Resistor Connections**

### POWER LIMIT THRESHOLD

The LM25066 determines the power dissipation in the external MOSFET ($Q_1$) by monitoring the drain current (the current in $R_S$), and the $V_{DS}$ of $Q_1$ (SENSE to OUT pins). The resistor at the PWR pin ($R_{PWR}$) sets the maximum power dissipation for $Q_1$ and is calculated from the following equation:

$$R_{PWR} = 1.71 \times 10^5 \times R_S \times P_{MOSFET(LIM)} \quad (2)$$

where $P_{MOSFET(LIM)}$ is the desired power limit threshold for $Q_1$ and $R_S$ is the current sense resistor described in the Current Limit section. For example, if $R_S$ is 10 mΩ and the desired power limit threshold is 20W, $R_{PWR}$ calculates to 34.2 kΩ. If $Q_1$'s power dissipation reaches the threshold, $Q_1$'s gate is controlled to regulate the load current, keeping $Q_1$'s power from exceeding the threshold. For proper operation of the power limiting feature, $R_{PWR}$ must be ≤150 kΩ. While the power limiting circuit is active, the fault timer is active as described in the Fault Timer & Restart section. Typically, power limit is reached during startup, or if the output voltage falls because of a severe overload or short circuit. The programmed maximum power dissipation should have a reasonable margin from the maximum power defined by the SOA chart, especially if retry is enabled since the MOSFET will be repeatedly stressed during fault restart cycles. The MOSFET manufacturer should be consulted for guidelines. If the application does not require use of the power limit function, the PWR pin can be left open. The accuracy of the power limit function at turn-on may degrade if a very low value power dissipation limit is set. The reason for this caution is that the voltage across the sense resistor, which is monitored and regulated by the power limit circuit, is lowest at turn-on when the regulated current is at a minimum. The voltage across the sense resistor during power limit can be expressed as follows:

$$V_{SENSE} = I_L \times R_S = \frac{R_{PWR}}{1.71 \times 10^5 \times V_{DS}} = \frac{R_S \times P_{FET(LIM)}}{V_{DS}} \quad (3)$$

where $I_L$ is the current in $R_S$ and $V_{DS}$ is the voltage across $Q_1$. For example, if the power limit is set at 20W with $R_S$ = 10 mΩ and $V_{DS}$ = 15V, the sense resistor voltage calculates to 13.3 mV, which is comfortably regulated by the LM25066. However, if the power limit is set lower (e.g. 2W), the sense resistor voltage calculates to 1.33 mV. At this low level, noise and offsets within the LM25066 may degrade the power limit accuracy. To maintain accuracy, the sense resistor voltage should not be less than 5 mV.

## TURN-ON TIME

The output turn-on time depends on whether the LM25066 operates in current limit, or in both power limit and current limit, during turn-on.

**A) Turn-on with current limit only:** The current limit threshold ($I_{LIM}$) is determined by the current sense resistor ($R_S$). If the current limit threshold is less than the current defined by the power limit threshold at maximum $V_{DS}$, the circuit operates at the current limit threshold only during turn-on. Referring to *Figure 8*A, as the load current reaches $I_{LIM}$, the gate-to-source voltage is controlled at $V_{GSL}$ to maintain the current at $I_{LIM}$. As the output voltage reaches its final value ($V_{DS}$ ≅ 0V) the drain current reduces to its normal operating value. The time for the OUT pin voltage to transition from zero volts to $V_{SYS}$ is equal to:

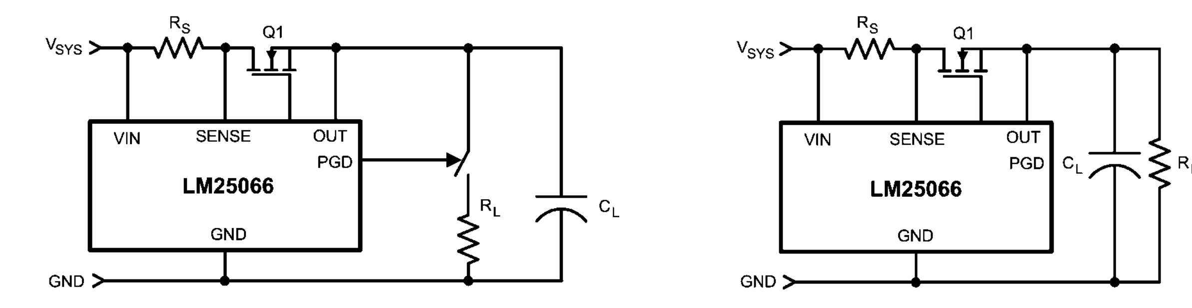
$$t_{ON} = \frac{V_{SYS} \times C_L}{I_{LIM}} \quad (4)$$

where $C_L$ is the load capacitance. For example, if $V_{SYS}$ = 12V, $C_L$ = 1000 µF, and $I_{LIM}$ = 1A, $t_{ON}$ calculates to 12 ms. The maximum instantaneous power dissipated in the MOSFET is 12W. This calculation assumes the time from $t_1$ to $t_2$ in *Figure 9*(a) is small compared to $t_{ON}$ and the load does not draw any current until after the output voltage has reached its final value, and PGD switches high (*Figure 8*A). The Fault Timeout Period must be set longer than $t_{ON}$ to prevent a fault shutdown before the turn-on sequence is complete.

If the load draws current during the turn-on sequence (*Figure 8*B), the turn-on time is longer than the above calculation and is approximately equal to:

$$t_{ON} = -(R_L \times C_L) \times \ln\left[\frac{(I_{LIM} \times R_L) - V_{SYS}}{(I_{LIM} \times R_L)}\right] \quad (5)$$

where $R_L$ is the load resistance. The Fault Timeout Period must be set longer than $t_{ON}$ to prevent a fault shutdown before the turn-on sequence is complete.




A. No Load Current During Turn-On

B. Load Draws Current During Turn-On

**FIGURE 8.**

**B) Turn-On with Power Limit and Current Limit:** The maximum allowed power dissipation in $Q_1$ ($P_{MOSFET(LIM)}$) is defined by the resistor at the PWR pin, and the current sense resistor $R_S$. See the Power Limit Threshold section. If the current limit threshold ($I_{LIM}$) is higher than the current defined by the power limit threshold at maximum $V_{DS}$ ($P_{MOSFET(LIM)}/V_{SYS}$), the circuit operates initially in the power limit mode when the $V_{DS}$ of $Q_1$ is high and then transitions to current limit mode as the current increases to $I_{LIM}$ and $V_{DS}$ decreases. Assuming the load ($R_L$) is not connected during turn-on, the time for the output voltage to reach its final value is approximately equal to:

$$t_{ON} = \frac{C_L \times V_{SYS}^2}{2 \times P_{MOSFET(LIM)}} + \frac{C_L \times P_{MOSFET(LIM)}}{2 \times I_{LIM}^2} \quad (6)$$

For example, if $V_{SYS}$ = 12V, $C_L$ = 1000 µF, $I_{LIM}$ = 1A, and $P_{MOSFET(LIM)}$ = 10W, $t_{ON}$ calculates to ≅12.2 ms, and the initial current level ($I_P$) is approximately 0.83A. The Fault Timeout Period must be set longer than $t_{ON}$.

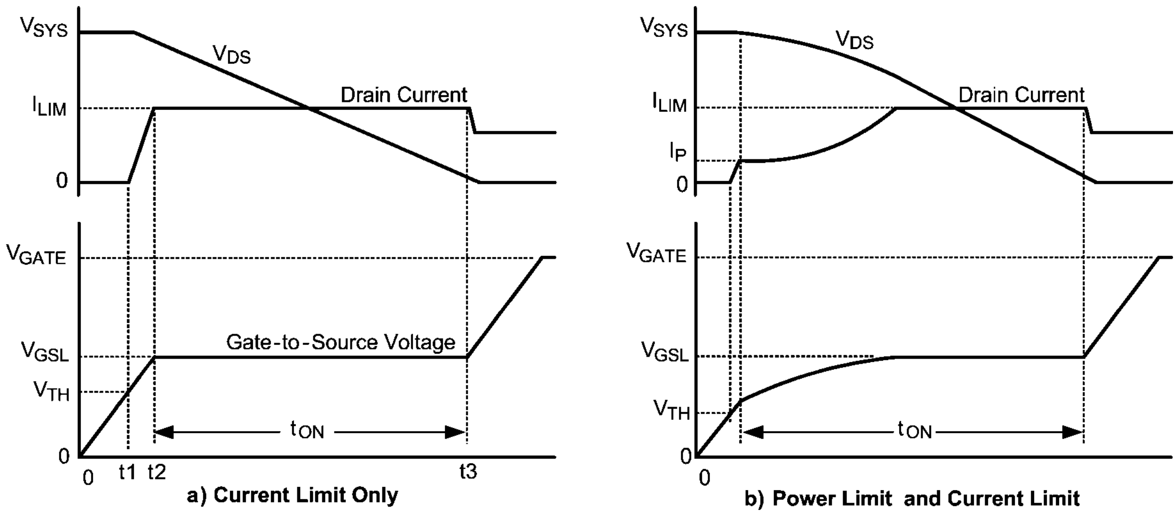



**FIGURE 9. MOSFET Power Up Waveforms**

## TIMER CAPACITOR, $C_T$

The TIMER pin capacitor ($C_T$) sets the timing for the insertion time delay, fault timeout period, and the restart timing of the LM25066.

**A) Insertion Delay -** Upon applying the system voltage ($V_{SYS}$) to the circuit, the external MOSFET ($Q_1$) is held off during the insertion time ($t_1$ in *Figure 2*) to allow ringing and transients at $V_{SYS}$ to settle. Since each backplane's response to a circuit card plug-in is unique, the worst case settling time must be determined for each application. The insertion time starts when VIN reaches the POR threshold, at which time the internal 5.5 µA current source charges $C_T$ from 0V to 1.7V. The required capacitor value is calculated from:

$$C_T = \frac{t_1 \times 5.5\ \mu A}{1.7V} = t_1 \times 3.2 \times 10^{-6} \quad (7)$$

For example, if the desired insertion delay is 250 ms, $C_T$ calculates to 0.8 µF. At the end of the insertion delay, $C_T$ is quickly discharged by a 1.9 mA current sink.

**B) Fault Timeout Period -** During inrush current limiting or upon detection of a fault condition where the current limit and/or power limit circuits regulate the current through $Q_1$, the fault timer current source (90 µA) is switched on to charge $C_T$. The Fault Timeout Period is the time required for the TIMER pin voltage to reach 1.7V, at which time $Q_1$ is switched off. The required capacitor value for the desired Fault Timeout Period $t_{FAULT}$ is calculated from:

$$C_T = \frac{t_{FAULT} \times 90\ \mu A}{1.7V} = t_{FAULT} \times 5.3 \times 10^{-5} \quad (8)$$

For example, if the desired Fault Timeout Period is 15 ms, $C_T$ calculates to 0.8 µF. $C_T$ is discharged by the 2.8 µA current sink at the end of the Fault Timeout Period. After the Fault Timeout Period, if retry is disabled, the LM25066 latches the GATE pin low until a power up sequence is initiated by external circuitry. When the Fault Timeout Period of the LM25066 expires, a restart sequence starts as described below (Restart Timing). During consecutive cycles of the restart sequence, the fault timeout period is shorter than the initial fault timeout period described above by approximately 20% since the voltage at the TIMER pin starts ramping up from 0.3V rather than ground.

Since the LM25066 normally operates in power limit and/or current limit during a power up sequence, the Fault Timeout Period **MUST** be longer than the time required for the output voltage to reach its final value. See the Turn-On Time section.

**C) Restart Timing** - For the LM25066, after the Fault Timeout Period described above, $C_T$ is discharged by the 2.8 µA current sink to 1V. The TIMER pin then cycles through seven additional charge/discharge cycles between 1V and 1.7V as shown in *Figure 4*. The restart time ends when the TIMER pin voltage reaches 0.3V during the final high-to-low ramp. The restart time, after the Fault Timeout Period, is equal to:

$$t_{RESTART} = C_T \times \left[ \frac{7 \times 0.7V}{2.8\ \mu A} + \frac{7 \times 0.7V}{90\ \mu A} + \frac{1.4V}{2.8\ \mu A} \right] \quad (9)$$

$$= C_T \times 2.3 \times 10^6 \quad (10)$$

For example, if $C_T$ = 0.8 µF, $t_{RESTART}$ = 2 seconds. At the end of the restart time, $Q_1$ is switched on. If the fault is still present, the fault timeout and restart sequence repeats. The on-time duty cycle of $Q_1$ is approximately 0.67% in this mode.

## UVLO, OVLO

By programming the UVLO and OVLO thresholds the LM25066 enables the series pass device ($Q_1$) when the input supply voltage ($V_{SYS}$) is within the desired operational range. If $V_{SYS}$ is below the UVLO threshold, or above the OVLO threshold, $Q_1$ is switched off, denying power to the load. Hysteresis is provided for each threshold.

**Option A:** The configuration shown in *Figure 10* requires three resistors (R1-R3) to set the thresholds.

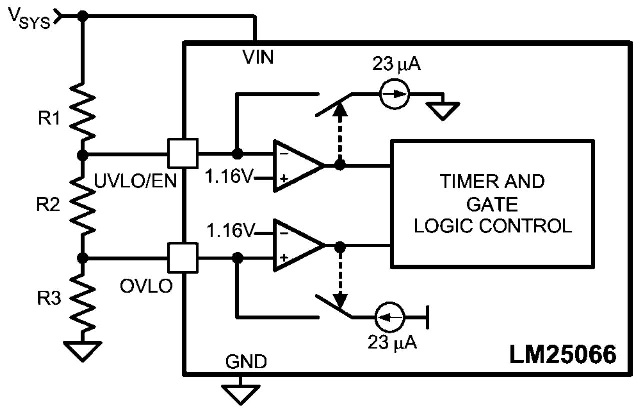



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**FIGURE 10. UVLO and OVLO Thresholds Set By R1-R3**

The procedure to calculate the resistor values is as follows:

- Choose the upper UVLO threshold ($V_{UVH}$), and the lower UVLO threshold ($V_{UVL}$).
- Choose the upper OVLO threshold ($V_{OVH}$).
- The lower OVLO threshold ($V_{OVL}$) cannot be chosen in advance in this case, but is determined after the values for R1-R3 are determined. If $V_{OVL}$ must be accurately defined in addition to the other three thresholds, see Option B below.

The resistors are calculated as follows:

$$R1 = \frac{V_{UVH} - V_{UVL}}{23\ \mu A} = \frac{V_{UV(HYS)}}{23\ \mu A} \quad (11)$$

$$R3 = \frac{1.16V \times R1 \times V_{UVL}}{V_{OVH} \times (V_{UVL} - 1.16V)} \quad (12)$$

$$R2 = \frac{1.16V \times R1}{V_{UVL} - 1.16V} - R3 \quad (13)$$

The lower OVLO threshold is calculated from:

$$V_{OVL} = [(R1 + R2) \times (\frac{1.16V}{R3} - 23\ \mu A)] + 1.16V \quad (14)$$

As an example, assume the application requires the following thresholds: $V_{UVH}$ = 8V, $V_{UVL}$ = 7V, $V_{OVH}$ = 15V.

$$R1 = \frac{8V - 7V}{23\ \mu A} = \frac{1V}{23\ \mu A} = 43.5\ k\Omega \quad (15)$$

$$R3 = \frac{1.16V \times R1 \times 7V}{15V \times (7V - 1.16V)} = 4.03\ k\Omega \quad (16)$$

$$R2 = \frac{1.16V \times R1}{(7V - 1.16V)} - R3 = 4.61\ k\Omega \quad (17)$$

The lower OVLO threshold calculates to 12.03V and the OVLO hysteresis is 2.97V. Note that the OVLO hysteresis is always slightly greater than the UVLO hysteresis in this configuration. When the R1-R3 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 1.16V + [R1 \times (23\ \mu A + \frac{1.16V}{(R2 + R3)})] \quad (18)$$

$$V_{UVL} = \frac{1.16V \times (R1 + R2 + R3)}{R2 + R3} \quad (19)$$

$$V_{UV(HYS)} = R1 \times 23\mu A$$

$$V_{OVH} = \frac{1.16V \times (R1 + R2 + R3)}{R3} \quad (20)$$

$$V_{OVL} = [(R1 + R2) \times (\frac{1.16V}{R3} - 23\ \mu A)] + 1.16V \quad (21)$$

$$V_{OV(HYS)} = (R1 + R2) \times 23\mu A$$

**Option B:** If all four thresholds must be accurately defined, the configuration in *Figure 11* can be used.

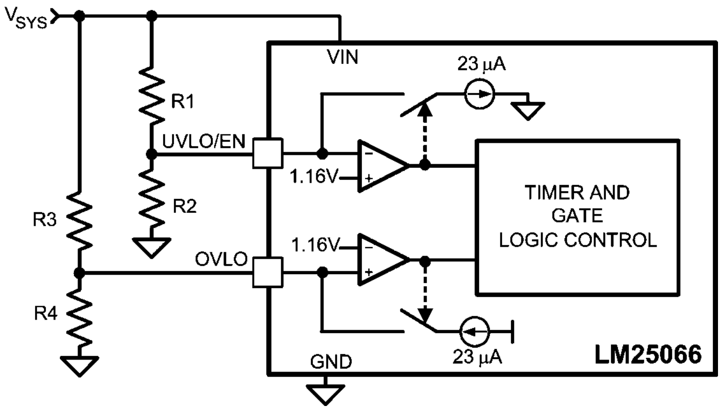



**FIGURE 11. Programming the Four Thresholds**

The four resistor values are calculated as follows: - Choose the upper and lower UVLO thresholds ($V_{UVH}$) and ($V_{UVL}$).

$$R1 = \frac{V_{UVH} - V_{UVL}}{23\ \mu A} = \frac{V_{UV(HYS)}}{23\ \mu A} \quad (22)$$

$$R2 = \frac{1.16V \times R1}{(V_{UVL} - 1.16V)} \quad (23)$$

- Choose the upper and lower OVLO threshold ($V_{OVH}$) and ($V_{OVL}$).

$$R3 = \frac{V_{OVH} - V_{OVL}}{23\ \mu A} = \frac{V_{OV(HYS)}}{23\ \mu A} \quad (24)$$

$$R4 = \frac{1.16V \times R3}{(V_{OVH} - 1.16V)} \quad (25)$$

As an example, assume the application requires the following thresholds: $V_{UVH}$ = 8V, $V_{UVL}$ = 7V, $V_{OVH}$ = 15.5V, and $V_{OVL}$ = 14V. Therefore $V_{UV(HYS)}$ = 1V and $V_{OV(HYS)}$ = 1.5V. The resistor values are:

R1 = 43.5 kΩ, R2 = 8.64 kΩ

R3 = 65.2 kΩ, R4 = 5.27 kΩ

When the R1-R4 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 1.16V + [R1 \times (\frac{1.16V}{R2} + 23\ \mu A)] \quad (26)$$

$$V_{UVL} = \frac{1.16V \times (R1 + R2)}{R2} \quad (27)$$

$$V_{UV(HYS)} = R1 \times 23\ \mu A$$

$$V_{OVH} = \frac{1.16V \times (R3 + R4)}{R4} \quad (28)$$

$$V_{OVL} = 1.16V + [R3 \times (\frac{1.16V}{R4} - 23\ \mu A)] \quad (29)$$

$$V_{OV(HYS)} = R3 \times 23\ \mu A$$

**Option C:** The minimum UVLO level is obtained by connecting the UVLO/EN pin to VIN as shown in *Figure 12*. $Q_1$ is switched on when the VIN voltage reaches the POR threshold (≊2.6V). The OVLO thresholds are set using R3, R4. Their values are calculated using the procedure in Option B.

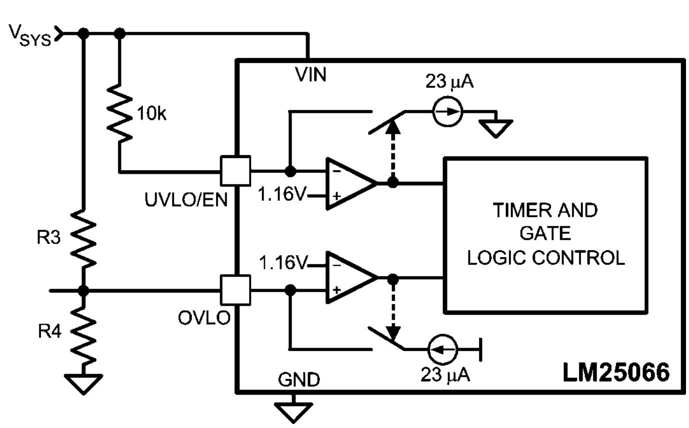



**FIGURE 12. UVLO = POR**

**Option D:** The OVLO function can be disabled by grounding the OVLO pin. The UVLO thresholds are set as described in Option B or Option C.

## POWER GOOD

When the voltage at the FB pin increases above its threshold, the internal pull-down acting on the PGD pin is disabled allowing PGD to rise to $V_{PGD}$ through the pull-up resistor, $R_{PG}$, as shown in *Figure 14*. The pull-up voltage ($V_{PGD}$) can be as high as 17V, and can be higher or lower than the voltages at VIN and OUT. VDD is a convenient choice for $V_{PGD}$ as it allows interface to low voltage logic and avoids glitching on PGD during power-up. If a delay is required at PGD, suggested circuits are shown in *Figure 15*. In *Figure 15*A, capacitor $C_{PG}$ adds delay to the rising edge, but not to the falling edge. In *Figure 15*B, the rising edge is delayed by $R_{PG1} + R_{PG2}$ and $C_{PG}$, while the falling edge is delayed a lesser amount by $R_{PG2}$ and $C_{PG}$. Adding a diode across $R_{PG2}$ (*Figure 15*C) allows for equal delays at the two edges, or a short delay at the rising edge and a long delay at the falling edge.

Setting the output threshold for the PGD pin requires two resistors (R4, R5) as shown in *Figure 13*. While monitoring the output voltage is shown in *Figure 13*, R4 can be connected to any other voltage which requires monitoring.

The resistor values are calculated as follows:

Choose the upper and lower threshold ($V_{PGDH}$) and ($V_{PGDL}$) at $V_{OUT}$.

$$R4 = \frac{V_{PGDH} - V_{PGDL}}{24\ \mu A} = \frac{V_{PGD(HYS)}}{24\ \mu A}$$

$$R5 = \frac{1.167V \times R4}{(V_{PGDH} - 1.167V)}$$

As an example, assume the application requires the following thresholds: $V_{PGDH}$ = 10.14V, and $V_{PGDL}$ = 9.9V. Therefore $V_{PGD(HYS)}$ = 0.24V. The resistor values are:

R4 = 10 kΩ, R5 = 1.3 kΩ

Where the R4 and R5 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{PGDH} = \frac{1.167V \times (R4 + R5)}{R5}$$

$$V_{PGDL} = 1.167V + \left[R4 \times \left(\frac{1.167V}{R5} + 24\ \mu A\right)\right]$$

$$V_{PGD(HYS)} = R4 \times 24\ \mu A$$

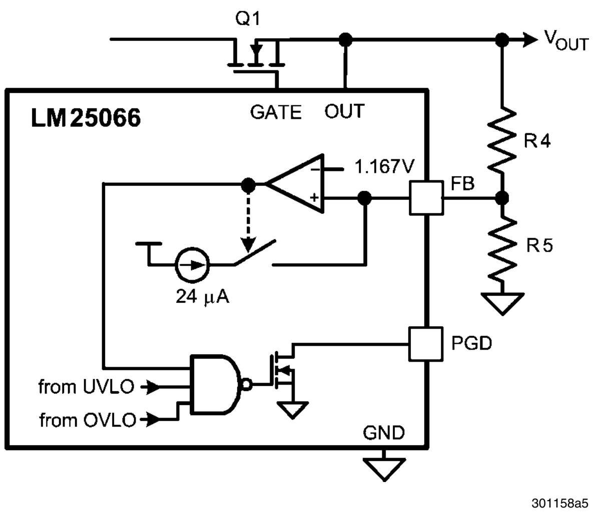



**FIGURE 13. Programming the PGD Threshold**

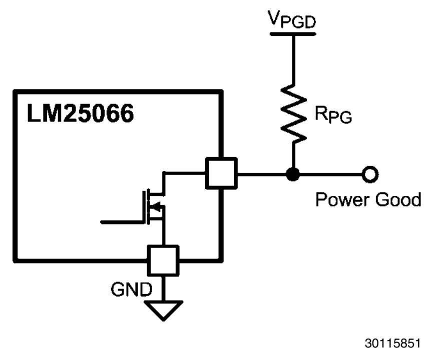



**FIGURE 14. Power Good Output**

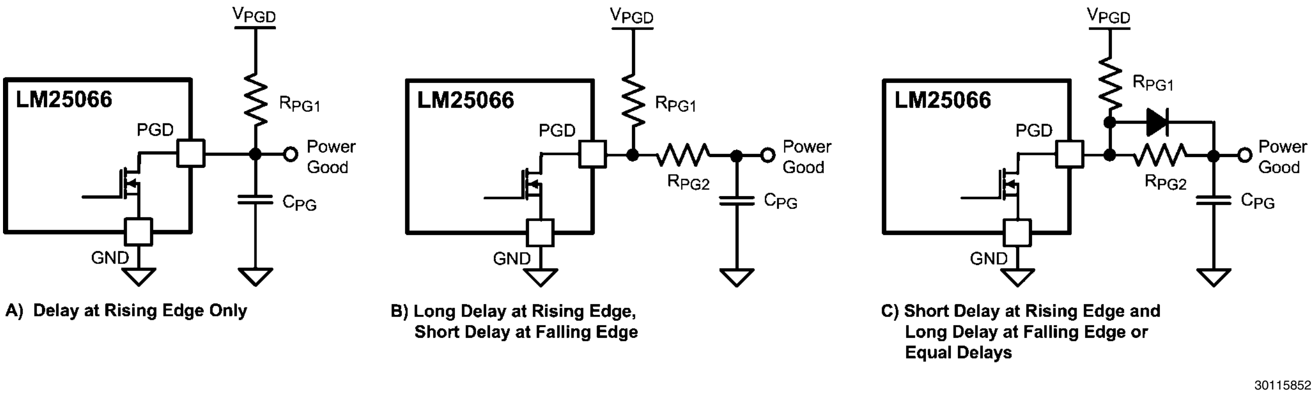



**FIGURE 15. Adding Delay to the Power Good Output Pin**

## SYSTEM CONSIDERATIONS

A) Continued proper operation of the LM25066 hot-swap circuit normally dictates that capacitance be present on the supply side of the connector into which the hot-swap circuit is plugged in, as depicted in *Figure 16*. The capacitor in the "LIVE POWER SOURCE" section is necessary to absorb the transient generated whenever the hot-swap circuit shuts off the load current. If the capacitance is not present, parasitic inductance of the supply lines will generate a voltage transient at shut-off which may exceed the absolute maximum rating of the LM25066, resulting in its destruction. A TVS device with appropriate voltage and power ratings can also be connected from VIN to GND to clamp the voltage spike (see application note AN-2100).

B) If the load powered by the LM25066 hot-swap circuit has inductive characteristics, a Schottky diode is required across the LM25066's output along with some load capacitance. The capacitance and diode are necessary to limit the negative excursion at the OUT pin when the load current is shut off. If the OUT pin transitions more than 0.3V negative, the LM25066 will internally reset, erasing the volatile setting for retries and warning thresholds. See *Figure 16*. To alleviate this, a small gate resistance (e.g. 10Ω) can be used. This resistor has the added benefit of damping any high frequency gate voltage oscillations, particularly in paralleled FET arrangements.

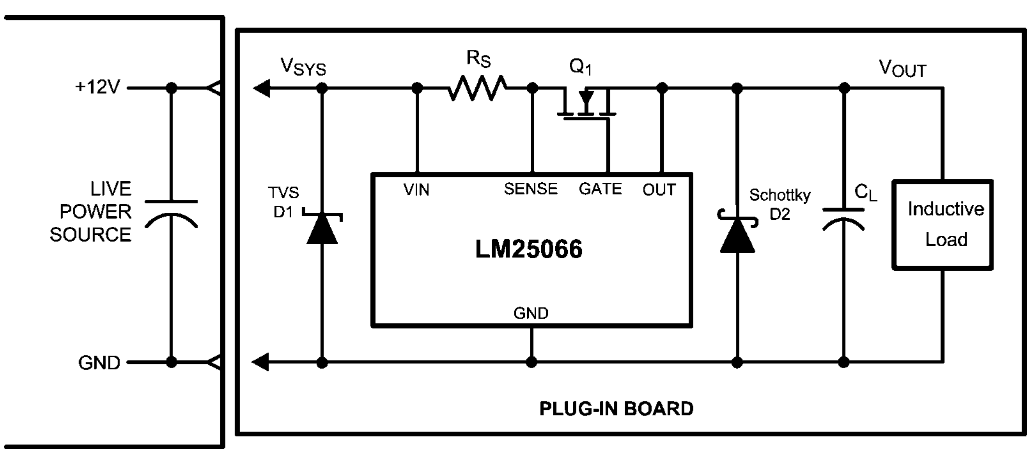



**FIGURE 16. Output Diode Required for Inductive Loads**

## PC BOARD GUIDELINES

The following guidelines should be followed when designing the PC board for the LM25066:

- Place the LM25066 close to the board's input connector to minimize trace inductance from the connector to the MOSFET.
- Place a small capacitor, $C_{IN}$ (1nF), directly adjacent to the VIN and GND pins of the LM25066 to help minimize transients which may occur on the input supply line. Transients of several volts can easily occur when the load current is shut off. ASIDE: note that if the current drawn by such capacitor is deemed unacceptable, input voltage spike transients can be appropriately miniminzed by proper placement of a TVS device and operation without this $C_{IN}$ capacitor becomes feasible.
- Place a 1 µF capacitor as close as possible to VREF pin.
- Place a 1 µF capacitor as close as possible to VDD pin.
- The sense resistor ($R_S$) should be placed close to the LM25066. In particular, the trace to the VIN pin should be made as low resistance as practical to ensure maximum current and power measurement accuracy. Connect $R_S$ using the Kelvin techniques shown in *Figure 7*.

- The high current path from the board's input to the load (via $Q_1$) and the return path should be parallel and close to each other to minimize parasitic loop inductance.

- The ground connections for the various components around the LM25066 should be connected directly to each other and to the LM25066's GND pin and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line. For more details, see application note AN-2100.

- Provide adequate heat sinking for the series pass device ($Q_1$) to help reduce stresses during turn-on and turn-off.

- Keep the gate trace from the LM25066 to the pass MOSFET short and direct.

- The board's edge connector can be designed such that the LM25066 detects via the UVLO/EN pin that the board is being removed and responds by turning off the load before the supply voltage is disconnected. For example, in Figure 17, the voltage at the UVLO/EN pin goes to ground before $V_{SYS}$ is removed from the LM25066 because of the shorter edge connector pin. When the board is inserted into the edge connector, the system voltage is applied to the LM25066's VIN pin before the UVLO voltage is taken high, thereby allowing the LM25066 to turn on the output in a controlled fashion.

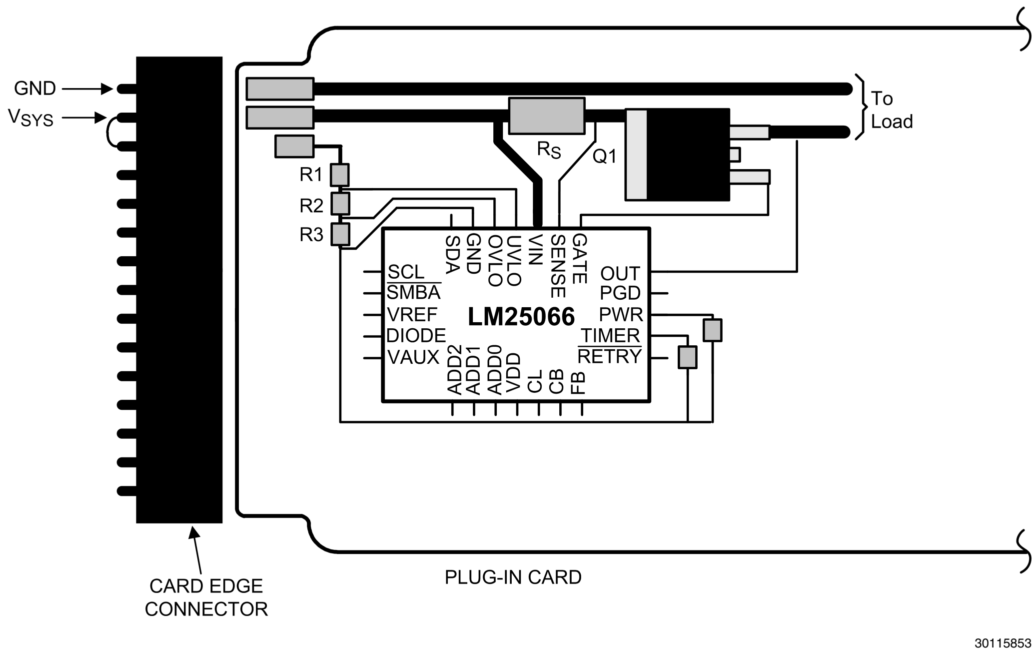



**FIGURE 17. Recommended Board Connector Design**

## PMBus™ Command Support

The device features an SMBus interface that allows the use of PMBus™ commands to set warn levels, error masks, and get telemetry on $V_{IN}$, $V_{OUT}$, $I_{IN}$, $V_{AUX}$, and $P_{IN}$. The supported PMBus™ commands are shown in Table 1.

**TABLE 1. Supported PMBus™ Commands**

| Code | Name | Function | R/W | Number Of Data Bytes | Default Value |
|---|---|---|---|---|---|
| 01h | OPERATION | Retrieves or stores the operation status. | R/W | 1 | 80h |
| 03h | CLEAR_FAULTS | Clears the status registers and re-arms the black box registers for updating. | Send Byte | 0 | |
| 19h | CAPABILITY | Retrieves the device capability. | R | 1 | B0h |
| 43h | VOUT_UV_WARN_LIMIT | Retrieves or stores output under-voltage warn limit threshold. | R/W | 2 | 0000h |
| 4Fh | OT_FAULT_LIMIT | Retrieves or stores over-temperature fault limit threshold. | R/W | 2 | 0960h (150°C) |
| 51h | OT_WARN_LIMIT | Retrieves or stores over-temperature warn limit threshold. | R/W | 2 | 07D0h (125°C) |
| 57h | VIN_OV_WARN_LIMIT | Retrieves or stores input over-voltage warn limit threshold. | R/W | 2 | 0FFFh |
| 58h | VIN_UV_WARN_LIMIT | Retrieves or stores input under-voltage warn limit threshold. | R/W | 2 | 0000h |
| 78h | STATUS_BYTE | Retrieves information about the part operating status. | R | 1 | 49h |
| 79h | STATUS_WORD | Retrieves information about the part operating status. | R | 2 | 3849h |
| 7Ah | STATUS_VOUT | Retrieves information about output voltage status. | R | 1 | 00h |
| 7Ch | STATUS_INPUT | Retrieves information about input status. | R | 1 | 10h |
| 7Dh | STATUS_TEMPERATURE | Retrieves information about temperature status. | R | 1 | 00h |
| 7Eh | STATUS_CML | Retrieves information about communications status. | R | 1 | 00h |
| 80h | STATUS_MFR_SPECIFIC | Retrieves information about circuit breaker and MOSFET shorted status. | R | 1 | 10h |
| 88h | READ_VIN | Retrieves input voltage measurement. | R | 2 | 0000h |
| 8Bh | READ_VOUT | Retrieves output voltage measurement. | R | 2 | 0000h |
| 8Dh | READ_TEMPERATURE_1 | Retrieves temperature measurement. | R | 2 | 0190h |
| 99h | MFR_ID | Retrieves manufacturer ID in ASCII characters (NSC). | R | 3 | 4Eh<br>53h<br>43h |
| 9Ah | MFR_MODEL | Retrieves Part number in ASCII characters. (LM25066). | R | 8 | 4Ch<br>4Dh<br>32h<br>35h<br>30h<br>36h<br>36h<br>0h |
| 9Bh | MFR_REVISION | Retrieves part revision letter/number in ASCII (e.g. AA). | R | 2 | 41h<br>41h |
| D0h | MFR_SPECIFIC_00<br>READ_VAUX | Retrieves auxiliary voltage measurement. | R | 2 | 0000h |
| D1h | MFR_SPECIFIC_01<br>MFR_READ_IIN | Retrieves input current measurement. | R | 2 | 0000h |
| D2h | MFR_SPECIFIC_02<br>MFR_READ_PIN | Retrieves input power measurement. | R | 2 | 0000h |
| D3h | MFR_SPECIFIC_03<br>MFR_IIN_OC_WARN_LIMIT | Retrieves or stores input current limit warn threshold. | R/W | 2 | 0FFFh |
| D4h | MFR_SPECIFIC_04<br>MFR_PIN_OP_WARN_LIMIT | Retrieves or stores input power limit warn threshold. | R/W | 2 | 0FFFh |

| Code | Name | Function | R/W | Number Of Data Bytes | Default Value |
|---|---|---|---|---|---|
| D5h | MFR_SPECIFIC_05<br>READ_PIN_PEAK | Retrieves measured maximum input power measurement. | R | 2 | 0000h |
| D6h | MFR_SPECIFIC_06<br>CLEAR_PIN_PEAK | Resets the contents of the peak input power register to zero. | Send Byte | 0 | |
| D7h | MFR_SPECIFIC_07<br>GATE_MASK | Disables external MOSFET gate control for FAULTs. | R/W | 1 | 0000h |
| D8h | MFR_SPECIFIC_08<br>ALERT_MASK | Retrieves or stores user $\overline{\text{SMBA}}$ fault mask. | R/W | 2 | 0820h |
| D9h | MFR_SPECIFIC_09<br>DEVICE_SETUP | Retrieves or stores information about number of retry attempts. | R/W | 1 | 0000h |
| DAh | MFR_SPECIFIC_10<br>BLOCK_READ | Retrieves most recent diagnostic and telemetry information in a single transaction. | R | 12 | 0460h<br>0000h<br>0000h<br>0000h<br>0000h<br>0000h |
| DBh | MFR_SPECIFIC_11<br>SAMPLES_FOR_AVG | Exponent value AVGN for number of samples to be averaged, range = 00h to 0Ch. | R/W | 1 | 00h |
| DCh | MFR_SPECIFIC_12<br>READ_AVG_VIN | Retrieves averaged input voltage measurement. | R | 2 | 0000h |
| DDh | MFR_SPECIFIC_13<br>READ_AVG_VOUT | Retrieves averaged output voltage measurement. | R | 2 | 0000h |
| DEh | MFR_SPECIFIC_14<br>READ_AVG_IIN | Retrieves averaged input current measurement. | R | 2 | 0000h |
| DFh | MFR_SPECIFIC_15<br>READ_AVG_PIN | Retrieves averaged input power measurement. | R | 2 | 0000h |
| E0h | MFR_SPECIFIC_16<br>BLACK_BOX_READ | Captures diagnostic and telemetry information which are latched when the first $\overline{\text{SMBA}}$ alert occurs after faults have been cleared. | R | 12 | 0000h<br>0000h<br>0000h<br>0000h<br>0000h<br>0000h |
| E1h | MFR_SPECIFIC_17<br>READ_DIAGNOSTIC_WORD | Manufacturer-specific parallel of the STATUS_WORD to convey all FAULT/WARN data in a single transaction. | R | 2 | 0460h |
| E2h | MFR_SPECIFIC_18<br>AVG_BLOCK_READ | Retrieves most recent average telemetry and diagnostic information in a single transaction. | R | 12 | 0460h<br>0000h<br>0000h<br>0000h<br>0000h<br>0000h |

## Standard PMBus™ Commands

### OPERATION (01h)

The OPERATION command is a standard PMBus™ command that controls the MOSFET switch. This command may be used to switch the MOSFET ON and OFF under host control. It is also used to re-enable the MOSFET after a fault triggered shutdown. Writing an OFF command followed by an ON command will clear all faults. Writing only an ON command after a fault triggered shutdown will not clear the fault registers. The OPERATION command is issued with the write byte protocol.

**TABLE 2. Recognized OPERATION Command Values**

| Value | Meaning | Default |
|---|---|---|
| 80h | Switch ON | 80h |
| 00h | Switch OFF | n/a |

### CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is a standard PMBus™ command that resets all stored warning and fault flags and the SMBA signal. If a fault or warning condition still exists when the CLEAR_FAULTS command is issued, the SMBA signal may not clear or will re-assert almost immediately. Issuing a CLEAR_FAULTS command will not cause the MOSFET to switch back on in the event of a fault turn-off: that must be done by issuing an OPERATION command after the fault condition is cleared. This command uses the PMBus™ send byte protocol.

### CAPABILITY (19h)

The CAPABILITY command is a standard PMBus™ command that returns information about the PMBus™ functions supported by the LM25066. This command is read with the PMBus™ read byte protocol.

**TABLE 3. CAPABILITY Register**

| Value | Meaning | Default |
|---|---|---|
| B0h | Supports Packet Error Check, 400Kbits/sec, Supports SMBus Alert | B0h |

### VOUT_UV_WARN_LIMIT (43h)

The VOUT_UV_WARN_LIMIT command is a standard PMBus™ command that allows configuring or reading the threshold for the VOUT Under-voltage Warning detection. Reading and writing to this register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table. Accesses to this command should use the PMBus™ read or write word protocol. If the measured value of VOUT falls below the value in this register, VOUT UV Warn Limit flags are set in the respective registers, and the SMBA signal is asserted.

**TABLE 4. VOUT_UV_WARN_LIMIT Register**

| Value | Meaning | Default |
|---|---|---|
| 1h – 0FFFh | VOUT Under-voltage Warning detection threshold | 0000h (disabled) |
| 0000h | VOUT Under-voltage Warning disabled | n/a |

### OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT is a standard PMBus™ command that allows configuring or reading the threshold for the Overtemperature Fault detection. Reading and writing to this register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table. Accesses to this command should use the PMBus™ read or write word protocol. If the measured temperature exceeds this value, an overtemperature fault is triggered, the MOSFET is switched off, OT Fault flags are set in the respective registers, and the SMBA signal is asserted. After the measured temperature falls below the value in this register, the MOSFET may be switched back on with the OPERATION command. A single temperature measurement is an average of 16 round-robin cycles. Therefore, the minimum temperature fault detection time is 16 ms.

**TABLE 5. OT_FAULT_LIMIT Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFEh | Overtemperature Fault Threshold Value | 0960h (150°C) |
| 0FFFh | Overtemperature Fault detection disabled | n/a |

### OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT is a standard PMBus™ command that allows configuring or reading the threshold for the Overtemperature Warning detection. Reading and writing to this register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table. Accesses to this command should use the PMBus™ read or write word protocol. If the measured temperature exceeds this value, an overtemperature warning is triggered, the OT Warn flags are set in the respective registers, and the SMBA signal is asserted. A single temperature measurement is an average of 16 round-robin cycles. Therefore, the minimum temperature warn detection time is 16 ms.

**TABLE 6. OT_WARN_LIMIT Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFEh | Overtemperature Warn Threshold Value | 07D0h (125°C) |
| 0FFFh | Overtemperature Warn detection disabled | n/a |

### VIN_OV_WARN_LIMIT (57h)

The VIN_OV_WARN_LIMIT is a standard PMBus™ command that allows configuring or reading the threshold for the VIN Over-voltage Warning detection. Reading and writing to this register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table. Accesses to this command should use the PMBus™ read or write word protocol. If the measured value of VIN rises above the value in this register, VIN OV Warn flags are set in the respective registers, and the SMBA signal is asserted.

**TABLE 7. VIN_OV_WARN_LIMIT Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFEh | VIN Over-voltage Warning detection threshold | 0FFFh (disabled) |
| 0FFFh | VIN Over-voltage Warning disabled | n/a |

**TABLE 8. VIN_UV_WARN_LIMIT Register**

| Value | Meaning | Default |
|---|---|---|
| 1h – 0FFFh | VIN Under-voltage Warning detection threshold | 0000h (disabled) |
| 0000h | VIN Under-voltage Warning disabled | n/a |

### VIN_UV_WARN_LIMIT (58h)

The VIN_UV_WARN_LIMIT is a standard PMBus™ command that allows configuring or reading the threshold for the VIN Under-voltage Warning detection. Reading and writing to this register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table. Accesses to this command should use the PMBus™ read or write word protocol. If the measured value of VIN falls below the value in this register, VIN UV Warn flags are set in the respective registers, and the $\overline{\text{SMBA}}$ signal is asserted.

### STATUS_BYTE (78h)

The STATUS_BYTE command is a standard PMBus™ command that returns the value of a number of flags indicating the state of the LM25066. Accesses to this command should use the PMBus™ read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

**TABLE 9. STATUS_BYTE Definitions**

| Bit | NAME | Meaning | Default |
|---|---|---|---|
| 7 | BUSY | Not Supported, always 0 | 0 |
| 6 | OFF | This bit is asserted if the MOSFET is not switched on for any reason. | 1 |
| 5 | VOUT OV | Not Supported, always 0 | 0 |
| 4 | IOUT OC | Not Supported, always 0 | 0 |
| 3 | VIN UV FAULT | A VIN Under-voltage Fault has occurred | 1 |
| 2 | TEMPERATURE | A Temperature Fault or Warning has occurred | 0 |
| 1 | CML | A Communication Fault has occurred | 0 |
| 0 | None of the Above | A fault or warning not listed in bits [7:1] has occurred | 1 |

### STATUS_WORD (79h)

The STATUS_WORD command is a standard PMBus™ command that returns the value of a number of flags indicating the state of the LM25066. Accesses to this command should use the PMBus™ read word protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued. The INPUT and VIN UV FAULT flags will default to 1 on startup. However, they will be cleared to 0 after the first time the input voltage exceeds the resistor programmed UVLO threshold.

**TABLE 10. STATUS_WORD Definitions**

| Bit | NAME | Meaning | Default |
|---|---|---|---|
| 15 | VOUT | An output voltage fault or warning has occurred | 0 |
| 14 | IOUT/POUT | Not Supported, always 0 | 0 |
| 13 | INPUT | An input voltage or current fault has occurred | 1 |
| 12 | MFR | A Manufacturer Specific Fault or Warning has occurred | 1 |
| 11 | $\overline{\text{POWER GOOD}}$ | The Power Good signal has been negated | 1 |
| 10 | FANS | Not Supported, always 0 | 0 |
| 9 | OTHER | Not Supported, always 0 | 0 |
| 8 | UNKNOWN | Not Supported, always 0 | 0 |
| 7 | BUSY | Not Supported, always 0 | 0 |
| 6 | OFF | This bit is asserted if the MOSFET is not switched on for any reason. | 1 |
| 5 | VOUT OV | Not Supported, always 0 | 0 |
| 4 | IOUT OC | Not Supported, always 0 | 0 |
| 3 | VIN UV FAULT | A VIN Under-voltage Fault has occurred | 1 |
| 2 | TEMPERATURE | A Temperature Fault or Warning has occurred | 0 |
| 1 | CML | A Communication Fault has occurred | 0 |
| 0 | None of the Above | A fault or warning not listed in bits [7:1] has occurred | 1 |

**STATUS_VOUT (7Ah)**

The STATUS_VOUT command is a standard PMBus™ command that returns the value of the VOUT UV Warning flag. Accesses to this command should use the PMBus™ read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

**TABLE 11. STATUS_VOUT Definitions**

| Bit | NAME | Meaning | Default |
|---|---|---|---|
| 7 | VOUT OV Fault | Not Supported, always 0 | 0 |
| 6 | VOUT OV Warn | Not Supported, always 0 | 0 |
| 5 | VOUT UV Warn | A VOUT Under-voltage Warning has occurred | 0 |
| 4 | VOUT UV Fault | Not Supported, always 0 | 0 |
| 3 | VOUT Max | Not Supported, always 0 | 0 |
| 2 | TON Max Fault | Not Supported, always 0 | 0 |
| 1 | TOFF Max Fault | Not Supported, always 0 | 0 |
| 0 | VOUT Tracking Error | Not Supported, always 0 | 0 |

**STATUS_INPUT (7Ch)**

The STATUS_INPUT command is a standard PMBus™ command that returns the value of a number of flags related to input voltage, current, and power. Accesses to this command should use the PMBus™ read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued. The VIN UV Warn flag will default to 1 on startup. However, it will be cleared to 0 after the first time the input voltage exceeds the resistor programmed UVLO threshold.

**TABLE 12. STATUS_INPUT Definitions**

| Bit | NAME | Meaning | Default |
|---|---|---|---|
| 7 | VIN OV Fault | A VIN Over-voltage Fault has occurred | 0 |
| 6 | VIN OV Warn | A VIN Over-voltage Warning has occurred | 0 |
| 5 | VIN UV Warn | A VIN Under-voltage Warning has occurred | 1 |
| 4 | VIN UV Fault | A VIN Under-voltage Fault has occurred | 0 |
| 3 | Insufficient Voltage | Not Supported, always 0 | 0 |
| 2 | IIN OC Fault | An IIN Over-current Fault has occurred | 0 |
| 1 | IIN OC Warn | An IIN Over-current Warning has occurred | 0 |
| 0 | PIN OP Warn | A PIN Over-power Warning has occurred | 0 |

**STATUS_TEMPERATURE (7Dh)**

The STATUS_TEMPERATURE is a standard PMBus™ command that returns the value of the of a number of flags related to the temperature telemetry value. Accesses to this command should use the PMBus™ read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

**TABLE 13. STATUS_TEMPERATURE Definitions**

| Bit | NAME | Meaning | Default |
|---|---|---|---|
| 7 | Overtemp Fault | An Overtemperature Fault has occurred | 0 |
| 6 | Overtemp Warn | An Overtemperature Warning has occurred | 0 |
| 5 | Undertemp Warn | Not Supported, always 0 | 0 |
| 4 | Undertemp Fault | Not Supported, always 0 | 0 |
| 3 | reserved | Not Supported, always 0 | 0 |
| 2 | reserved | Not Supported, always 0 | 0 |
| 1 | reserved | Not Supported, always 0 | 0 |
| 0 | reserved | Not Supported, always 0 | 0 |

### STATUS_CML (7Eh)

The STATUS_CML command is a standard PMBus™ command that returns the value of a number of flags related to communication faults. Accesses to this command should use the PMBus™ read byte protocol. To clear bits in this register, a CLEAR_FAULTS command should be issued.

**TABLE 14. STATUS_CML Definitions**

| Bit | NAME | Default |
|---|---|---|
| 7 | Invalid or unsupported command received | 0 |
| 6 | Invalid or unsupported data received | 0 |
| 5 | Packet Error Check failed | 0 |
| 4 | Memory Fault Detected Not supported, always 0 | 0 |
| 3 | Processor Fault Detected Not supported, always 0 | 0 |
| 2 | Reserved Not supported, always 0 | 0 |
| 1 | Miscellaneous communications fault has occurred | 0 |
| 0 | Other memory or logic fault detected Not supported, always 0 | 0 |

### STATUS_MFR_SPECIFIC (80h)

The STATUS_MFR_SPECIFIC command is a standard PMBus™ command that contains manufacturer specific status information. Accesses to this command should use the PMBus™ read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command should be issued.

**TABLE 15. STATUS_MFR_SPECIFIC Definitions**

| Bit | Meaning | Default |
|---|---|---|
| 7 | Circuit breaker fault | 0 |
| 6 | Ext. MOSFET shorted fault | 0 |
| 5 | Not Supported, Always 0 | 0 |
| 4 | Defaults loaded | 1 |
| 3 | Not supported: Always 0 | 0 |
| 2 | Not supported: Always 0 | 0 |
| 1 | Not supported: Always 0 | 0 |
| 0 | Not supported: Always 0 | 0 |

### READ_VIN (88h)

The READ_VIN command is a standard PMBus™ command that returns the 12-bit measured value of the input voltage. Reading this register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table. Accesses to this command should use the PMBus™ read word protocol. This value is also used internally for the VIN Over and Under Voltage Warning detection.

**TABLE 16. READ_VIN Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFFh | Measured value for VIN | 0000h |

### READ_VOUT (8Bh)

The READ_VOUT command is a standard PMBus™ command that returns the 12-bit measured value of the output voltage. Reading this register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table. Accesses to this command should use the PMBus™ read word protocol. This value is also used internally for the VOUT Under Voltage Warning detection.

**TABLE 17. READ_VOUT Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFFh | Measured value for VOUT | 0000h |

### READ_TEMPERATURE_1 (8Dh)

The READ_TEMPERATURE _1 command is a standard PMBus™ command that returns the signed value of the temperature measured by the external temperature sense diode. Reading this register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table. Accesses to this command should use the PMBus™ read word protocol. This value is also used internally for the Over Temperature Fault and Warning detection. This data has a range of -256°C to + 255°C after the coefficients are applied.

**TABLE 18. READ_TEMPERATURE_1 Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFFh | Measured value for TEMPERATURE | 0000h |

### MFR_ID (99h)

The MFR_ID command is a standard PMBus™ command that returns the identification of the manufacturer. To read the MFR_ID, use the PMBus™ block read protocol.

**TABLE 19. MFR_ID Register**

| Byte | Name | Value |
|---|---|---|
| 0 | Number of bytes | 03h |
| 1 | MFR ID-1 | 4Eh ‘N’ |
| 2 | MFR ID-2 | 53h ‘S’ |
| 3 | MFR ID-3 | 43h ‘C’ |

### MFR_MODEL (9Ah)

The MFR_MODEL command is a standard PMBus™ command that returns the part number of the chip. To read the MFR_MODEL, use the PMBus™ block read protocol.

**TABLE 20. MFR_MODEL Register**

| Byte | Name | Value |
|---|---|---|
| 0 | Number of bytes | 08h |
| 1 | MFR ID-1 | 4Ch ‘L’ |
| 2 | MFR ID-2 | 4Dh ‘M’ |
| 3 | MFR ID-3 | 32h ‘2’ |
| 4 | MFR ID-4 | 35h ‘5’ |
| 5 | MFR ID-5 | 30h ‘0’ |
| 6 | MFR ID-6 | 36h ‘6’ |
| 7 | MFR ID-7 | 36h ‘6’ |
| 8 | MFR ID-8 | 00h |

### MFR_REVISION (9Bh)

The MFR_REVISION command is a standard PMBus™ command that returns the revision level of the part. To read the MFR_REVISION, use the PMBus™ block read protocol.

**TABLE 21. MFR_REVISION Register**

| Byte | Name | Value |
|---|---|---|
| 0 | Number of bytes | 02h |
| 1 | MFR ID-1 | 41h ‘A’ |
| 2 | MFR ID-2 | 41h ‘A’ |

## Manufacturer Specific PMBus™ Commands

### MFR_SPECIFIC_00: READ_VAUX (D0h)

The READ_VAUX command will report the 12-bit ADC measured auxiliary voltage. Voltages greater than or equal to 1.16V to ground will be reported at plus full scale (0FFFh). Voltages less than or equal to 0V referenced to ground will be reported as 0 (0000h). Coefficients for the VAUX value are dependent on the value of the external divider (if used). To read data from the READ_VAUX command, use the PMBus™ Read Word protocol.

**TABLE 22. READ_VAUX Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFFh | Measured value for VAUX input | 0000h |

### MFR_SPECIFIC_01: MFR_READ_IIN (D1h)

The MFR_READ_IIN command will report the 12-bit ADC measured current sense voltage. To read data from the MFR_READ_IIN command, use the PMBus™ Read Word protocol. Reading this register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table. Please see the section on coefficient calculations to calculate the values to use.

**TABLE 23. MFR_READ_IIN Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFFh | Measured value for input current sense voltage | 0000h |

### MFR_SPECIFIC_02: MFR_READ_PIN (D2h)

The MFR_ READ_PIN command will report the upper 12 bits of the VIN x IIN product as measured by the 12-bit ADC. To read data from the MFR_READ_PIN command, use the PMBus™ Read Word protocol. Reading this register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table. Please see the section on coefficient calculations to calculate the values to use.

**TABLE 24. MFR_READ_PIN Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFFh | Value for input current x input voltage | 0000h |

### MFR_SPECIFIC_03: MFR_IN_OC_WARN_LIMIT (D3h)

The MFR_IIN_OC_ WARN_LIMIT PMBus™ command sets the input over-current warning threshold. In the event that the input current rises above the value set in this register, the IIN over-current flags are set in the status registers and the $\overline{\text{SMBA}}$ is asserted. To access the MFR_IIN_ OC_WARN_LIMIT register, use the PMBus™ Read/Write Word protocol. Reading/writing to this register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table.

**TABLE 25. MFR_IIN_OC_WARN_LIMIT Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFEh | Value for input over-current warn limit | 0FFFh |
| 0FFFh | Input over-current warning disabled | n/a |

### MFR_SPECIFIC_04: MFR_PIN_OP_WARN_LIMIT (D4h)

The MFR_PIN_OP_WARN_LIMIT PMBus™ command sets the input over-power warning threshold. In the event that the input power rises above the value set in this register, the PIN Over-power flags are set in the status registers and the $\overline{\text{SMBA}}$ is asserted. To access the MFR_PIN_OP_WARN_LIMIT register, use the PMBus™ Read/Write Word protocol. Reading/writing to this register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table.

**TABLE 26. MFR_PIN_OP_WARN_LIMIT Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFEh | Value for input over-power warn limit | 0FFFh |
| 0FFFh | Input over-power warning disabled | n/a |

### MFR_SPECIFIC_05: READ_PIN_PEAK (D5h)

The READ_PIN_PEAK command will report the maximum input power measured since a Power-On-Reset or the last CLEAR_PIN_PEAK command. To access the READ_PIN_PEAK command, use the PMBus™ Read Word protocol. Use the coefficients shown in the Telemetry and Warning Coefficients Table.

**TABLE 27. READ_PIN_PEAK Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFEh | Maximum value for input current x input voltage since reset or last clear | 0h |

### MFR_SPECIFIC_06: CLEAR_PIN_PEAK (D6h)

The CLEAR_PIN_PEAK command will clear the PIN_PEAK register. This command uses the PMBus™ Send Byte protocol.

### MFR_SPECIFIC_07: GATE_MASK (D7h)

The GATE_MASK register allows the hardware to prevent fault conditions from switching off the MOSFET. When the bit is high, the corresponding FAULT has no control over the MOSFET gate. All status registers will still be updated (STATUS, DIAGNOSTIC) and an $\overline{\text{SMBA}}$ will still be issued. This register is accessed with the PMBus™ Read / Write Byte protocol.

**Warning:** **Inhibiting the MOSFET switch off in response to over-current or circuit breaker fault conditions will likely result in the destruction of the MOSFET! This functionality should be used with great care and supervision!**

**TABLE 28. GATE_MASK Register**

| Bit | NAME | Default |
|---|---|---|
| 7 | Not used, always 0 | 0 |
| 6 | Not used, always 0 | 0 |
| 5 | VIN UV FAULT | 0 |
| 4 | VIN OV FAULT | 0 |
| 3 | IIN/PFET FAULT | 0 |
| 2 | OVERTEMP FAULT | 0 |
| 1 | Not used, always 0 | 0 |
| 0 | CIRCUIT BREAKER FAULT | 0 |

The IIN/PFET Fault refers to the input current fault and the MOSFET power dissipation fault. There is no input power fault detection, only input power warning detection.

### MFR_SPECIFIC_08: ALERT_MASK (D8h)

The ALERT_MASK is used to mask the $\overline{\text{SMBA}}$ when a specific fault or warning has occurred. Each bit corresponds to one of the 14 different analog and digital faults or warnings that would normally result in an $\overline{\text{SMBA}}$ being set. When the corresponding bit is high, that condition will not cause the $\overline{\text{SMBA}}$ to be asserted. If that condition occurs, the registers where that condition is captured will still be updated (STATUS registers, DIAGNOSTIC_WORD) and the external MOSFET gate control will still be active (VIN_OV_FAULT, VIN_UV_FAULT, IIN/PFET_FAULT, CB_FAULT, OT_FAULT). This register is accessed with the PMBus™ Read / Write Word protocol. The VIN UNDERVOLTGE FAULT flag will default to 1 on startup. However, it will be cleared to 0 after the first time the input voltage exceeds the resistor programmed UVLO threshold.

**TABLE 29. ALERT_MASK Definitions**

| BIT | NAME | DEFAULT |
|---|---|---|
| 15 | VOUT UNDERVOLTAGE WARN | 0 |
| 14 | IIN LIMIT Warn | 0 |
| 13 | VIN UNDERVOLTAGE WARN | 0 |
| 12 | VIN OVERVOLTAGE WARN | 0 |
| 11 | $\overline{\text{POWER GOOD}}$ | 1 |
| 10 | OVERTEMP WARN | 0 |
| 9 | Not Used | 0 |
| 8 | OVERPOWER LIMIT WARN | 0 |
| 7 | Not Used | 0 |
| 6 | EXT_MOSFET_SHORTED | 0 |
| 5 | VIN UNDERVOLTAGE FAULT | 1 |
| 4 | VIN OVERVOLTAGE FAULT | 0 |
| 3 | IIN/PFET FAULT | 0 |
| 2 | OVERTEMPERATURE FAULT | 0 |
| 1 | CML FAULT (Communications Fault) | 0 |
| 0 | CIRCUIT BREAKER FAULT | 0 |

### MFR_SPECIFIC_09: DEVICE_SETUP (D9h)

The DEVICE_SETUP command may be used to override pin settings to define operation of the LM25066 under host control. This command is accessed with the PMBus™ read / write byte protocol.

**TABLE 30. DEVICE_SETUP Byte Format**

| Bit | Name | Meaning |
|---|---|---|
| 7:5 | Retry setting | 111 = Unlimited retries |
| | | 110 = Retry 16 times |
| | | 101 = Retry 8 times |
| | | 100 = Retry 4 times |
| | | 011 = Retry 2 times |
| | | 010 = Retry 1 time |
| | | 001 = No retries |
| | | 000 = Pin configured retries |
| 4 | Current limit setting | 0 = Low setting (25mV) |
| | | 1 = High setting (46mV) |
| 3 | CB/CL Ratio | 0 = Low setting (1.8x) |
| | | 1 = High setting (3.6x) |
| 2 | Current limit Configuration | 0 = Use pin settings |
| | | 1 = Use SMBus settings |
| 1 | Circuit breaker Configuration | 0 = Use pin settings |
| | | 1 = Use SMBus settings |
| 0 | Unused | |

In order to configure the Current Limit Setting via this register, it is necessary to set the Current Limit Configuration bit (2) to 1 to enable the register to control the current limit function and the Current Limit Setting bit (4) to select the desired setting. Similarly, in order to control the Circuit Breaker via this register, it is necessary to set the Circuit Breaker Configuration bit (1) to 1 to enable the register to control the Circuit Breaker Setting, and the Circuit Breaker / Current Limit Ratio bit (3) to the desired value. If the respective Configuration bits are not set, the Settings will be ignored and the pin set values used.

The Current Limit Configuration effects the coefficients used for the Current and Power measurements and warning registers.

### MFR_SPECIFIC_10: BLOCK_READ (DAh)

The BLOCK_READ command concatenates the DIAGNOSTIC_WORD with input and output telemetry information (IIN, VOUT, VIN, PIN) as well as TEMPERATURE to capture all of the operating information of the LM25066 in a single SMBus transaction. The block is 12 bytes long with telemetry information being sent out in the same manner as if an individual READ_XXX command had been issued (shown below). The contents of the block read register are updated every clock cycle (85ns) as long as the SMBus interface is idle. BLOCK_READ also guarantees that the VIN, VOUT, IIN and PIN measurements are all time-aligned whereas there is a chance they may not be if read with individual PMBus™ commands.

The Block Read command is read via the PMBus™ block read protocol.

**TABLE 31. BLOCK_READ Register Format**

| | |
|---|---|
| Byte Count (always 12) | (1 byte) |
| DIAGNOSTIC_WORD | (1 Word) |
| IIN_BLOCK | (1 Word) |
| VOUT_BLOCK | (1 Word) |
| VIN_BLOCK | (1 Word) |
| PIN_BLOCK | (1 Word) |
| TEMP_BLOCK | (1 Word) |

### MFR_SPECIFIC_11: SAMPLES_FOR_AVG (DBh)

The SAMPLES_FOR_AVERAGE is a manufacturer specific command for setting the number of samples used in computing the average values for IIN, VIN, VOUT, PIN. The decimal equivalent of the AVGN nibble is the power of 2 samples (e.g. AVGN=12 equates to 4096 samples used in computing the average). The LM25066 supports average numbers of 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096. The SAMPLES_FOR_AVG number applies to average values of IIN, VIN, VOUT, PIN simultaneously. The LM25066 uses simple averaging. This is accomplished by summing consecutive results up to the number programmed, then dividing by the number of samples. Averaging is calculated according to the following sequence:

$$Y = (X_{(N)} + X_{(N-1)} + ... + X_{(0)}) / 2^{AVGN}$$

When the averaging has reached the end of a sequence (for example, 4096 samples are averaged), then a whole new sequence begins that will require the same number of samples (in this example, 4096) to be taken before the new average is ready.

**TABLE 32. SAMPLES_FOR_AVG Register**

| AVGN | $N=2^N$ averages | Averaging/Register Update Period (ms) |
|---|---|---|
| 0000 | 1 | 1 |
| 0001 | 2 | 2 |
| 0010 | 4 | 4 |
| 0011 | 8 | 8 |
| 0100 | 16 | 16 |
| 0101 | 32 | 32 |
| 0110 | 64 | 64 |
| 0111 | 128 | 128 |
| 1000 | 256 | 256 |
| 1001 | 512 | 512 |
| 1010 | 1024 | 1024 |
| 1011 | 2048 | 2048 |
| 1100 | 4096 | 4096 |

Note that a change in the SAMPLES_FOR_AVG register will not be reflected in the average telemetry measurements until the present averaging interval has completed. The default setting for AVGN is 0000 and therefore the average telemetry will mirror the instantaneous telemetry until a value higher than zero is programmed.

The SAMPLES_FOR_AVG register is accessed via the PMBus™ read / write byte protocol.

**TABLE 33. SAMPLES_FOR_AVG Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0Ch | Exponent (AVGN) for number of samples to average over | 00h |

### MFR_SPECIFIC_12: READ_AVG_VIN (DCh)

The READ_AVG_VIN command will report the 12-bit ADC measured input average voltage. If the data is not ready, the returned value will be the previous averaged data. However, if there is no previously averaged data, the default value (0000h) will be returned. This data is read with the PMBus™ Read Word protocol. This register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table.

**TABLE 34. READ_AVG_VIN Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFFh | Average of measured values for input voltage | 0000h |

### MFR_SPECIFIC_13: READ_AVG_VOUT (DDh)

The READ_AVG_VOUT command will report the 12-bit ADC measured average output voltage. The returned value will be the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus™ Read Word protocol. This register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table.

**TABLE 35. READ_AVG_VOUT Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFFh | Average of measured values for output voltage | 0000h |

### MFR_SPECIFIC_14: READ_AVG_IIN (DEh)

The READ AVG_IIN command will report the 12-bit ADC measured current sense average voltage. The returned value will be the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus™ Read Word protocol. This register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table.

**TABLE 36. READ_AVG_IIN Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFFh | Average of measured values for current sense voltage | 0000h |

### MFR_SPECIFIC_15: READ_AVG_PIN (DFh)

The READ_AVG_PIN command will report the upper 12 bits of the average VIN x IIN product as measured by the 12-bit ADC. You will read the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus™ Read Word protocol. This register should use the coefficients shown in the Telemetry and Warning Conversion Coefficients Table.

**TABLE 37. READ_AVG_PIN Register**

| Value | Meaning | Default |
|---|---|---|
| 0h – 0FFFh | Average of measured value for input voltage x input current sense voltage | 0000h |

### MFR_SPECIFIC_16: BLACK_BOX_READ (E0h)

The BLACK_BOX_READ command retrieves the BLOCK_READ data which was latched in at the first assertion of $\overline{\text{SMBA}}$. It is re-armed with the CLEAR_FAULTS command. It is the same format as the BLOCK_READ registers, the only difference being that its contents are updated with the $\overline{\text{SMBA}}$ edge rather than the internal clock edge. This command is read with the PMBus™ Block Read protocol.

### MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h)

The READ_DIAGNOSTIC_WORD PMBus command will report all of the LM25066 faults and warnings in a single read operation. The standard response to the assertion of the $\overline{\text{SMBA}}$ signal of issuing multiple read requests to various status registers can be replaced by a single word read to the DIAGNOSTIC_WORD register. The READ_DIAGNOSTIC_WORD command should be read with the PMBus™ Read Word protocol. The DIAGNOSTIC_WORD is also returned in the BLOCK_READ, BLACK_BOX_READ, and AVG_BLOCK_READ operations.

**TABLE 38. READ_DIAGNOSTIC_WORD Format**

| Bit | Meaning | Default |
|---|---|---|
| 15 | VOUT_UNDERVOLTAGE_WARN | 0 |
| 14 | IIN_OP_WARN | 0 |
| 13 | VIN_UNDERVOLTAGE_WARN | 0 |
| 12 | VIN_OVERVOLTAGE_WARN | 0 |
| 11 | $\overline{\text{POWER GOOD}}$ | 1 |
| 10 | OVER_TEMPERATURE_WARN | 0 |
| 9 | TIMER_LATCHED_OFF | 0 |
| 8 | EXT_MOSFET_SHORTED | 0 |
| 7 | CONFIG_PRESET | 1 |
| 6 | DEVICE_OFF | 1 |
| 5 | VIN_UNDERVOLTAGE_FAULT | 1 |
| 4 | VIN_OVERVOLTAGE_FAULT | 0 |
| 3 | IIN_OC/PFET_OP_FAULT | 0 |
| 2 | OVER_TEMPERATURE_FAULT | 0 |
| 1 | CML_FAULT | 0 |
| 0 | CIRCUIT_BREAKER_FAULT | 0 |

### MFR_SPECIFIC_18: AVG_BLOCK_READ (E2h)

The AVG_BLOCK_READ command concatenates the DIAGNOSTIC_WORD with input and output average telemetry information (IIN, VOUT, VIN, PIN) as well as TEMPERATURE to capture all of the operating information of the part in a single PMBus™ transaction. The block is 12 bytes long with telemetry information being sent out in the same manner as if an individual READ_AVG_XXX command had been issued (shown below). AVG_BLOCK_READ also guarantees that the VIN, VOUT, PIN, and IIN measurements are all time-aligned whereas there is a chance they may not be if read with individual PMBus™ commands. To read data from the AVG_BLOCK_READ command, use the SMBus Block Read protocol.

**TABLE 39. AVG_BLOCK_READ Register Format**

| | |
|---|---|
| Byte Count (always 12) | (1 byte) |
| DIAGNOSTIC_WORD | (1 word) |
| AVG_IIN | (1 word) |
| AVG_VOUT | (1 word) |
| AVG_VIN | (1 word) |
| AVG_PIN | (1 word) |
| TEMPERATURE | (1 word) |

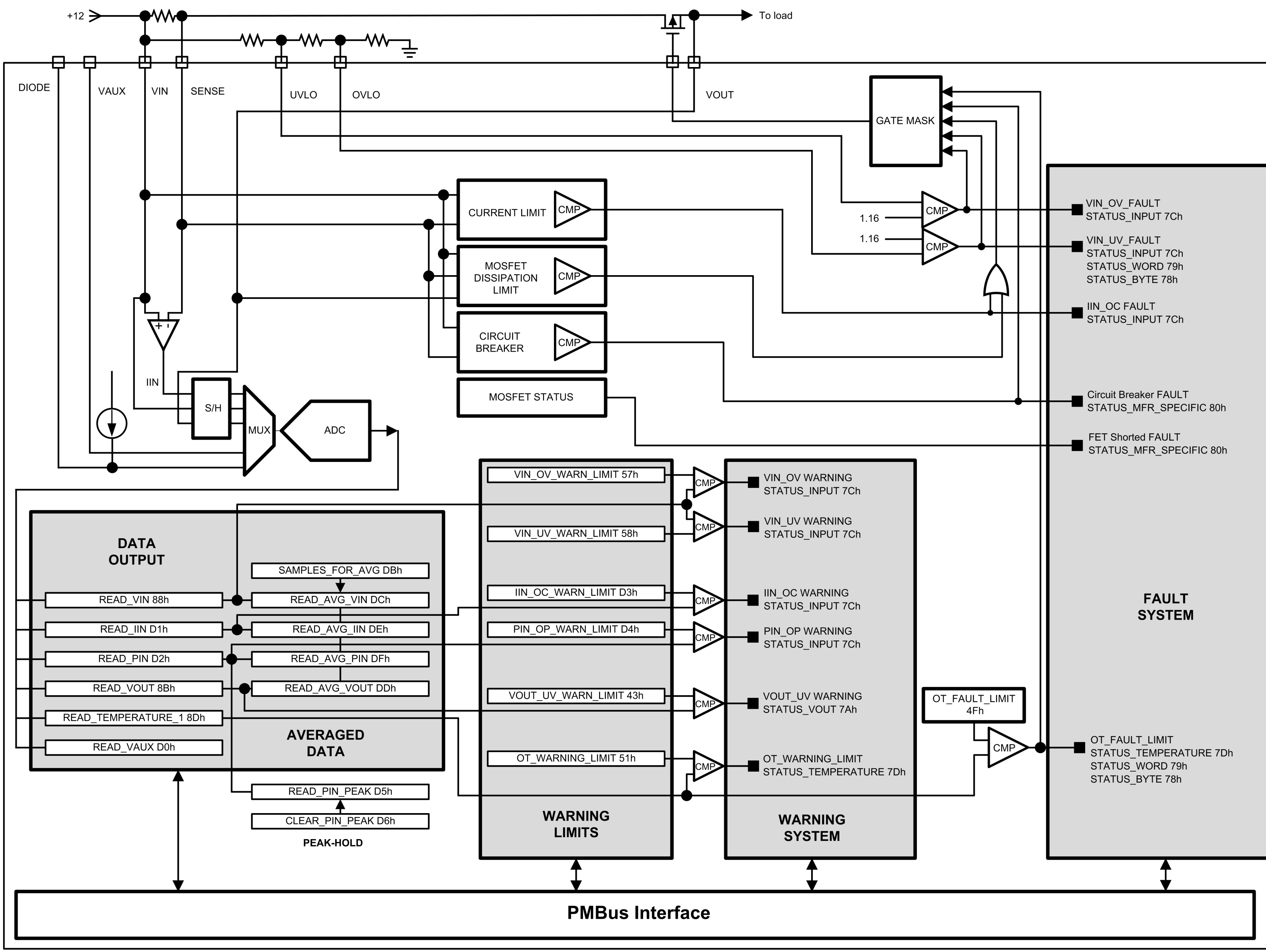



FIGURE 18. Command/Register and Alert Flow Diagram

## Reading and Writing Telemetry Data and Warning Thresholds

All measured telemetry data and user programmed warning thresholds are communicated in 12 bit two's compliment binary numbers read/written in 2 byte increments conforming to the Direct format as described in section 8.3.3 of the PMBus™ Power System Management Protocol Specification 1.1 (Part II). The organization of the bits in the telemetry or warning word is shown in Table 40, where Bit_11 is the most significant bit (MSB) and Bit_0 is the least significant bit (LSB). The decimal equivalent of all warning and telemetry words are constrained to be within the range of 0 to 4095, with the exception of temperature. The decimal equivalent value of the temperature word ranges from 0 to 65535.

**TABLE 40. Telemetry and Warning Word Format**

| Byte | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 |
| 2 | 0 | 0 | 0 | 0 | Bit_11 | Bit_10 | Bit_9 | Bit_8 |

Conversion from direct format to real world dimensions of current, voltage, power, and temperature is accomplished by determining appropriate coefficients as described in section 7.2.1 of the PMBus™ Power System Management Protocol Specification 1.1 (Part II). According to this specification, the host system converts the values received into a reading of volts, amperes, watts, or other units using the following relationship:

$$X = \frac{1}{m}(Y \times 10^{-R} - b)$$

where:

**X:** the calculated "real world" value (volts, amps, watt, etc.)

**m:** the slope coefficient

**Y:** a two byte two's complement integer received from device

**b:** the offset, a two byte two's complement integer

**R:** the exponent, a one byte two's complement integer

R is only necessary in systems where m is required to be an integer (for example, where m may be stored in a register in an integrated circuit). In those cases, R only needs to be large enough to yield the desired accuracy.

**TABLE 41. Telemetry and Warning Conversion Coefficients**

| Commands | Condition | Format | Number of Data Bytes | m | b | R | Units |
|---|---|---|---|---|---|---|---|
| READ_VIN, READ_AVG_VIN<br>VIN_OV_WARN_LIMIT<br>VIN_UV_WARN_LIMIT | | DIRECT | 2 | 22070 | -1800 | -2 | V |
| READ_VOUT, READ_AVG_VOUT<br>VOUT_UV_WARN_LIMIT | | DIRECT | 2 | 22070 | -1800 | -2 | V |
| READ_VAUX | | DIRECT | 2 | 3546 | -3 | 0 | V |
| *READ_IIN, READ_AVG_IIN<br>MFR_IIN_OC_WARN_LIMIT | CL = GND | DIRECT | 2 | 13661 | -5200 | -2 | A |
| *READ_IIN, READ_AVG_IIN<br>MFR_IIN_OC_WARN_LIMIT | CL = VDD | DIRECT | 2 | 6852 | -3100 | -2 | A |
| *READ_PIN, READ_AVG_PIN,<br>READ_PIN_PEAK<br>MFR_PIN_OP_WARN_LIMIT | CL = GND | DIRECT | 2 | 736 | -3300 | -2 | W |
| *READ_PIN, READ_AVG_PIN,<br>READ_PIN_PEAK<br>MFR_PIN_OP_WARN_LIMIT | CL = VDD | DIRECT | 2 | 369 | -1900 | -2 | W |
| READ_TEMPERATURE_1<br>OT_WARN_LIMIT<br>OT_FAULT_LIMIT | | DIRECT | 2 | 16000 | 0 | -3 | °C |

* The coefficients relating to current/power measurements and warning thresholds shown in Table 41 are normalized to a sense resistor ($R_S$) value of 1mΩ. In general, the current/power coefficients can be calculated using the relationships shown in Table 42.

**TABLE 42. Current and Power Telemetry and Warning Conversion Coefficients ($R_S$ in mΩ)**

| Commands | Condition | Format | Number of Data Bytes | m | b | R | Units |
|---|---|---|---|---|---|---|---|
| *READ_IIN, READ_AVG_IIN MFR_IIN_OC_WARN_LIMIT | CL = GND | DIRECT | 2 | 13661 x $R_S$ | -5200 | -2 | A |
| *READ_IIN, READ_AVG_IIN MFR_IIN_OC_WARN_LIMIT | CL = VDD | DIRECT | 2 | 6854 x $R_S$ | -3100 | -2 | A |
| *READ_PIN, READ_AVG_PIN, READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT | CL = GND | DIRECT | 2 | 736 x $R_S$ | -3300 | -2 | W |
| *READ_PIN, READ_AVG_PIN, READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT | CL = VDD | DIRECT | 2 | 369 x $R_S$ | -1900 | -2 | W |

Care must be taken to adjust the exponent coefficient, R, such that the value of m remains within the range of -32768 to +32767. For example, if a 5 mΩ sense resistor is used, the correct coefficients for the READ_IIN command with CL = VDD would be m = 6830, b = -310, R = -1.

**A Note on the "b" Coefficient**

Since b coefficients represent offset, for simplification b is set to zero in the following discussions.

## Reading Current

The current register actually displays a value equivalent to a voltage across the user specified sense resistor, $R_S$. The coefficients enable the data output to be converted to amps. The values shown in the example are based on having the device programmed for a 25 mV current limit threshold (CL = GND). In the 25mV range, the LSB value is 7.32 µV and the full scale range is 30.2 mV. In the 46mV range (CL = VDD), the LSB value is 14.64 µV and the full scale range in 60.4 mV.

| Step | Example |
|---|---|
| 1. Determine full scale current and shunt value based on 29.98 mV across shunt at full scale. Use either: $$I_{IN\_MAX} = \frac{30.2\text{ mV}}{R_S}$$ or: | Example: 122A application with 250 µΩ shunt. $$I_{IN\_MAX} = \frac{30.2\text{ mV}}{0.25\text{ m}\Omega} = 120.8\text{A}$$ |
| 2. Determine m': $$m'' = \frac{4095}{I_{IN\_MAX}}$$ | $$m' = \frac{4095}{120.8\text{A}} = 33.90$$ |
| 3. Determine exponent R necessary to set m' to integer value m: $$10^R = \frac{m'}{m}$$ | Select R to provide integer value of m: $$R = \log_{10}\frac{33.90}{3390}$$ R = -2 |
| 4. Final values | m = 3390 |
| | R = -2 |
| | b = 0 |

## Reading Input and Output Voltage

Coefficients for VIN and VOUT are fixed and are consistent between read telemetry measurements (e.g., READ_VIN, READ_AVG_VIN) and warning thresholds (e.g. VIN_UV_WARN_LIMIT). Input and output voltage values are read/written in Direct Format with 12-bit resolution and a 4.54 mV LSB. An example of calculating the PMBus™ coefficients for input voltage is shown below.

| Step | Example |
|---|---|
| 1. Determine m' based on full scale analog input and full scale digital range: $$m'' = \frac{4095}{V_{IN\_MAX}} = \frac{4095}{18.59V}$$ | $$m' = \frac{4095}{18.59V} = 220.26$$ |
| 2. Determine exponent R necessary to set m' to integer value m with desired accuracy: $$10^R = \frac{m'}{m}$$ | Select R to provide 5 digit accuracy for the integer value of m (which would be 21703 in this example: $$R = \log_{10}\frac{220.26}{22026}$$ R = -2 |
| 3. Final values | m = 22026 |
| | R = -2 |
| | b =0 |

## Reading Power

The power calculation of the LM25066 is a relative power calculation meaning that full scale of the power register corresponds to simultaneous full scale values in the current register and voltage register such that the power register has the following relationship based on decimal equivalents of the register contents:

$$PIN = \frac{IIN \times VIN}{4095}$$

For this reason power coefficients will also vary depending on the shunt value and must be calculated for each application. The power LSB will vary depending on shunt value according to 276 µW/Rsense for 46mV range or 138.2 µW/Rsense for 25mV range.

| Step | Example |
|---|---|
| 1. Determine full scale power from known full scale of input current and input voltage $P_{IN\_MAX} = V_{IN\_MAX} \times I_{IN\_MAX}$ | Example: 125A application with 250 µΩ shunt. $P_{IN\_MAX} = (18.59V) \times (120.8A) = 2246W$ |
| 2. Determine m': $$m' = \frac{4095}{P_{MAX}}$$ | $$m' = \frac{4095}{2246W} = 1.823$$ |
| 3. Optional: Determine exponent R necessary to set m' to integer value m with desired accuracy: $$10^R = \frac{m'}{m}$$ | Select R (in this case selected to provide 4 digit accuracy for the integer value of m): $$R = \log_{10}\frac{1.823}{1823}$$ R = -3 |
| 4. Final values | m = 1823 |
| | R = -3 |
| | b = 0 |

## Determining Telemetry Coefficients Empirically with Linear Fit

The coefficients for telemetry measurements and warning thresholds presented in Table 41 are adequate for the majority of applications. Current and power coefficients must be calculated per application as they are dependent on the value of the sense resistor, $R_S$, used. Table 42 provides the equations necessary for calculating the current and power coefficients for the general case. The small signal nature of the current measurement make it and the power measurement more susceptible to PCB parasitics than other telemetry channels. This may cause slight variations in the optimum coefficients (m, b, R) for converting from Direct Format digital values to real-world values (e.g. Amps and Watts). The optimum coefficients can be determined empirically for a specific application and PCB layout using two or more measurements of the telemetry channel of interest. The current coefficients can be determined using the following method:

1. While the LM25066 is in normal operation, measure the voltage across the sense resistor using kelvin test points and a high accuracy DVM while controlling the load current. Record the integer value returned by the READ_AVG_IIN command (with the SAMPLES_FOR_AVG set to a value greater than 0) for two or more voltages across the sense resistor. For best results, the individual READ_AVG_IIN measurements should span nearly the full scale range of the current (for example, voltage across $R_S$ of 5 mV and 20 mV).
2. Convert the measured voltages to currents by dividing them by the value of $R_S$. For best accuracy, the value of $R_S$ should be measured. Table 43 assumes a sense resistor value of 5 mΩ.

**TABLE 43. Measurements for linear fit determination of current coefficients:**

| Measured voltage across $R_S$ (V) | Measured Current (A) | READ_AVG_IIN (integer value) |
|---|---|---|
| 0.005 | 1 | 648 |
| 0.01 | 2 | 1331 |
| 0.02 | 4 | 2698 |

3. Using the spreadsheet or math program of your choice, determine the slope and the y-intercept values returned by the READ_AVG_IIN command versus the measured current. For the data shown in *Table 43*:
   READ_AVG_IIN value = slope x (Measured Current) + (y-intercept)
   slope = 683.4
   y-intercept = -35.5
4. To determine the '**m**' coefficient, simply shift the decimal point of the calculated slope to arrive at an integer with a suitable number of significant digits for accuracy (typically 4) while staying with the range of -32768 to +32767. This shift in the decimal point equates to the '**R**' coefficient. For the slope value shown above, the decimal point would be shifted to the right once hence **R** = -1.
5. Once the '**R**' coefficient has been determined, the '**b**' coefficient is found by multiplying the y-intercept by $10^{-R}$. In this case the value of **b** = -355.
   Calculated Current Coefficients:
   **m** = 6834
   **b** = -355
   **R** = -1

$$X = \frac{1}{m}(Y \times 10^{-R} - b)$$

where:

**X:** the calculated "real world" value (volts, amps, watts, temperature)

**m:** the slope coefficient, a the two byte two's complement integer

**Y:** a two byte, two's complement integer received from device

**b:** the offset, a two byte two's complement integer

**R:** the exponent, a one byte two's complement integer

The above procedure can be repeated to determine the coefficients of any telemetry channel simply by substituting measured current for some other parameter (e.g. power, voltage, etc.).

## Writing Telemetry Data

There are several locations that will require writing data if their optional usage is desired. Use the same coefficients previously calculated for your application and apply them using this method as prescribed by the PMBus™ revision section 7.2.2 "Sending a Value"

$$Y = (mX + b) \times 10^{R}$$

where:

**X:** the calculated "real world" value (volts, amps, watts, temperature)

**m:** the slope coefficient, a two byte two's complement integer

**Y:** a two byte two's complement integer received from device

**b:** the offset, a two byte two's complement integer

**R:** the exponent, a one byte two's complement integer

## PMBus™ Address Lines (ADR0, ADR1, ADR2)

The three address lines are to be set high (connect to VDD), low (connect to GND), or open to select one of 27 addresses for communicating with the LM25066. Table 44 depicts 7-bit addresses (eighth bit is read/write bit):

**TABLE 44. Device Addressing**

| ADR2 | ADR1 | ADR0 | Decoded Address |
|---|---|---|---|
| Z | Z | Z | 40h |
| Z | Z | 0 | 41h |
| Z | Z | 1 | 42h |
| Z | 0 | Z | 43h |
| Z | 0 | 0 | 44h |
| Z | 0 | 1 | 45h |
| Z | 1 | Z | 46h |
| Z | 1 | 0 | 47h |
| Z | 1 | 1 | 10h |
| 0 | Z | Z | 11h |
| 0 | Z | 0 | 12h |
| 0 | Z | 1 | 13h |
| 0 | 0 | Z | 14h |
| 0 | 0 | 0 | 15h |
| 0 | 0 | 1 | 16h |
| 0 | 1 | Z | 17h |
| 0 | 1 | 0 | 50h |
| 0 | 1 | 1 | 51h |
| 1 | Z | Z | 52h |
| 1 | Z | 0 | 53h |
| 1 | Z | 1 | 54h |
| 1 | 0 | Z | 55h |
| 1 | 0 | 0 | 56h |
| 1 | 0 | 1 | 57h |
| 1 | 1 | Z | 58h |
| 1 | 1 | 0 | 59h |
| 1 | 1 | 1 | 5Ah |

## SMBus Communications Timing Requirements

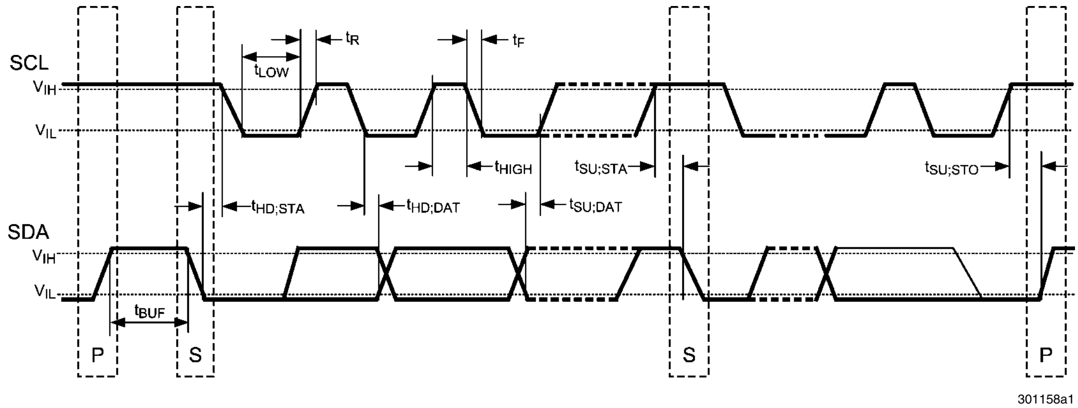



**FIGURE 19. SMBus Timing Diagram**

**TABLE 45. SMBus Timing Definition**

| Symbol | Parameter | Limits | | Units | Comments |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $F_{SMB}$ | SMBus Operating Frequency | 10 | 400 | kHz | |
| $T_{BUF}$ | Bus free time between Stop and Start Condition | 1.3 | | µs | |
| $T_{HD:STA}$ | Hold time after (Repeated) Start Condition. After this period, the first clock is generated. | 0.6 | | µs | |
| $T_{SU:STA}$ | Repeated Start Condition setup time | 0.6 | | µs | |
| $T_{SU:STO}$ | Stop Condition setup time | 0.6 | | µs | |
| $T_{HD:DAT}$ | Data hold time | 300 | | ns | |
| $T_{SU:DAT}$ | Data setup time | 100 | | ns | |
| $T_{TIMEOUT}$ | Clock low time-out | 25 | 35 | ms | (Note 8) |
| $T_{LOW}$ | Clock low period | 1.5 | | µs | |
| $T_{HIGH}$ | Clock high period | 0.6 | | µs | (Note 9) |
| $T_{LOW:SEXT}$ | Cumulative clock low extend time (slave device) | | 25 | ms | (Note 10) |
| $T_{LOW:MEXT}$ | Cumulative low extend time (master device) | | 10 | ms | (Note 11) |
| $T_F$ | Clock or Data Fall Time | 20 | 300 | ns | (Note 12) |
| $T_R$ | Clock or Data Rise Time | 20 | 300 | ns | (Note 12) |

**Note 8:** Devices participating in a transfer will timeout when any clock low exceeds the value of $T_{TIMEOUT,MIN}$ of 25 ms. Devices that have detected a timeout condition must reset the communication no later than $T_{TIMEOUT,MAX}$ of 35 ms. The maximum value must be adhered to by both a master and a slave as it incorporates the cumulative stretch limit for both a master (10ms) and a slave (25ms).

**Note 9:** $T_{HIGH\ MAX}$ provides a simple method for devices to detect bus idle conditions.

**Note 10:** $T_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop. If a slave exceeds this time, it is expected to release both its clock and data lines and reset itself.

**Note 11:** $T_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop.

**Note 12:** Rise and fall time is defined as follows:

- $T_R$ = ( $V_{ILMAX}$ – 0.15) to ($V_{IHMIN}$ + 0.15)
- $T_F$ = 0.9 VDD to ($V_{ILMAX}$ – 0.15)

## $\overline{\text{SMBA}}$ Response

The $\overline{\text{SMBA}}$ effectively has two masks:

1. The Alert Mask Register at D8h, and
2. The ARA Automatic Mask.

The ARA Automatic Mask is a mask that is set in response to a successful ARA read. An ARA read operation returns the PMBus™ address of the lowest addressed part on the bus that has its $\overline{\text{SMBA}}$ asserted. A successful ARA read means that THIS part was the one that returned its address. When a part responds to the ARA read, it releases the $\overline{\text{SMBA}}$ signal. When the last part on the bus that has an $\overline{\text{SMBA}}$ set has successfully reported its address, the $\overline{\text{SMBA}}$ signal will de-assert.

The way that the LM25066 releases the $\overline{\text{SMBA}}$ signal is by setting the ARA Automatic mask bit for all fault conditions present at the time of the ARA read. All status registers will still show the fault condition, but it will not generate an $\overline{\text{SMBA}}$ on that fault again until the ARA Automatic mask is cleared by the host issuing a Clear Fault command to this part. This should be done as a routine part of servicing an $\overline{\text{SMBA}}$ condition on a part, even if the ARA read is not done. *Figure 20* depicts a schematic version of this flow.

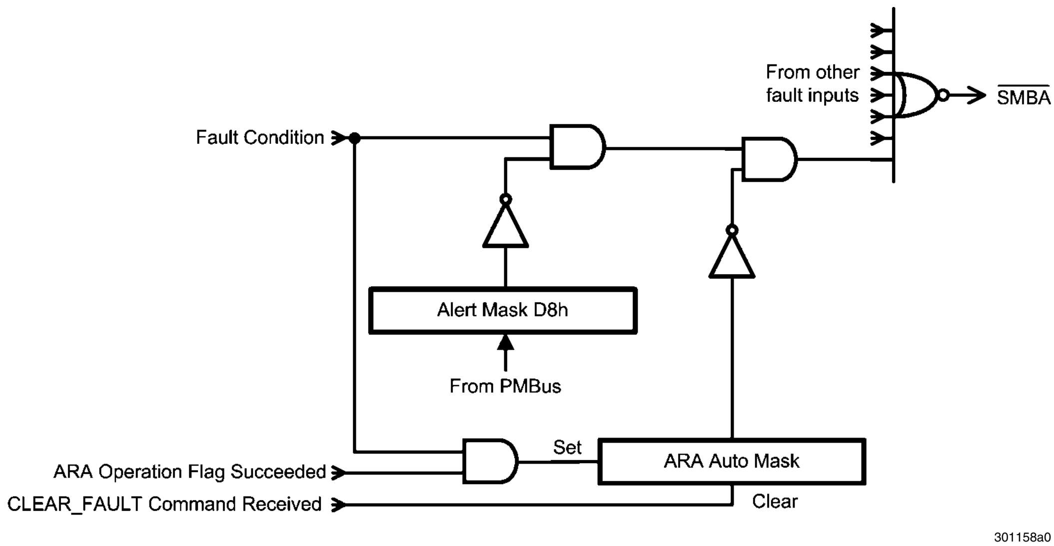
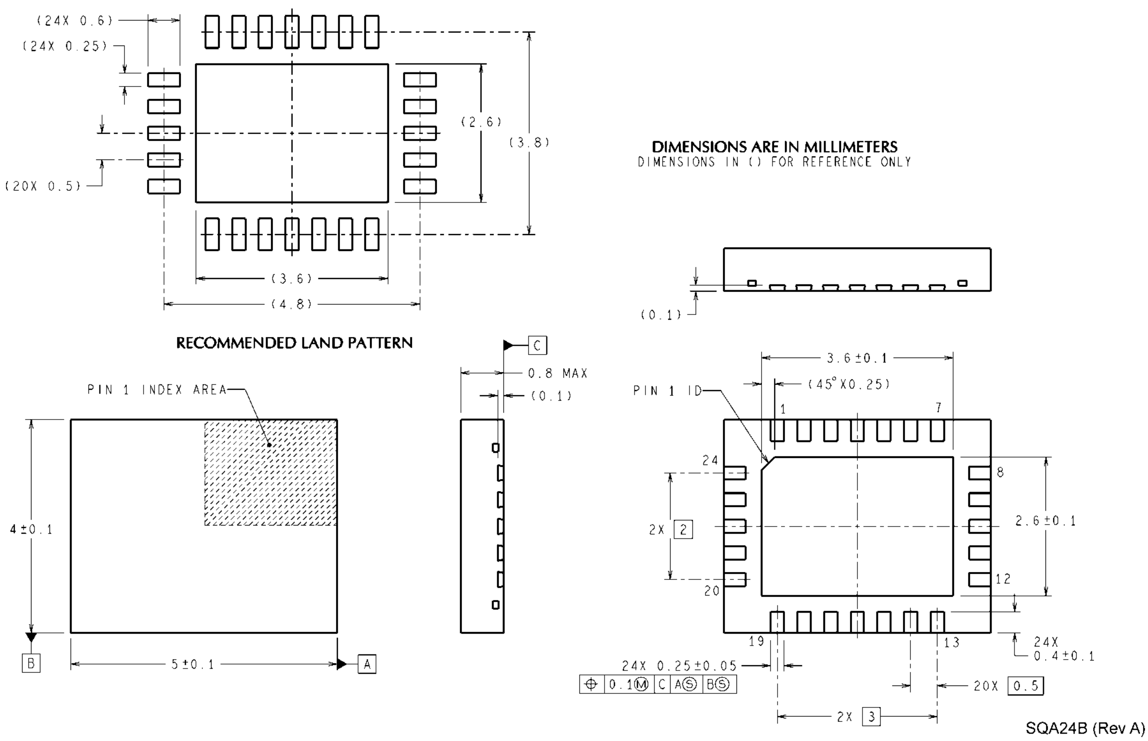



**FIGURE 20. Typical Flow Schematic for $\overline{\text{SMBA}}$ Fault**

## Physical Dimensions inches (millimeters) unless otherwise noted

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# Notes

# Notes

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