

LP5900

Application Note 1494 LP5900SD 6 Pin LLP Evaluation Board Information



Literature Number: SNVA173A

LP5900SD 6 Pin LLP Evaluation Board Information

National Semiconductor
Application Note 1494
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Introduction

This evaluation board is designed to enable the evaluation of the LP5900 Voltage Regulator. Each board is assembled and tested in the factory. This evaluation board has the 6 pin LLP package mounted.

General Description

The LP5900 is a linear regulator capable of supplying 150mA output current. Designed to meet the requirements of RF/Analog circuits, the LP5900 provides low device noise, high PSRR, low quiescent current, and low line transient response. Using new innovative design techniques the LP5900 offers class-leading noise performance without a noise bypass capacitor.

The device has been designed to work with 0.47 μ F input and output ceramic capacitors down to 0603 component size.

Operation

The input voltage, applied between V_{IN} and GND, should be at least 1.0V greater than V_{OUT} and no more than 5.5V. The minimum operating voltage is 2.5V. Loads can be connected to V_{OUT} with reference to GND. V_{OUT} and V_{IN} sense pins are provided on the board to allow accurate measurements directly onto the input and output pins of the device, eliminating any voltage drop on the PCB traces or connecting wires to the load.

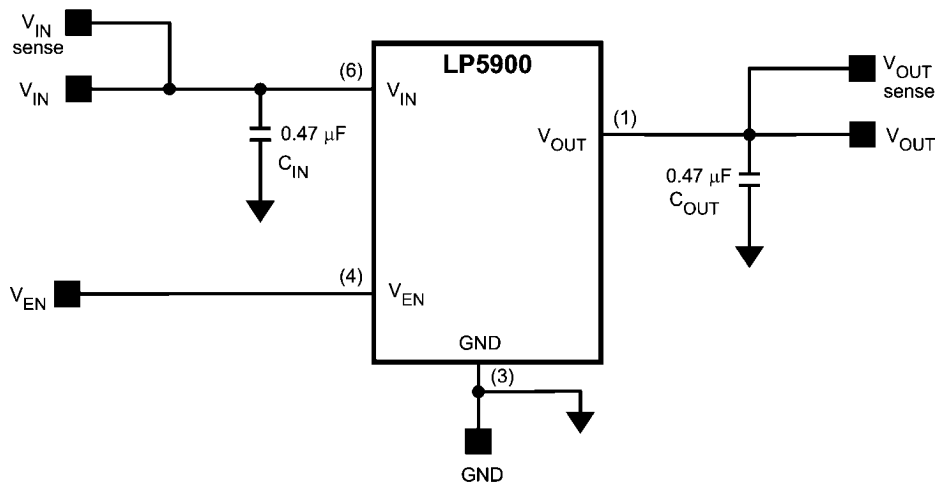
ON/OFF control is provided by a logic signal on the V_{EN} pin. A minimum of 1.2V is required at this pin to enable the LDO. The LDO will be shutdown when the V_{EN} pin is set to 0.4V or less.

In applications where the LP5900 is operated continuously from the battery then V_{IN} and V_{EN} can be tied together. However if ON/OFF control is required the V_{EN} pin should be driven from a separate signal to ensure correct operation of the fast start-up circuit. The device has a 1M Ω internal resistor from V_{EN} to GND.

Hardware

The schematic and layout of the evaluation board are given below:

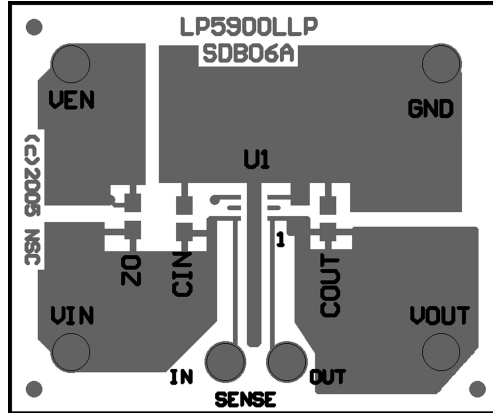
Schematic Diagram



Evaluation Board Schematic.

20196804

PCB Layout



Evaluation Board Component and Pin Layout Board Size:- 1.200" x 1.000"
20196810

Hardware

Designator	Value	Amount	Footprint	Note
U1	LP5900SD	1	SDB06A	
CIN	0.47 μ F	1	0603	X7R, X5R
COUT	0.47 μ F	1	0603	X7R, X5R
IN, OUT, IN SENSE, OUT SENSE, ON/OFF, GND	Test Pins	6		

Notes

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Notes

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