User's Guide

SLVU198A – February 2007 – Revised May 2007

Using the TPS40131EVM, A 40A Single Output Two-Phase Synchronous Buck Converter

Contents

List of Figures

List of Tables

1 Introduction

The TPS40131EVM evaluation module (EVM) is a single output two-phase synchronous buck converter. The EVM delivers 1.5V at 40A. The module uses the TPS40131 Synchronous Buck Controller.

2 Description

TPS40131EVM is designed to use a regulated 10.8V to 13.2V bus to produce a high current, regulated output. The output is capable of supplying up to 40A of load current. The TPS40131EVM is designed to demonstrate the TPS40131 in a typical regulated bus to low-voltage application while providing a number of test points to evaluate the performance of the TPS40131 in a given application.

2.1 Applications

- Point of Load Converters
- Graphics Cards
- Internet Servers
- Networking Equipment
- Telecommunications Equipment
- DC Power Distributed Systems

2.2 Features

- 10.8V – 13.2V input range
- 1.5V fixed output
- 40-A DC Steady State Current
- 380kHz switching frequency per phase
- Single Main Switch N-channel MOSFET and Two Synchronous Rectifier N-channel MOSFETs per phase
- Convenient test points for probing critical waveforms and non-invasive loop response testing

3 TPS40131EVM Electrical Performance Specifications

Table 1. TPS40131EVM Electrical and Performance Specifications

Parameter	Notes and Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS					
Input voltage range (V_{IN1})		10.8		13.2	V
Max input current	V_{IN1} = 10.8 V, I_{OUT} = 40 A		6.5		A
No-load input current	V_{IN1} = 13.2 V, I_{OUT} = 0A		35		mA
Input voltage range(V_{IN2})		4.5		5.5	V
Max input current			120		mA
OUTPUT CHARACTERISTICS					
OUTPUT (V_{OUT})					V
Output voltage			1.5		V
Output voltage regulation	Line Regulation (10.8 V < V_{IN} < 13.2 V, I_{OUT} = 40 A)			0.2%	
	Load Regulation (0A < I_{OUT} < 40 A, V_{IN} = 12 V)			0.2%	
Output voltage ripple	V_{IN} = 13.2 V, I_{OUT} = 40 A		30		mVpp
Output load current	I_{OUT}	0		40	A
Output over current				55	A
SYSTEM CHARACTERISTICS					
Switching Frequency			380		kHz
Peak efficiency	V_{OUT} = 1.5 V, 18A < I_{OUT} < 22A, V_{IN} = 12 V		88.5%		
Full load efficiency	V_{OUT} = 1.5 V, I_{OUT} = 40 A, V_{IN} = 12 V		85%		

4 Schematic

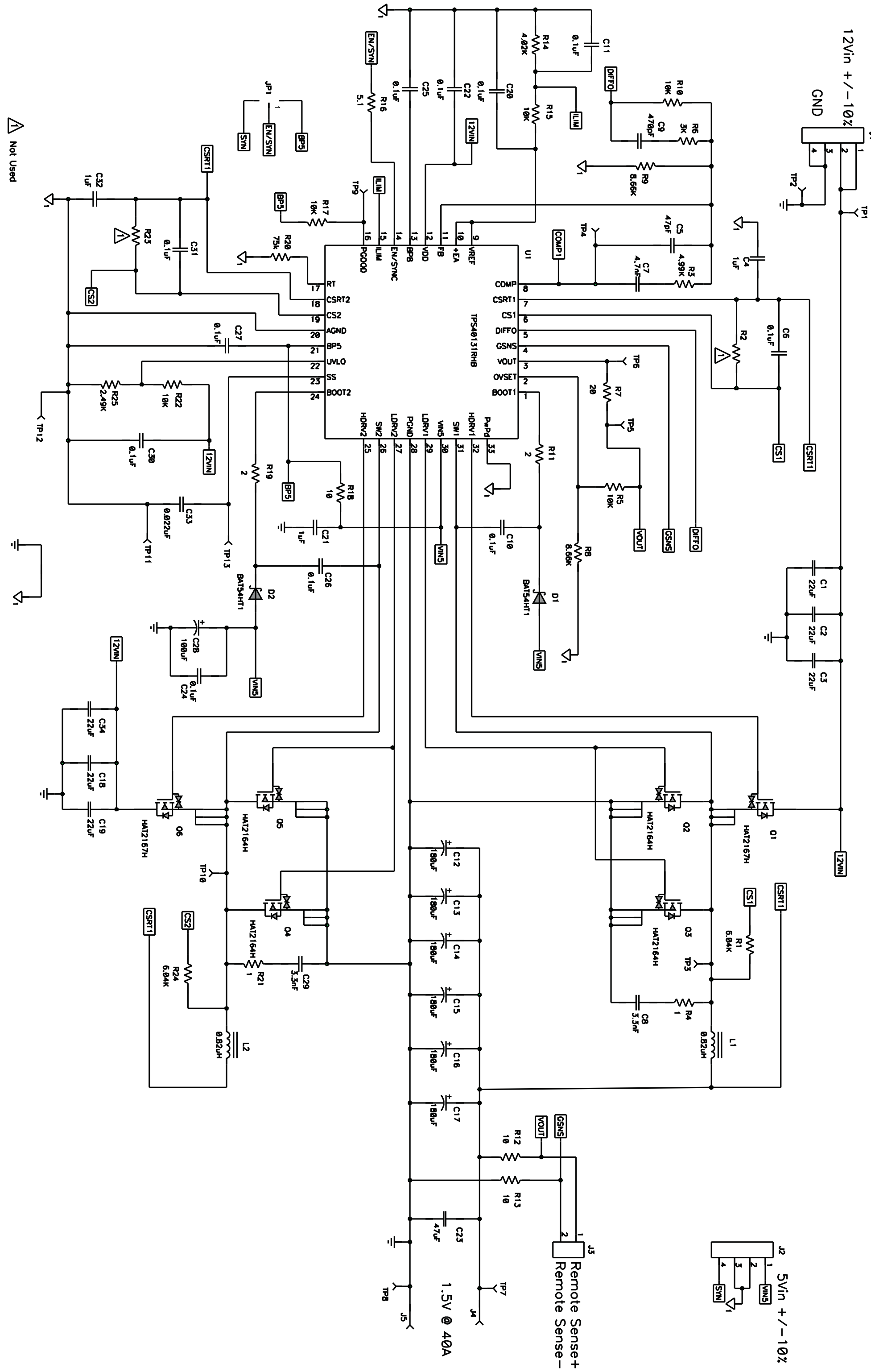

Figure 1. TPS40131EVM Power Stage/Control Schematic
For Reference Only, See Table 3: Bill of Materials for Specific Values

5 Test Set Up

5.1 Recommended Test Equipment

5.1.1 Voltage Source

The input voltage source V_{IN1} should be a 0–15 V variable DC source capable of 10 A. Connect V_{IN1} to J1 as shown in Figure 2.

The input voltage source V_{IN2} should be a 0–6 V variable DC source capable of 2 A. Connect V_{IN2} to J2 as shown in Figure 2.

5.1.2 Meters

V1: V_{IN} 0–15 V voltmeter
V2: V_{OUT} 0–5 V voltmeter
I1: I_{IN}, 0–10 A current meter

5.1.3 Loads

The output load (LOAD) should be an electronic constant current mode load capable of 0–40 A DC at 1.5 V.

5.1.4 Oscilloscope

A digital or analog oscilloscope can be used to measure the ripple voltage on V_{OUT}. The oscilloscope should be set for 1 MΩ impedance, 20MHz Bandwidth, AC coupling, 1µs/division horizontal resolution, 20mV/division vertical resolution for taking output ripple measurements. Test points TP7 and TP8 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP7 and holding the ground barrel TP8 as shown in Figure 3. Using a leaded ground connection may induce additional noise due to the large ground loop area.

5.1.5 Recommended Wire Gauge

VIN1 to J1 (12V input)
The connection between the source voltage, VIN1 and J1 of the EVM can carry as much as 10 Amps DC. The recommended wire size is 1x AWG #16 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return).

VIN2 to J2 (5V auxiliary input)
The connection between the source voltage, VIN2 and J2 of the EVM can carry as much as 1 Amps DC. The recommended wire size is 1x AWG #22 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return).

J4,J5 to LOAD (Power)
The power connection between J4, J5 of the EVM and LOAD can carry as much as 40-A DC. The minimum recommended wire size is 2x AWG #16, with the total length of wire less than 4 feet (2 feet output, 2 feet return).

5.1.6 Other

FAN
This evaluation module includes components that can get hot to the touch, because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200–400 lfm is required to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered. The EVM should not be probed while the fan is not running.

5.2 Equipment Setup

Shown in Figure 2 is the basic test set up recommended to evaluate the TPS40131EVM.

Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic (ESD) smock and safety glasses should also be worn.

5.2.1 Input Connections

1. Prior to connecting the DC input source, V_{IN1}, it is advisable to limit the source current from V_{IN1} to 10A maximum. Make sure V_{IN1} is initially set to 0V and connected as shown in Figure 2.
2. Connect V_{IN2} to J2 and set V_{IN2} to 5V.

5.2.2 Output Connections

1. Connect LOAD to J4 and J5, set LOAD to constant current mode to sink 0A DC before V_{IN1} is applied.
2. Connect voltmeter, V2, across TP7 and TP8, as shown in Figure 2.

5.2.3 Other Connections

1. Place Fan as shown in Figure 2 and turn on, making sure air is flowing across the EVM.

5.2.4 Set Up Diagram

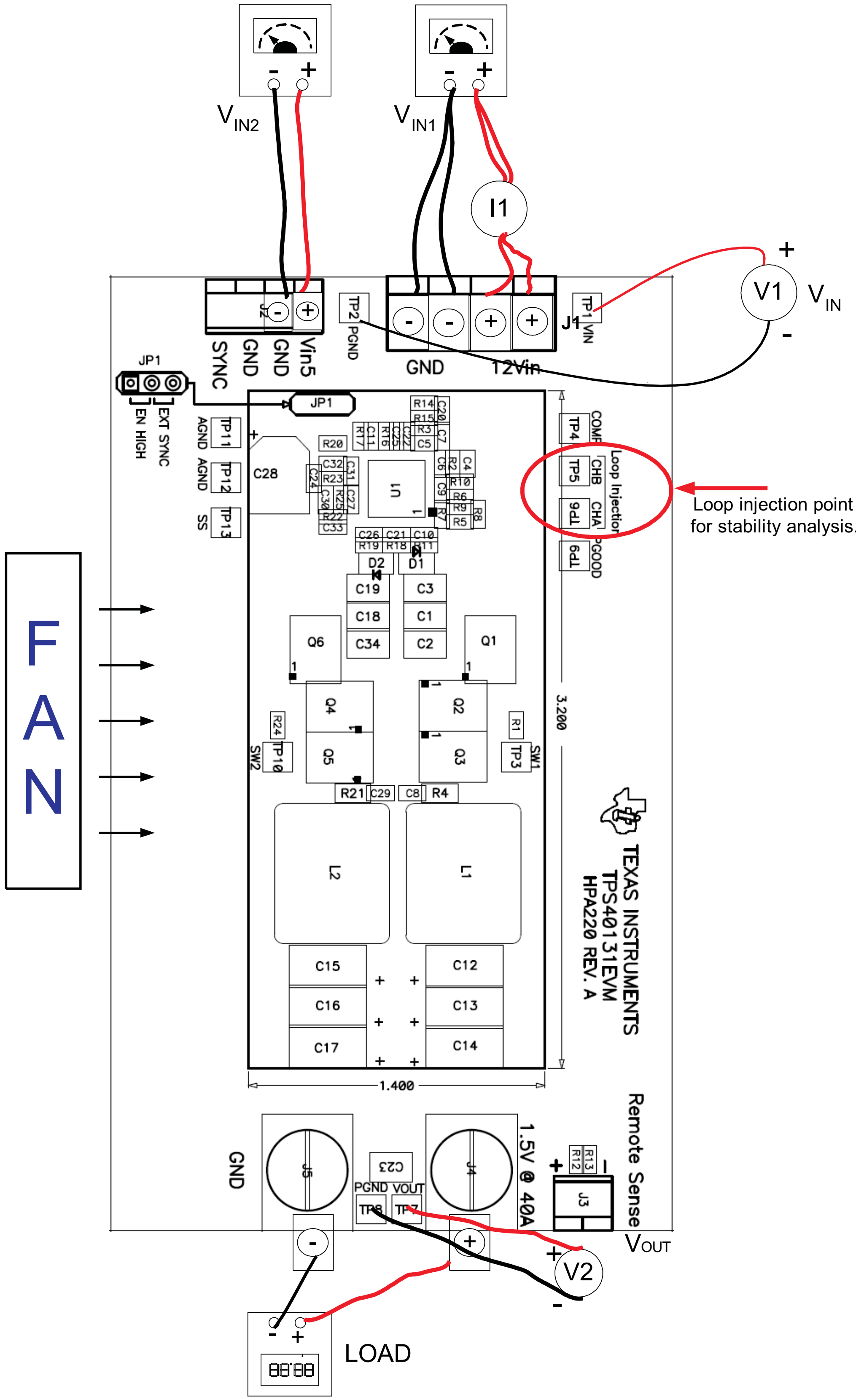

Figure 2. TPS40131EVM Recommended Test Set-Up

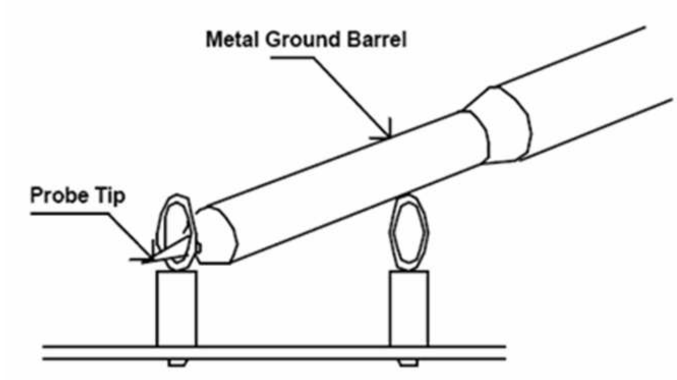

Figure 3. Output Ripple Measurement

5.3 Start Up and Test Procedure

1. Ensure LOAD is set to constant current mode and to sink 0A DC.
2. Set V_{IN2} to 5V.
3. Increase V_{IN1} from 0V to 12V, V_{OUT} should be in regulation per Table 1.
4. Vary LOAD from 0–40Adc, V_{OUT} should remain in regulation per Table 1 for all combinations of load on LOAD up to 40A.
5. Vary V_{IN1} from 10.8V to 13.2V, V_{OUT} should remain in regulation per Table 1 for all combinations of load on LOAD up to 40A.

5.4 Control Loop Gain and Phase Measurement Procedure

1. Connect 1 kHz–1MHz isolation transformer to test points marked TP5 and TP6.
2. Connect input signal amplitude measurement probe (channel A) to TP6.
3. Connect output signal amplitude measurement probe (channel B) to TP5.
4. Connect ground lead of channel A and channel B to TP11.
5. Inject 25mV or less signal through the isolation transformer.
6. Sweep the frequency from 100Hz to 1MHz with 10Hz or lower post filter.
7. The control loop gain can be measured by $20 \times \mathrm{LOG}\left(\frac{\mathrm{ChannelB}}{\mathrm{ChannelA}}\right)$.
8. Control loop phase is measured by the phase difference between Channel A an Channel B.
9. Disconnect isolation transformer from the bode plot test points before making other measurements (Signal Injection into Feedback may interfere with accuracy of other measurements).

5.5 EN/SYNC Configuration

5.5.1 EN High (Default)

Configure JP1 with a jumper as shown in Figure 4. The controller will generate its own clock and the operation is enabled.

Figure 4. Default EN Configuration

5.5.2 External Synchronization

Configure JP1 with a jumper as shown in the following figure and connect a clock source to SYNC and GND pins of J2 as shown in Figure 6. The controller will synchronize to the external clock.

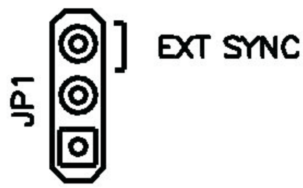

Figure 5. EN/SYNC Configuration

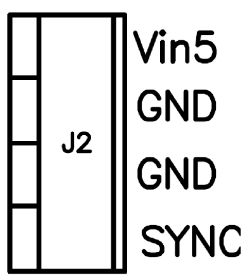

Figure 6. Connect External Clock to J2

5.6 Test Points

Several test points are located around the board. These can be used to sense what is occurring at different points of the converter. Table 2 lists these test points and what they are used for.

Table 2. List of Test Points

NAME	TEST POINT LABEL	DESCRIPTION
TP1	VIN	Input voltage positive sense point
TP2	PGND	Input voltage negative sense point
TP3	SW1	Channel 1 switch node
TP4	COMP	Error amplifier output
TP5	CHB	Loop injection point CHB
TP6	CHA	Loop injection point CHA
TP7	VOUT	Output positive sense point
TP8	PGND	Output negative sense point
TP9	PGOOD	Power good
TP10	SW2	Channel 2 switch node
TP11	AGND	Analog ground
TP12	AGND	Analog ground
TP13	SS	Soft start

5.7 Equipment Shutdown

A. Shut down LOAD
B. Shut down V_{IN1}
C. Shut down V_{IN2}
D. Shut down FAN

6 TPS40131EVM Typical Performance Data and Characteristic Curves

Figure 7 through Figure 9 present typical performance curves for the TPS40131EVM. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

6.1 Efficiency

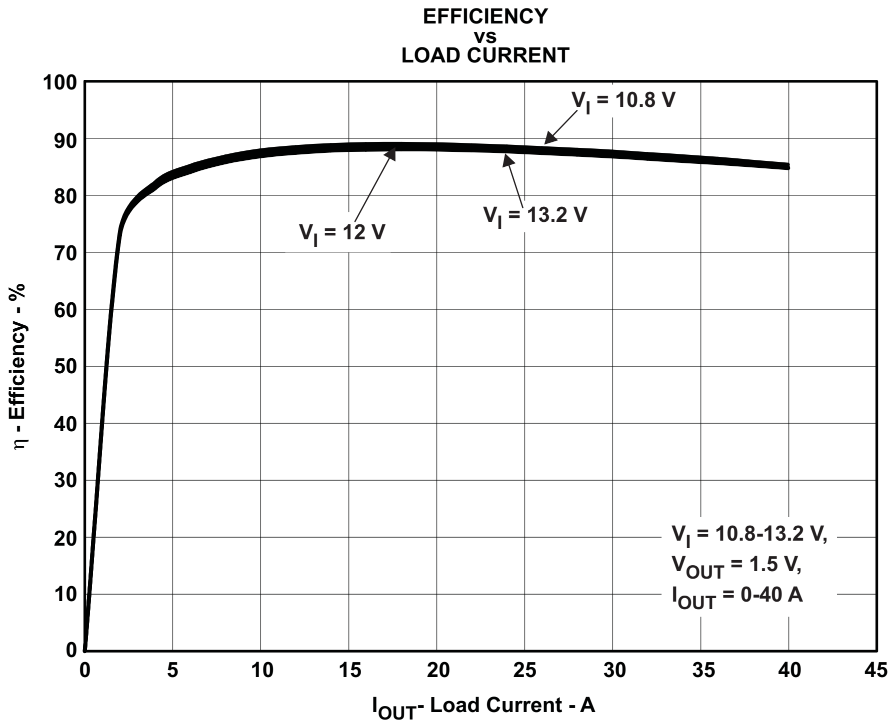

Figure 7. TPS40131EVM Efficiency
V_{IN} = 10.8–13.2V, V_{OUT} = 1.5V, I_{OUT} = 0–40A

6.2 Line and Load Regulation

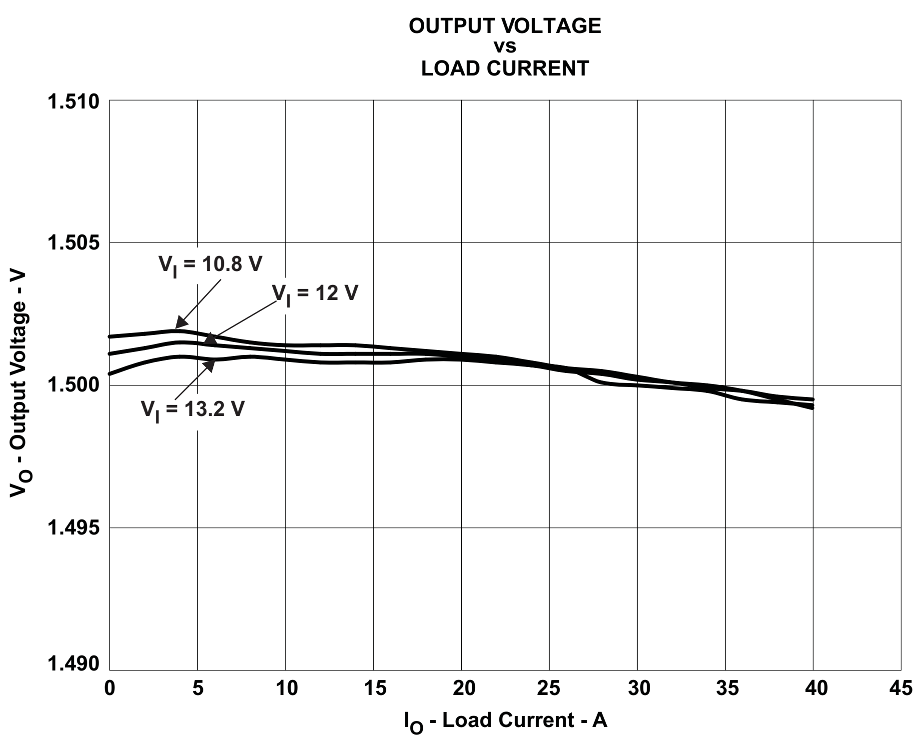

Figure 8. TPS40131EVM V_{OUT} = 1.5V Load Regulation

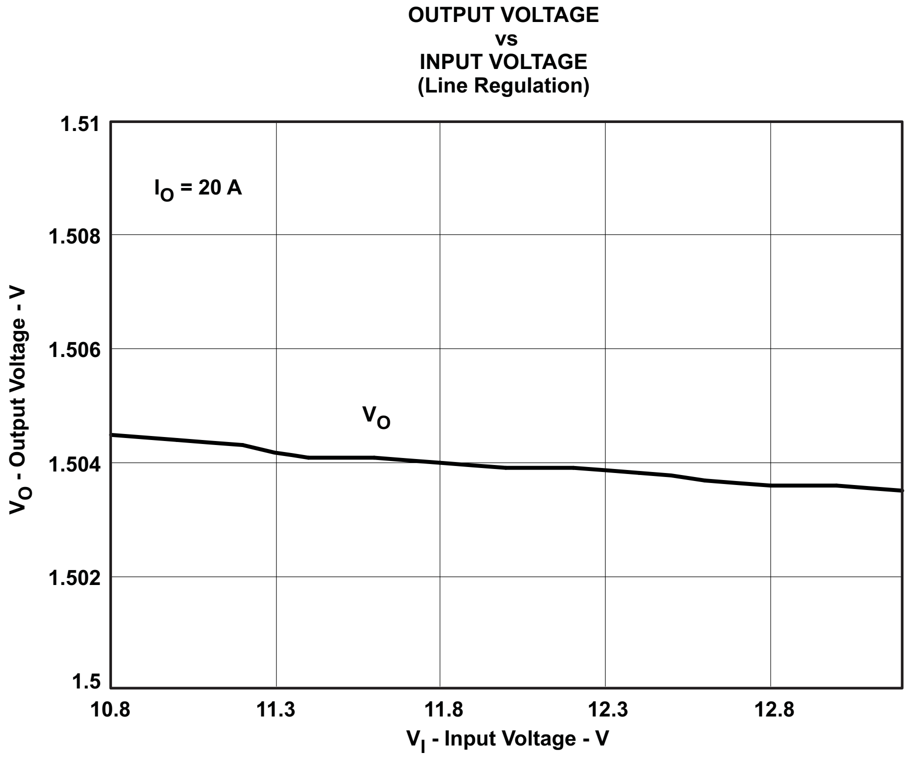

Figure 9. TPS40131EVM V V_{OUT} = 1.5V Line Regulation

6.3 Bode Plot

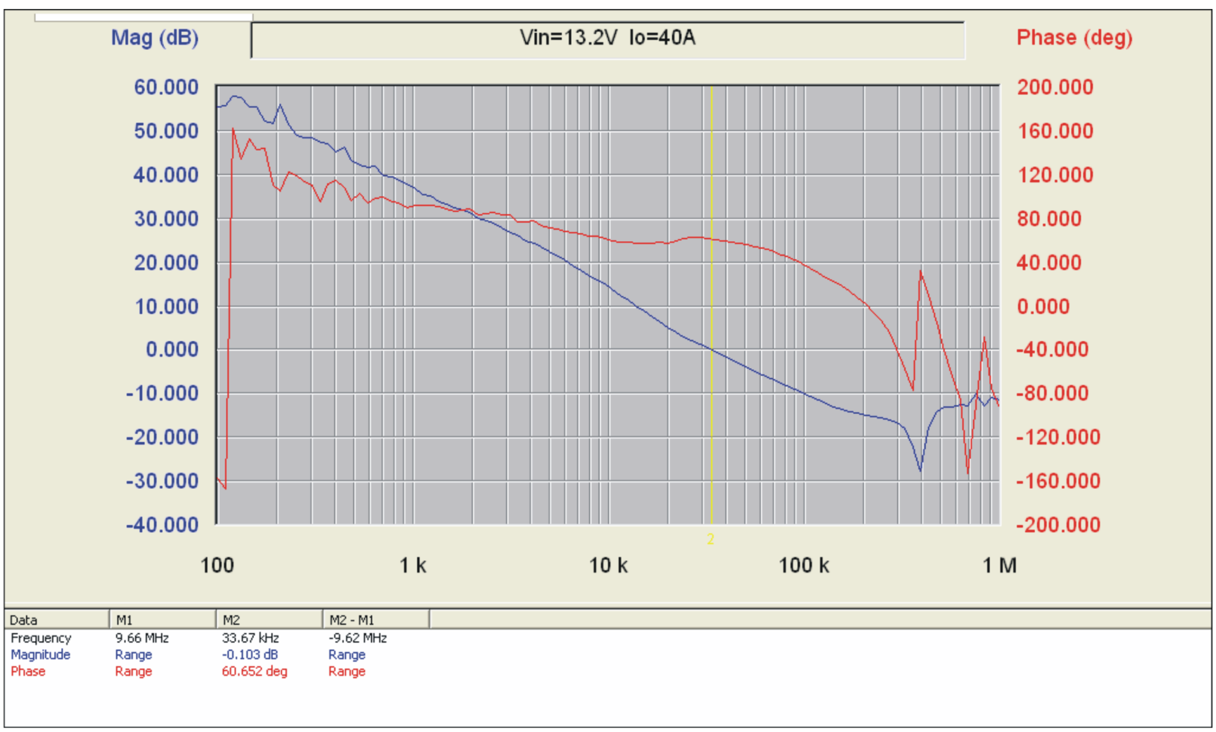

Figure 10. Loop Gain When V_{IN} = 13.2V and I_{OUT} = 40A

6.4 Transient Response

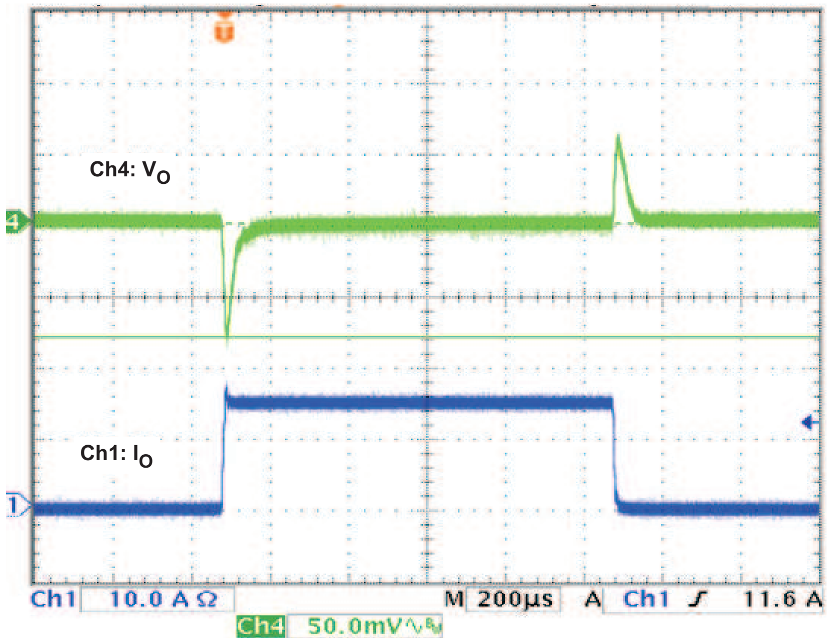

Figure 11. 0–15A load step, Ch1: I_{OUT} ; Ch4: V_{OUT}

7 EVM Assembly Drawings and Layout

The following figures (Figure 12 through Figure 16) show the design of the TPS40131EVM printed circuit board. The EVM has been designed using a four layer, 2-ounce, copper-clad circuit board with all components on the top side, allowing the user to easily view, probe and evaluate the TPS40131 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space-constrained systems.

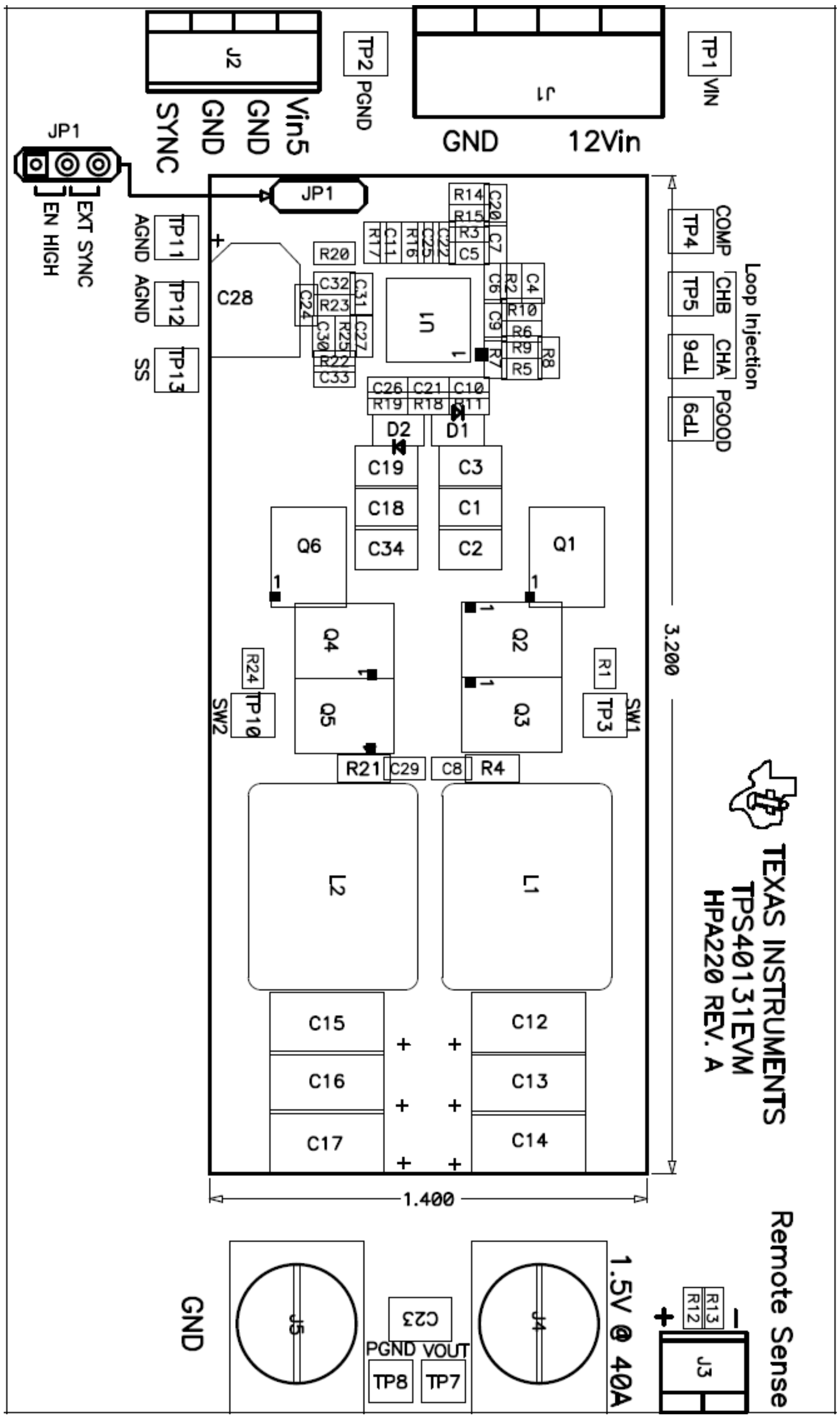

Figure 12. TPS40131EVM Component Placement (Viewed from Top)

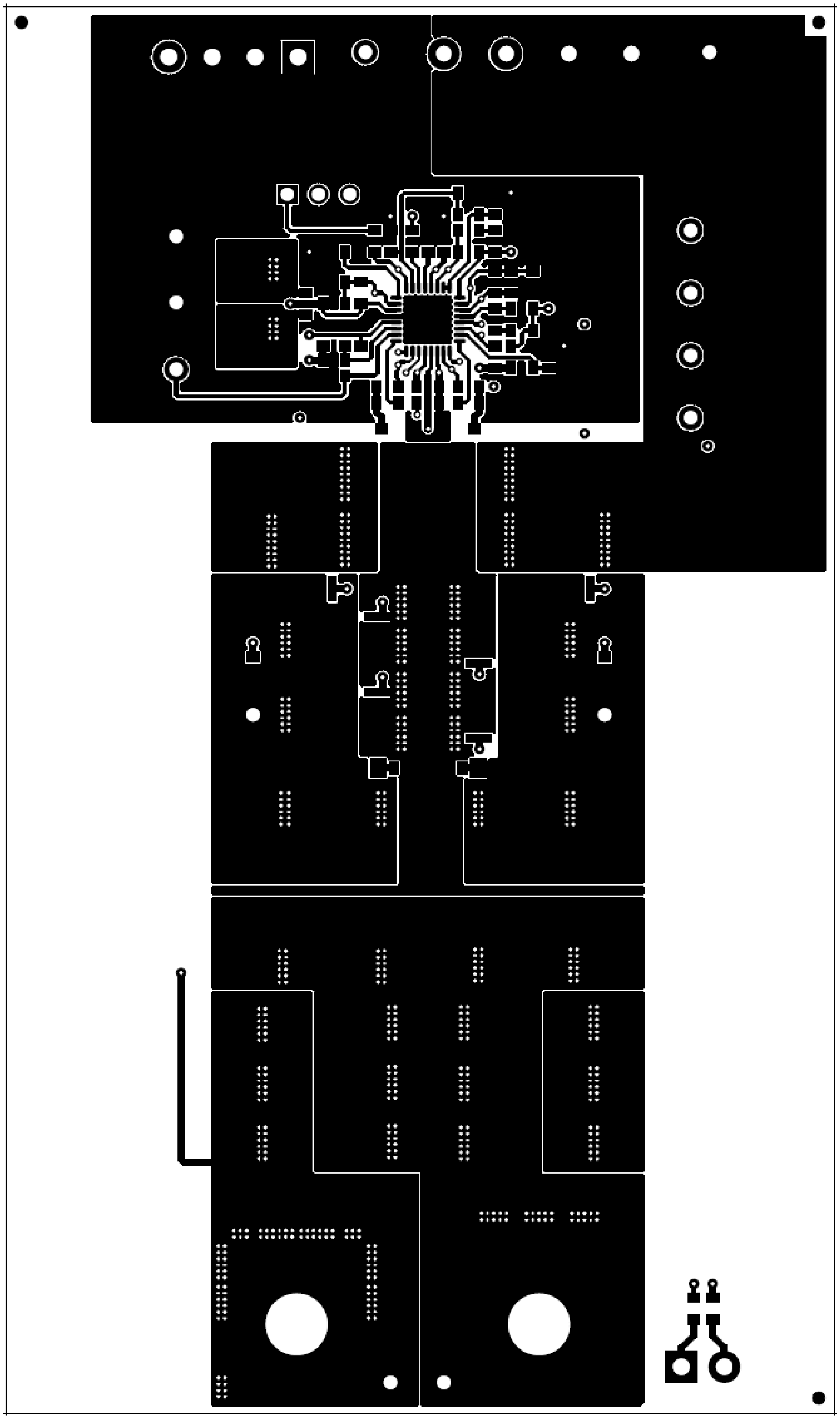

Figure 13. TPS40131EVM Top Copper (Viewed from Top)

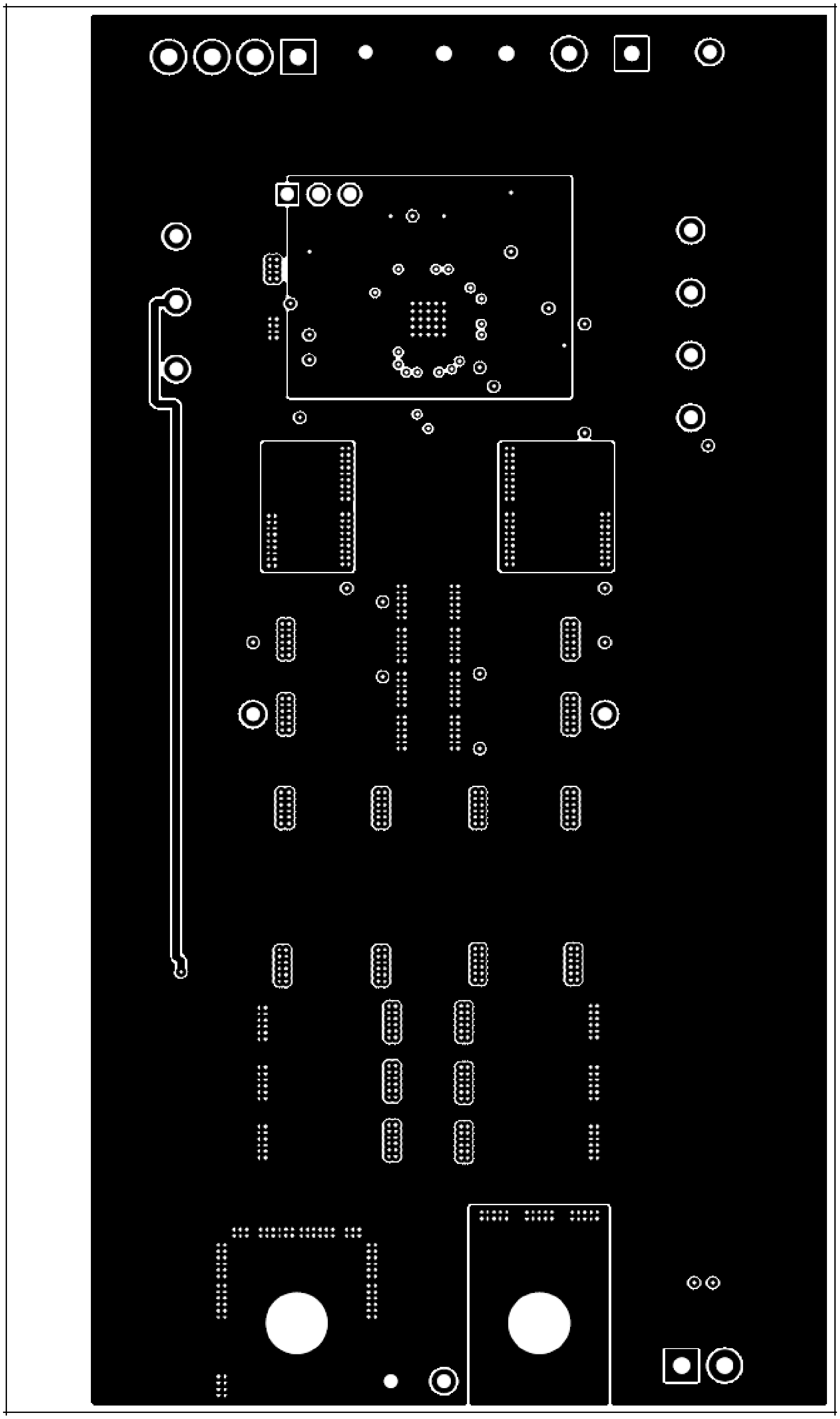

Figure 14. TPS40131EVM Layer 2 Copper (X-Ray View from Top)

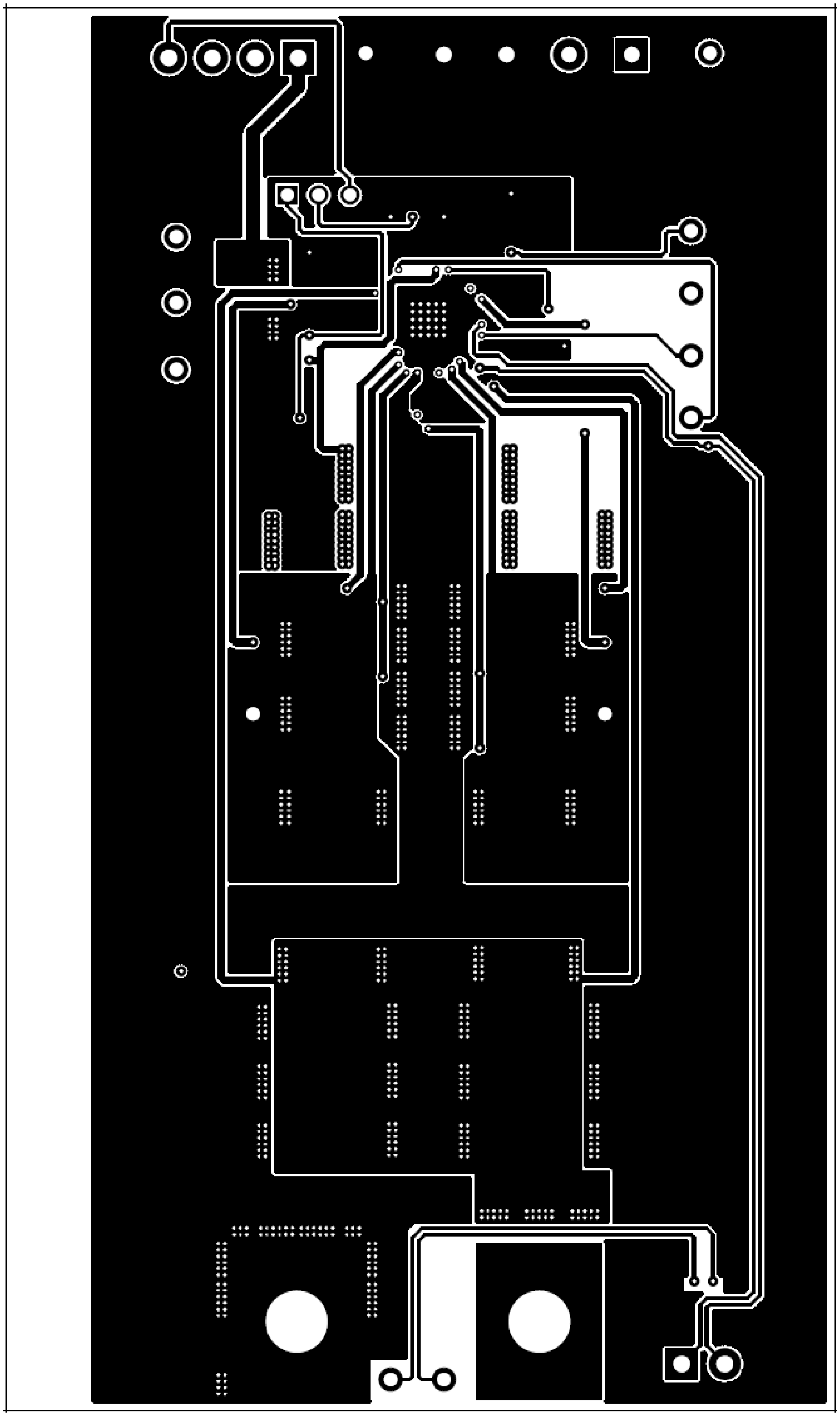

Figure 15. TPS40131EVM Layer 3 Copper (X-Ray View from Top)

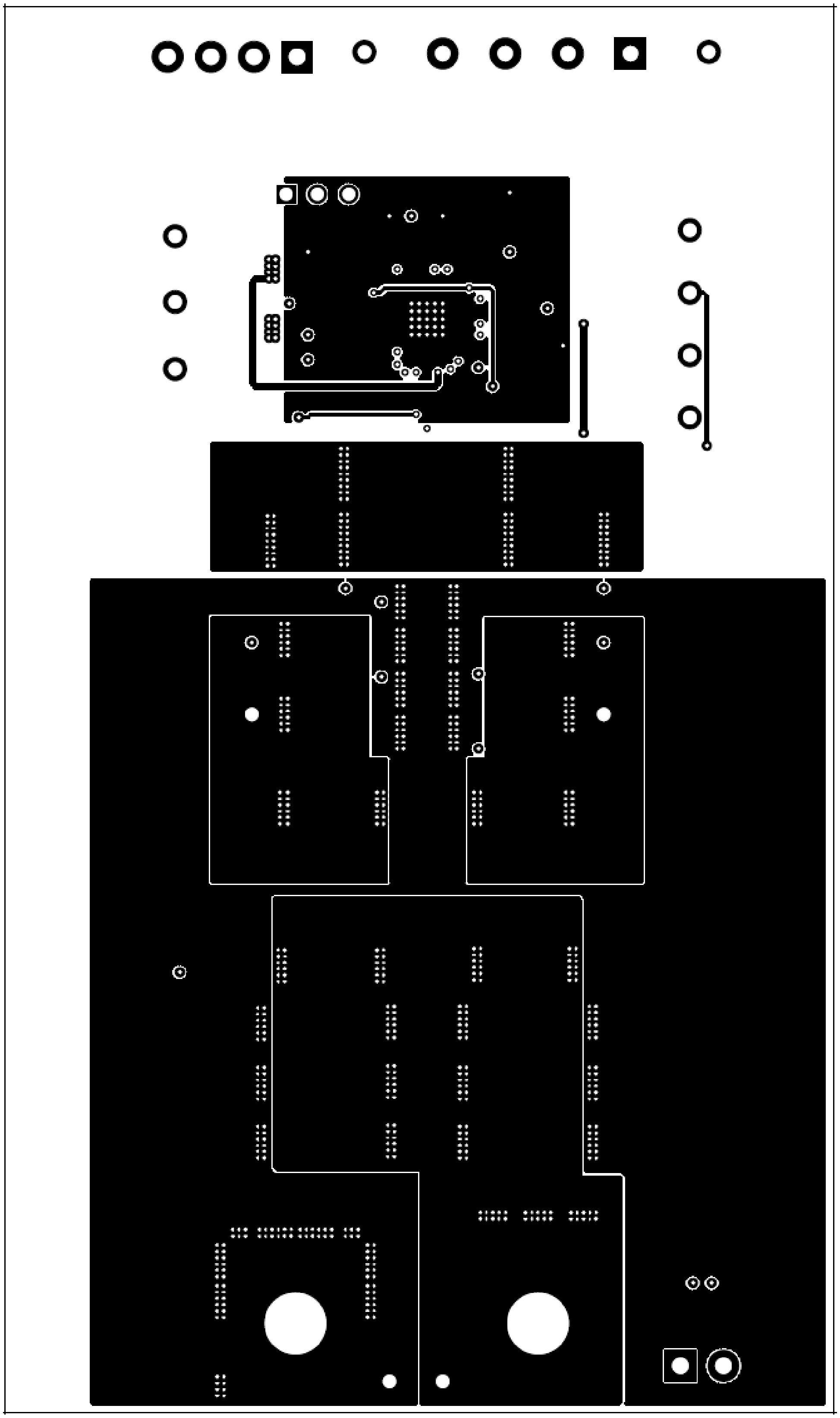

Figure 16. TPS40131EVM Bottom Copper (X-Ray View from Top)

8 List of Materials

Table 3 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 3. TPS40131EVM Bill of Materials

Count	RefDes	Description	Part Number	MFR
6	C1, C2, C3, C18, C19, C34	Capacitor, Ceramic, 22-µF, 16-V, X5R, 20%, 1210	Std	Std
11	C6, C10, C11, C20, C22, C24, C25, C26, C27, C30, C31	Capacitor, Ceramic, 0.1-µF, 16-V, X7R, 10%, 0603	Std	Std
6	C12, C13, C14, C15, C16, C17	Capacitor, Aluminum-SE, 180-µF, 6.3-V, 5-mΩ	EEF-SE0J181R	Pansonic
1	C23	Capacitor, Ceramic, 47-µF, 6.3-V, X5R, 20%	C3225X5R0J476M	TDK
1	C28	Capacitor, Aluminum, 100-µF, 16-V, ±20	EEVFK1C101P	Panasonic
1	C33	Capacitor, Ceramic, 0.022-µF, 16-V, X7R, 10%, 0603	Std	Std
3	C4, C21, C32	Capacitor, Ceramic, 1-µF, 6.3-V, X5R, 10%, 0603	Std	Std
1	C5	Capacitor, Ceramic, 47-pF, 16-V, X7R, 10%, 0603	Std	Std
1	C7	Capacitor, Ceramic, 4.7-nF, 16-V, X7R, 10%, 0603	Std	Std
2	C8, C29	Capacitor, Ceramic, 3.3-nF, 16-V, X7R, 10%, 0603	Std	Std
1	C9	Capacitor, Ceramic, 470-pF, 16-V, X7R, 10%, 0603	Std	Std
2	D1, D2	Diode, Schottky, 30-V, 0.35-Vf, SOD-323	BAT54HT1	On Semi
1	J1	Terminal Block, 4-pin, 15-A, 5,1-mm	ED2227	OST
1	J2	Terminal Block, 4-pin, 6-A, 3,5-mm	ED1516	OST
1	J3	Terminal Block, 2-pin, 6-A, 3,5mm	ED1514	OST
1	JP1	Header, 3-pin, 100-mil spacing, (36-pin strip)	PTC36SAAN	Sullins
2	L1, L2	Inductor, SMT, 0.82-µH	IHLP-5050FD-01	Vishay
2	Q1, Q6	MOSFET, N-Ch, Vds 30V, Rds 4.2 mΩ, Id 40A	HAT2167H	Renesas
4	Q2, Q3, Q4, Q5	MOSFET, N-Ch, Vds 30V, Rds 2.5 mΩ, Id 60A	HAT2164H	Renesas
2	R1, R24	Resistor, Chip, 6.04-kΩ, 1%, 0603	Std	Std
2	R11, R19	Resistor, Chip, 2-Ω, 1%, 0603	Std	Std
2	R12, R13, R18	Resistor, Chip, 10-Ω, 1%, 0603	Std	Std
1	R14	Resistor, Chip, 4.02-kΩ, 1%, 0603	Std	Std
1	R16	Resistor, Chip, 5.1-Ω, 1%, 0603	Std	Std
0	R2, R23	Resistor, Chip, Open, 1%, 0603	Std	Std
1	R20	Resistor, Chip, 75-kΩ, 1%, 0603	Std	Std
1	R25	Resistor, Chip, 2.49-kΩ, 1%, 0603	Std	Std
1	R3	Resistor, Chip, 4.99-kΩ, 1%, 0603	Std	Std
2	R4, R21	Resistor, Chip, 1-Ω, 0805	Std	Std
5	R5, R10, R15, R17, R22	Resistor, Chip, 10-kΩ, 1%, 0603	Std	Std
1	R6	Resistor, Chip, 3-kΩ, 1%, 0603	Std	Std
1	R7	Resistor, Chip, 20-Ω, 1%, 0603	Std	Std
2	R8, R9	Resistor, Chip, 8.66-kΩ, 1%, 0603	Std	Std
1		Jumper, 0.1-inch, 2 contacts	2-382811-1	Tyco/AMP
9	TP1, TP3, TP4, TP5, TP6, TP7, TP9, TP10, TP13	Test Point, Red, Thru-Hole Color Keyed	5000	Keystone
4	TP2, TP8, TP11, TP12	Test Point, Black, Thru-Hole Color Keyed	5001	Keystone
1	U1	IC, 2-phase single output PWM controller, QFN	TPS40131RHB	TI
1	HPA220	PCB, 4.5 inch (114,3 mm) × 2.7 inch (68,6 mm)	HPA220	

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 10.8 V to 13.2 V, and the output voltage range of 1.5 V at 40 A.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 70°C . The EVM is designed to operate properly with certain components above 70°C as long as the input and output ranges are maintained. These components include but are not limited to, switching transistors, inductor, and IC. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
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