

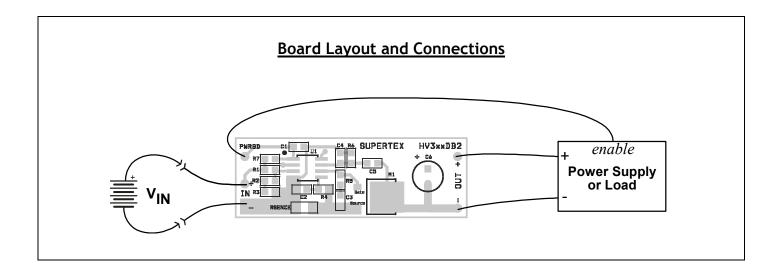
Introduction

The Supertex HV310DB2 demo board contains all necessay circuitry to demonstrate the features of the HV310 hotswap controller. Intended primarily as a negative hotswap controller, the HV310 controls the negative supply path.

Included on board is a 100 μ F capacitor to provide a capacitive load for testing. Additional capacitance (up to 2000 μ F) may be connected to the V_{OUT} terminals, or the 100 μ F may be removed altogether

The board may be modified to meet custom requirements. Instructions are provided on the next page for modifications.

Specifications



V_{IN}

Connect the supply voltage to these terminals. Supply voltage may range from 10 volts to 90 volts.

A high source impedance may cause oscillations when the input voltage is near the undervoltage trip point. A high source impedance results in a large voltage drop when loaded, causing undervoltage lockout to kick in, disconnecting the load. With the load removed, input voltage rises, causing undervoltage to release and reconnecting the load. The cycle repeats, resulting in oscillations. Source impedance must be less than the following to avoid oscillations:

$$R_{SOURCE} < \frac{3V}{I_{LOAD}}$$

V_{OUT}

Connect the power supply or other load to these terminals. $V_{\text{OUT+}}$ is permanently connected to $V_{\text{IN+}}$, it is $V_{\text{OUT-}}$ that is switched.

Application of a DC load during start-up extends the time inrush limiting is active. If this time exceeds about 100ms,

the FET may overheat. For this reason, DC load at start-up should be less than 900mA. Note that DC start-up load limitation decreases with added load capacitance.

Adding external load capacitance increases inrush limit time. Since inrush time is internally limited to 100ms, a maximum of 2000µF may be added

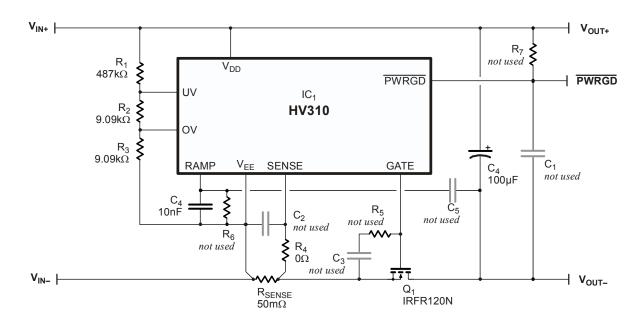
PWRGD

Connect to the power supply's ENABLE input. Depending on the power supply, it may be necessary to level-translate this signal via opto-isolator or discrete circuit. Refer to the HV300/310 data sheet for a description of PWRGD and related application circuits.

PWRGD is an open-drain output. During start-up and whenever V_{IN} is lower than the undervoltage trip point or greater than the overvoltage trip point, PWRGD is high impedance. Once V_{IN} is within the proper range and V_{OUT} has stabilized, PWRGD is pulled down to $V_{\text{IN}-}$.

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Schematic



Inrush Limit

As supplied, the inrush current limit is set at 1 amp. To set inrush limit to another value, change current sense resistor R_{SENSE} according to the formula:

$$R_{SENSE} = \frac{50 \text{mV}}{I_{INRIISH}}$$

The circuit breaker trip point (I_{CB}) is 2 times the inrush limit. For other ratios, refer to the 'Programming Inrush & I_{CB} ' section of the HV301/311 data sheet.

The power rating of R_{SENSE} should be selected based on maximum load current during normal operation.

$$P_{SENSE} = I_{LOAD}^{2} R_{SENSE}$$

Timing

Timing capacitor C_4 determines start-up delay and rise timel. Changing C_4 will alter these timings. Refer to the HV300/310 datasheet for the equations that relate these timings to the value of C_4 . For use in the equations, the nominal gate threshold voltage ($V_{\rm GS}$) of the supplied IRFR120N is 3V and transconductance is about 10 siemens.

Undervoltage/Overvoltage Lockout

Resistors R_1 , R_2 , and R_3 set the undervoltage and overvoltage trip points. New trip points may be programmed by changing the values of these resistors. Refer to the HV300/310 data sheet for more information.

Additional Components

The RC network (R_5C_3) across the gate-source of the external FET provides control loop compensation which prevents inrush current peaking.

A resistor at R_7 can be used to provide a passive pull-up for the PWRGD signal.

A 10nF capacitor at C_1 may be needed for stability to limit dV/dt if PWRGD experiences large voltage swings.

 $R_{\rm 6}$ is only used in the HV301/311 versions of the demo board.

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