# LM25085A

Application Note 1933 LM25085A Evaluation Board



Literature Number: SNVA384A

# LM25085A Evaluation Board

National Semiconductor Application Note 1933 Dennis Morgan February 26, 2009



#### Introduction

The LM25085AEVAL evaluation board provides the design engineer with a fully functional buck regulator, employing the LM25085A PFET switching controller which uses the constant on-time (COT) operating principle. This evaluation board provides a 1V output over an input range of 4.5V to 24V. The circuit delivers load currents to 5A, with current limit set at ≈8.2A. The board is populated with all components except C5 and C7.

The board's specification are:

Input Voltage: 4.5V to 24V

· Output Voltage: 1V

Maximum load current: 5A

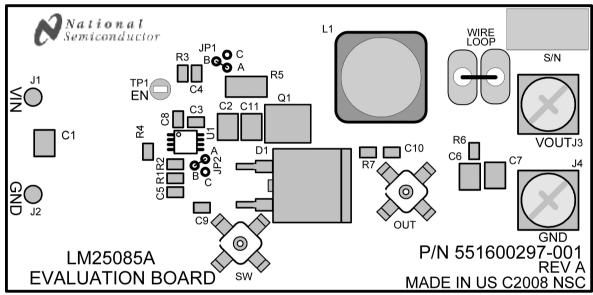
Minimum load current: 0A

Current Limit Threshold: ≊8.2A

 Measured Efficiency: 77.5% (V<sub>IN</sub> = 4.5V, I<sub>OUT</sub> = 1Amp, typical efficiency for converter providing a 1V output)

• Nominal Switching Frequency: 200 kHz

Size: 3.1 in. x 1.5 in.



30088501

FIGURE 1. Evaluation Board - Top Side

# **Theory of Operation**

Refer to the evaluation board schematic in *Figure 6*. When the circuit is in regulation, the on-time at the PGATE output pin is determined by R4 and the voltage at VIN according to the equation:

$$t_{ON} = \frac{1.45 \times 10^{-7} \times (R4 + 1.4)}{V_{IN} - 1.56V + R4/3167} + 50 \text{ ns}$$

where R4 is in kohms. The on-time at the SW node (junction of Q1, L1 and D1) is longer than the above calculated on-time due to the difference of the turn-on and turn-off delay of Q1. The data sheet for the Si7465 PFET indicates a typical turn-on delay of 8 ns, and a typical turn-off delay of 65 ns, resulting in an additional 57 ns at the SW node. The SW on-time of this evaluation board ranges from  $\approxeq1209$  ns at  $V_{IN}=4.5V,$  to  $\approxeq252$  ns at  $V_{IN}=24V.$  The on-time varies inversely with  $V_{IN}$  to maintain a nearly constant switching frequency.

During the off-time, the load current is supplied by the inductor and the output capacitor (C6). When the output voltage falls sufficiently that the voltage at FB is below the reference voltage (0.9V), the regulation comparator initiates a new on-time period. For stable, fixed frequency operation, a minimum of 25 mV of ripple is required at the FB pin to switch the regulation comparator. The required ripple is generated by R7 and C10, and supplied to the FB pin via C9.

The current limit threshold is set by the sense resistor (R5), and R3 at the ADJ pin, and is  $\approxeq$ 8.2A on this board. A current sink at the ADJ pin sets a constant voltage across R3. When the voltage across R5 exceeds the voltage across R3 the current limit comparator switches to shut off Q1, and the LM25085A forces a longer-than-normal off-time. The long off-time is a function of the input voltage ( $V_{IN}$ ) and the voltage at the FB pin, and is necessary to allow the inductor current to decrease at least as much, if not more, than the current increase which occurred during the on-time.

The circuit may be shutdown at any time by grounding the Enable test point (EN, TP1). Removing the ground connection allows normal operation to resume.

Refer to the LM25085A data sheet for a detailed block diagram, and a complete description of the various functional blocks.

## **Board Layout and Probing**

The pictorial in *Figure 1* shows the placement of the circuit components. The following should be kept in mind when the board is powered:

- 1) When operating at high load current forced air flow may be necessary to prevent overheating of Q1, D1, and L1. These components may be hot to the touch.
- Use CAUTION when probing the circuit at high input voltages to prevent injury, as well as possible damage to the circuit.
- 3) At maximum load current (5A), the wire size and length used to connect the source voltage, and the load, becomes important. Ensure there is not a significant drop in the wires supplying the input current and the load current.

## **Board Connection/Start-up**

The input connections are made to the J1 (+) and J2 (-) connectors. The load is connected to the J3 (VOUT) and J4 (GND) terminals. Ensure the wires are adequately sized for the intended load current. Before start-up a voltmeter should be connected to the input terminals, and one to the output terminals. The load current should be monitored with an ammeter or a current probe. It is recommended that the input voltage be increased gradually to 4.5V, at which time the output voltage should be 1V. If the output voltage is correct, then increase the input voltage as desired and proceed with evaluating the circuit. DO NOT EXCEED 35V AT VIN.

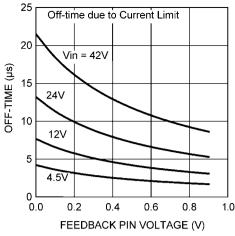
#### **Current Limit**

The LM25085A peak current limit detection operates by sensing the voltage across either the  $R_{\rm DS(ON)}$  of Q1, or a sense resistor (R5), during the on-time and comparing it to the voltage across R3 at the ADJ pin. The current limit threshold is reached when the sensed voltage exceeds the voltage across R3. When current limit is reached Q1 is immediately switched off. The current limit function is much more accurate and stable over temperature when a sense resistor is used. The  $R_{\rm DS}$   $_{\rm (ON)}$  of a MOSFET has a wide process variation and a large temperature coefficient.

Current sensing is disabled for a blanking time of  $\approxeq 100$  ns at the beginning of each on-time to prevent false triggering of the current limit comparator due to leading edge current spikes. After Q1 is turned off due to current limit detection, Q1 is held off for a longer-than-normal off-time. The extended off-time is a function of the input voltage and the voltage at the FB pin, as shown below in the graph "Current Limit Off-time vs.  $V_{IN}$  and  $V_{FB}$ ". The current limit off-time can be calculated from the following:

$$t_{OFF(CL)} = \frac{8 \times 10^{-6} \times ((V_{IN}/31) + 0.15)}{(V_{FB} \times 0.93) + 0.56V}$$

The longer-than-normal forced off-time allows the inductor current to decrease to a low level before the next on-time. This cycle-by-cycle monitoring, followed by a long forced off-time, provides effective protection from output load faults over a wide range of operating conditions.



20000505

FIGURE 2. Current Limit Off-time vs.  $V_{IN}$  and  $V_{EB}$ 

A) Sense resistor method – This evaluation board is supplied configured for the sense resistor method of current limit detection. Jumpers A-B are in place at both jumper locations (JP1, JP2), which connects the ADJ pin resistor (R3) and the ISEN pin across the sense resistor (R5). If the voltage across R5 exceeds the voltage across R3 during the on-time, the current limit comparator switches to turn off Q1. The voltage across R3 is set by an internal 40  $\mu$ A current sink at the ADJ pin. The current at which the current limit comparator switches is calculated from:

$$I_{CL} = 40 \,\mu\text{A} \, x \, \text{R}3/\text{R}5$$
 (1)

With R5 = 10 m $\Omega$  and R3 = 2.05 k $\Omega$ , the nominal current limit threshold calculates to 8.2A. Since that is the peak of the inductor current waveform, the load current is equal to that peak value minus one half the ripple current amplitude. At Vin = 4.5V, the ripple amplitude is  $\approx$ 622 mAp-p, and the load current at current limit is equal to 7.89A. At Vin = 24V, the ripple amplitude is  $\approx$ 851 mAp-p, and the load current at current limit is equal to  $\approx$ 7.77A.

Using the tolerances for the ADJ pin current and the current limit comparator offset, the maximum current limit threshold calculates to:

$$I_{CL(max)} = \frac{(2.05 \text{ k}\Omega \text{ x } 48 \text{ }\mu\text{A}) + 9 \text{ mV}}{0.01\Omega} = 10.74\text{A}$$

and the load current at current limit calculates to 10.43A at 4.5V, and 10.32A at 24V. The minimum current limit thresholds calculate to:

$$I_{CL(min)} = \frac{(2.05 \text{ k}\Omega \text{ x } 32 \text{ }\mu\text{A}) - 9 \text{ mV}}{0.01\Omega} = 5.66\text{A}$$

and the load current at current limit calculates to 5.35A at 4.5V, and 5.24A at 24V.

To change the current limit threshold the value for R5 should be chosen to achieve 50 mV to 100 mV across it at current limit, staying within the practical limitations of power dissipation and physical size of the resistor. A larger value for R5 reduces the effects of the current limit comparator offset, but at the expense of higher power dissipation. After selecting the value for R5, calculate the value for R3 by rearranging Equa-

tion 1 above. See the Applications Information section of the LM25085A data sheet for a procedure to account for ripple current amplitude and tolerances when selecting the resistor for the ADJ pin.

**B) Q1 R**<sub>DS(ON)</sub> **method** – To configure the evaluation board to use the R<sub>DS(ON)</sub> of Q1 for current limit detection, move the jumpers at both JP1 and JP2 from the A-B position to the B-C position. This change connects the ADJ pin resistor (R3) and the ISEN pin across Q1. Since the sense resistance is now the R<sub>DS(ON)</sub> of Q1, R3 must be changed. The data sheet for the Si7465 PFET lists the typical R<sub>DS(ON)</sub> as 51 mΩ at V<sub>GS</sub> = 10V, and 64 mΩ at V<sub>GS</sub> = 4.5V. Therefore, the R<sub>DS (ON)</sub> is estimated to be nominally 57 mΩ at V<sub>GS</sub> = 7.7V. To achieve the same nominal current limit threshold as above (8.2A), using Equation 6 in the data sheet R3 calculates to:

R3 = 
$$\frac{8.2 \text{A} \times 0.057 \Omega}{40 \text{ } \mu\text{A}}$$
 = 11.7 k $\Omega$ 

The load current is equal to the current limit threshold minus half the current ripple amplitude. R3 can be changed to set other current limit detection thresholds.

## **Output Ripple Control**

The LM25085A requires a minimum of 25 mVp-p ripple at the FB pin, in phase with the switching waveform at the SW node, for proper operation. On this evaluation board, the required ripple is generated by R7, C9, and C10, allowing the ripple at  $V_{\rm OUT}$  to be kept to a minimum, as described in option A below. Alternatively, the required ripple at the FB pin can be supplied from ripple generated at  $V_{\rm OUT}$  and passed through the feedback resistors, as described in options B and C below, using one or two less external components.

**A) Minimum Output Ripple:** This evaluation board is supplied configured for minimum ripple at  $V_{OUT}$  by using components R7, C9 and C10. The ripple voltage required by the FB pin is generated by R7 and C10 since the SW node switches

from  $\cong$ -1V to V<sub>IN</sub>, and the right end of C10 is a virtual ground. The values for R7 and C10 are chosen to generate a 25-40 mVp-p triangle waveform at their junction. That triangle wave is then coupled to the FB pin through C9. The following procedure is used to calculate values for R7, C9 and C10:

1) Calculate the voltage V<sub>a</sub>:

$$V_A = V_{OUT} - (V_{SW} x (1 - (V_{OUT}/V_{IN(min)})))$$

where  $V_{SW}$  is the absolute value of the voltage at the SW node during the off-time, typically 0.5V to 1V depending on the diode, and  $V_{IN}$  is the minimum input voltage. Using a typical value of 0.65V for  $V_{SW}$ ,  $V_A$  calculates to 0.49V. This is the approximate DC voltage at the R7/C10 junction, and is used in the next equation.

2) Calculate the R7xC10 product:

$$R7 \times C10 = \frac{(V_{IN} - V_A) \times t_{ON}}{\Lambda V}$$

where  $t_{ON}$  is the maximum on-time ( $\cong$ 1209 ns),  $V_{IN}$  is the minimum input voltage, and  $\Delta V$  is the desired ripple amplitude at the R7/C10 junction, 30 mVp-p for this example.

R7 x C10 = 
$$\frac{(4.5V - 0.49V) \times 1209 \text{ ns}}{0.03V}$$
 = 16.2 x 10<sup>-5</sup>

R7 and C10 are then chosen from standard value components to satisfy the above product. On this evaluation board, C10 is set at 3300 pF. R7 calculate to be 49 k $\Omega$ , and a standard value 48.7 k $\Omega$  resistor is used. C9 is chosen to be 0.01  $\mu$ F, large compared to C10. The circuit as supplied on this EVB is shown in *Figure 3*.

The output ripple, which ranges from  $\cong$ 20 mVp-p at V<sub>IN</sub> = 4.5V to  $\cong$ 33 mVp-p at V<sub>IN</sub> = 24V, is determined primarily by the ESR of the output capacitance (C6), and the inductor's ripple current. See *Figure 10*.

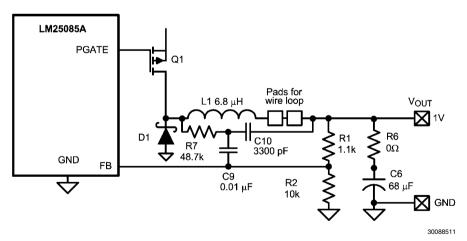


FIGURE 3. Minimum Ripple Using R7, C9, C10

B) Reduced Ripple Level Configuration: This configuration generates more ripple at V<sub>OUT</sub> than the above configuration, but uses one less capacitor. If some ripple is acceptable in the application, this configuration is slightly more economical, and simpler. R6 and C5 are used instead of R7, C9 and C10, as shown in *Figure 4*.

Ripple is generated at  $V_{OUT}$  as the inductor's ripple current flows through R6, and that ripple voltage is passed to the FB pin via C5. The ripple at  $V_{OUT}$  can be set as low as 25 mVpp since it is not attenuated by R1 and R2. The minimum value for R6 is calculated from:

$$R6 = \frac{25 \text{ mV}}{I_{OR(min)}}$$

where  $I_{OR(min)}$  is the minimum inductor's ripple current, which occurs at minimum input voltage, and is 622 mAp-p at 4.5V. The minimum value for R6 calculates to 0.04 ohms. Using a standard value 43 m $\Omega$  resistor for R6, the ripple at  $V_{OUT}$  ranges from 27 mVp-p to 37 mVp-p over the input voltage range. See *Figure 10*.

The minimum value for C5 is determined from:

$$C5 = \frac{3 \times t_{ON(max)}}{R1//R2}$$

Where  $t_{ON(max)}$  is the maximum on-time, 1209 ns in this evaluation board. The minimum value for C5 calculates to 3660 pF.

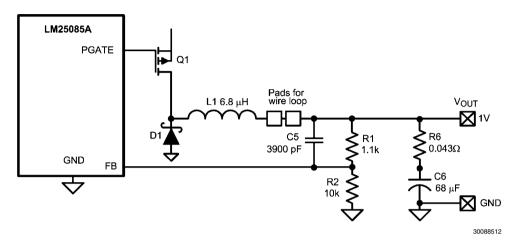
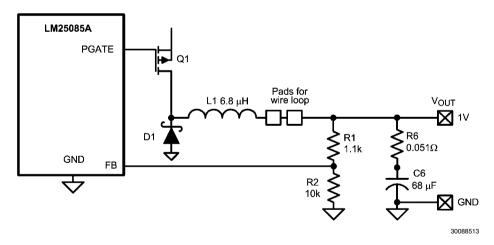


FIGURE 4. Reduced Ripple Configuration

**C)** Lowest Cost Configuration: This configuration is the same as option B above, but with C5 removed. The ripple at the FB pin is attenuated from that at  $V_{OUT}$  by the feedback resistors (R1, R2). Since  $\geq$ 25 mVp-p are required at the FB pin, R6 is chosen to generate  $\geq$ 28 mV at  $V_{OUT}$ . Since the minimum ripple current in this circuit is 622 mAp-p the minimum

mum value for R6 calculates to 45 m $\Omega$ . Using a standard value 51 m $\Omega$  resistor for R6, the ripple at V<sub>OUT</sub> ranges from  $\cong$ 32 mVp-p to  $\cong$ 43 mVp-p over the input voltage range. See *Figure 10*. If the application can accept this ripple level, this is the most economical solution. The circuit is shown in *Figure 5*.



**FIGURE 5. Lowest Cost Configuration** 

### **Monitor The Inductor Current**

The inductor's current can be monitored or viewed on a scope with a current probe. Remove the jumper from the WIRE LOOP pads, and install an appropriate current loop across the pads. In this way the inductor's ripple current and peak current can be accurately determined.

# **Scope Probe Adapters**

Scope probe adapters are provided on this evaluation board for monitoring the waveform at the SW node, and at the circuit's output ( $V_{\text{OUT}}$ ), without using the probe's ground lead which can pick up noise from the switching waveforms. The probe adapters are suitable for Tektronix P6137 or similar probes, with a 0.135" diameter.

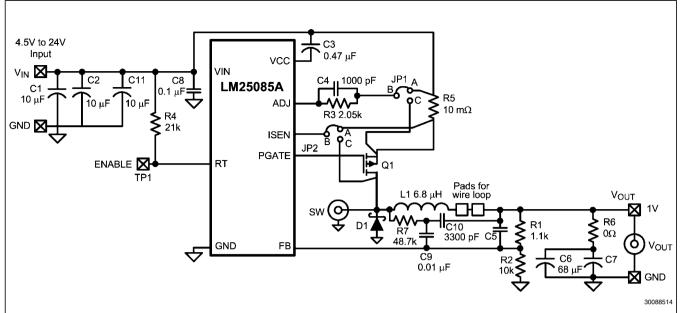


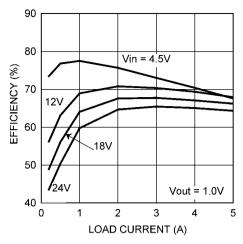
FIGURE 6. Complete Evaluation Board Schematic

5

# **Bill of Materials**

Item	Description	Mfg., Part Number	Package	Value
C1, C2, C11	Ceramic Capacitor	Taiyo Yuden GMK325BJ106KN	1210	10 μF, 35V
C3	Ceramic Capacitor	TDK C2012X7R1C474K	0805	0.47 μF, 16V
C4	Ceramic Capacitor	TDK C2012X7R2A102K	0805	1000 pF, 100V
C5		Unpopulated	0805	
C6	Ceramic Capacitor	TDK C3225X5R0J686M	1210	68 μF, 6.3V
C7		Unpopulated		
C8	Ceramic Capacitor	TDK C2012X7R2A104K	0805	0.1 μF, 100V
C9	Ceramic Capacitor	TDK C2012X7R2A103K	0805	0.01 μF, 100V
C10	Ceramic Capacitor	TKD C2012X7R2A332K	0805	3300 pF, 100V
D1	Schottky Diode	On Semi MBRB2535CTL	D2PAK	35V, 25A
L1	Power Inductor	Wurth XXL 7447709006	12 mm x 12 mm	6.8 µH
Q1	P-Channel MOSFET	Vishay Si7465DP	SO-8 Power	60V, 5A
R1	Resistor	Vishay CRCW08051101F	0805	1.1k
R2	Resistor	Vishay CRCW08051002F	0805	10k
R3	Resistor	Vishay CRCW08052051F	0805	2.05k
R4	Resistor	Vishay CRCW08052102F	0805	21k
R5	Resistor	Vishay WSL2010R0100F	2010	0.01 ohm,
R6	Resistor	Vishay CRCW08050000Z	0805 0 ohms	
R7	Resistor	Vishay CRCW08054872F	0805	48.7k
U1	Switching Regulator	National Semiconductor LM25085AMY	MSOP8-EP	

# **Circuit Performance**



30088515

(Efficiencies in this range are typical for a buck converter producing a 1.0V output)

FIGURE 7. Efficiency vs Load Current

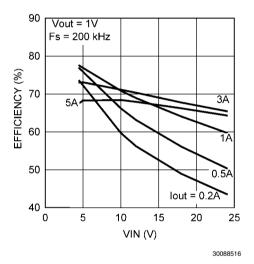


FIGURE 8. Efficiency vs Input Voltage

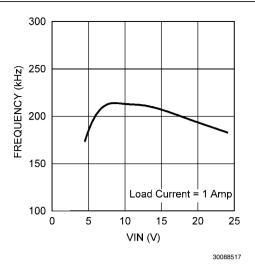


FIGURE 9. Switching Frequency vs. Input Voltage

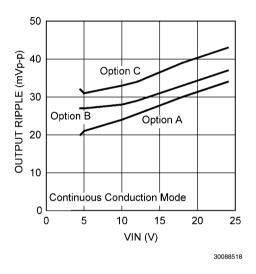


FIGURE 10. Output Voltage Ripple

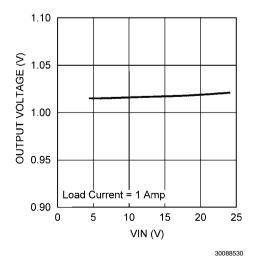


FIGURE 11. Line Regulation

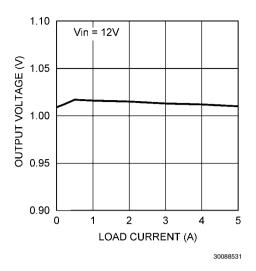
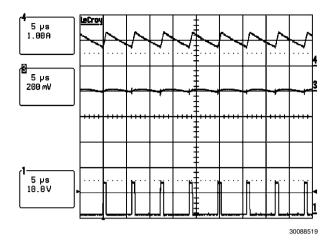


FIGURE 12. Load Regulation

# **Typical Waveforms**



Trace 4 = Inductor Current

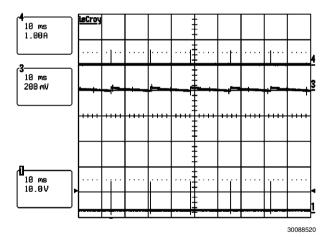
Trace 3 = V<sub>OUT</sub>

Trace 1 = SW Node

 $V_{IN} = 12V$ ,  $I_{OUT} = 1Amp$ 

Minimum Ripple Configuration (Option A)

**FIGURE 13. Continuous Conduction Mode** 

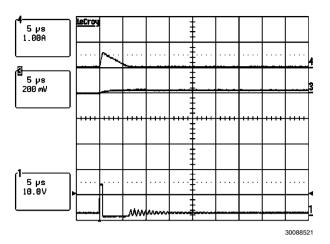


Trace 4 = Inductor Current

Trace 3 = V<sub>OUT</sub>
Trace 1 = SW Node

 $V_{IN}=12V,\ I_{OUT}=0$ 

**FIGURE 14. Discontinuous Conduction Mode** 

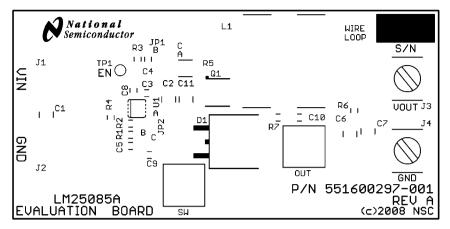


Trace 4 = Inductor Current
Trace 3 = V<sub>OUT</sub>

Trace 1 = SW Node  $V_{IN} = 12V$ ,  $I_{OUT} = 0$ 

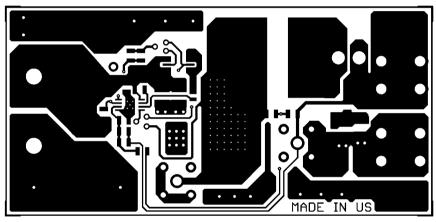
FIGURE 15. Discontinuous Conduction Mode (Expanded Scale)

# **PC Board Layout**



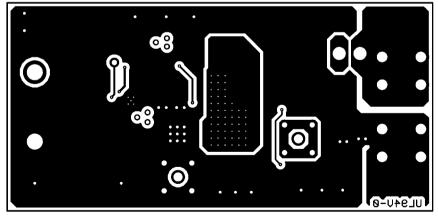
**Board Silkscreen** 

30088522



**Board Top Layer** 

30088523



**Board Bottom Layer (Viewed from Top)** 

30088524

13 www.national.com

AN-1933

## **Notes**

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Pr	oducts	Design Support		
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench	
Audio	www.national.com/audio	App Notes	www.national.com/appnotes	
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns	
Data Converters	www.national.com/adc	Samples	www.national.com/samples	
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards	
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging	
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green	
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts	
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality	
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback	
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy	
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions	
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero	
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic	
Wireless (PLL/VCO)	www.national.com/wireless	Analog University®	www.national.com/AU	

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

#### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2009 National Semiconductor Corporation

For the most current product information visit us at www.national.com



National Semiconductor Americas Technical Support Center Email: support@nsc.com Tel: 1-800-272-9959 National Semiconductor Europe Technical Support Center Email: europe.support@nsc.com National Semiconductor Asia Pacific Technical Support Center Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center Email: jpn.feedback@nsc.com

#### IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

#### Products Applications

Audio www.ti.com/audio Communications and Telecom www.ti.com/communications **Amplifiers** amplifier.ti.com Computers and Peripherals www.ti.com/computers dataconverter.ti.com Consumer Electronics www.ti.com/consumer-apps **Data Converters DLP® Products** www.dlp.com **Energy and Lighting** www.ti.com/energy DSP dsp.ti.com Industrial www.ti.com/industrial Clocks and Timers www.ti.com/clocks Medical www.ti.com/medical Interface interface.ti.com Security www.ti.com/security

Logic Space, Avionics and Defense <u>www.ti.com/space-avionics-defense</u>

Power Mgmt power.ti.com Transportation and Automotive www.ti.com/automotive
Microcontrollers microcontroller.ti.com Video and Imaging www.ti.com/video

RFID <u>www.ti-rfid.com</u>
OMAP Mobile Processors www.ti.com/omap

Wireless Connectivity <u>www.ti.com/wirelessconnectivity</u>

TI E2E Community Home Page <u>e2e.ti.com</u>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated