

TPS54821EVM-049, 8-A, SWIFT™ Regulator Evaluation Module

This user's guide contains information for the TPS54821EVM-049 evaluation module (PWR049) as well as for the TPS54821 dc/dc converter. Also included are the performance specifications, the schematic, and the bill of materials for the TPS54821EVM-049.

Contents

1	Introduction	2
2	Test Setup and Results	
3	Board Layout	
4	Schematic and Bill of Materials	14
	List of Figures	
1	TPS54821EVM-049 Efficiency	5
2	TPS54821EVM-049 Low Current Efficiency	5
3	TPS54821EVM-049 Load Regulation	6
4	TPS54821EVM-049 Line Regulation	6
5	TPS54821EVM-049 Transient Response	7
6	TPS54821EVM-049 Loop Response	7
7	TPS54821EVM-049 Output Ripple	8
8	TPS54821EVM-049 Input Ripple	8
9	TPS54821EVM-049 Start-Up Relative to V _{IN}	9
10	TPS54821EVM-049 Start-Up Relative to Enable	9
11	TPS54821EVM-049 Start-Up Into Pre-Bias	10
12	TPS54821EVM-049 Hiccup-Mode Current Limit	10
13	TPS54821EVM-049 Top-Side Assembly	11
14	TPS54821EVM-049 Top-Side Layout	12
15	TPS54821EVM-049 Internal Layer-1 Layout	12
16	TPS54821EVM-049 Internal Layer-2 Layout	13
17	TPS54821EVM-049 Bottom-Side Layout	13
18	TPS54821EVM-049 Schematic	14
	List of Tables	
1	Input Voltage and Output Current Summary	2
2	TPS54821EVM-049 Performance Specification Summary	2
3	Output Voltages Available	3
4	EVM Connectors and Test Points	4
5	TPS54821EVM-049 Bill of Materials	15

SWIFT is a trademark of Texas Instruments.



Introduction www.ti.com

1 Introduction

1.1 Background

The TPS54821 dc/dc converter is designed to provide up to a 8-A output. The TPS54821 implements split-input power rails with separate input voltage inputs for the power stage and control circuitry. The power stage input (PVIN) is rated for 1.6 V to 17 V whereas the control input (VIN) is rated for 4.5 V to 17 V. The TPS54821EVM-049 provides both inputs but is designed and tested using the PVIN connected to VIN. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54821 regulator. The switching frequency is externally set at a nominal 480 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54821 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS54821 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54821 provides adjustable slow start, tracking, and undervoltage lockout inputs. The absolute maximum input voltage is 20 V for the TPS54821EVM-049.

Table 1. Input Voltage and Output Current Summary

EVM	EVM INPUT VOLTAGE RANGE	
TPS54821EVM-049	VIN = 8 V to 17 V (VIN start voltage = 6.528 V)	0 A to 8 A

1.2 Performance Specification Summary

A summary of the TPS54821EVM-049 performance specifications is provided in Table 2. Specifications are given for an input voltage of $V_{\rm IN} = 12$ V and an output voltage of 3.3 V, unless otherwise specified. The TPS54821EVM-049 is designed and tested for $V_{\rm IN} = 8$ V to 17 V with the VIN and PVIN pins connect together with the JP1 jumper. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS54821EVM-049 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{IN} voltage range (PVIN = VIN)			8	12	17	V
V _{IN} start voltage				6.528		V
V _{IN} stop voltage				6.193		V
Output voltage setpoint				3.3		V
Output current range	V _{IN} = 8 V to 17 V		0		8	Α
Line regulation	I _O = 4 A, V _{IN} = 8 V to 17 V			±0.005		%
Load regulation	V _{IN} = 12 V, I _O = 0 A to 8 A			±0.07		%
	I _O = 2 A to 6 A	Voltage change		-130		mV
Lond formation to a constant		Recovery time		80		μs
Load transient response	I _O = 6 A to 2 A	Voltage change		130		mV
		Recovery time		80		μs
Loop bandwidth	$V_{IN} = 12 \text{ V}, I_{O} = 8 \text{ A}$	$I_O = 6$ A to 2 A Recovery time $V_{IN} = 12 \text{ V}, I_O = 8 \text{ A}$		60		kHz
Phase margin	$V_{IN} = 12 \text{ V}$, $I_{O} = 8 \text{ A}$	A		74		0
Input ripple voltage	I _O = 8 A			900		mVPP
Output ripple voltage	I _O = 8 A			10		mVPP
Output rise time				6		ms
Operating frequency				480		kHz
Maximum efficiency	TPS54821EVM-049, V _{IN} = 8 V, I _O = 1.5 A			95.9		%



www.ti.com Introduction

1.3 **Modifications**

These evaluation modules are designed to provide access to the features of the TPS54821. Some modifications can be made to this module.

1.3.1 **Output Voltage Setpoint**

The output voltage is set by the resistor divider network of R7 and R8. R7 is fixed at 10 k Ω . To change the output voltage of the EVM, it is necessary to change the value of resistor R8. Changing the value of R8 can change the output voltage above 0.6 V. The value of R8 for a specific output voltage can be calculated using Equation 1.

$$R8 = \frac{10 \ k\Omega \times 0.6 \ V}{V_{OUT} - 0.6 V}$$
 (1)

Table 3 lists the R8 values for some common output voltages. Note that V_{IN} must be in a range so that the on-time is greater than the minimum controllable on-time (94 ns typical, 145 ns maximum), and the maximum duty cycle is less than 95%. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

Output Voltage (V)	R8 Value (kΩ)
1.8	4.99
2.5	3.16
3.3	2.21
5	1.37

Table 3. Output Voltages Available

1.3.2 Slow-Start Time

The slow-start time can be adjusted by changing the value of C8. Use Equation 2 to calculate the required value of C8 for a desired slow-start time

$$C8(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref(V)}$$
(2)

The EVM is set for a slow-start time of 5.7 ms using C8 = $0.022 \mu F$.

1.3.3 Track In

The TPS54821 can track an external voltage during start-up. The J3 connector is provided to allow connection to that external voltage. Ratiometric or simultaneous tracking can be implemented using resistor divider R5 and R6. See the TPS54821 data sheet (SLVSA70) for details.

1.3.4 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R1 and R2. The EVM is set for a start voltage of 6.528 V and a stop voltage of 6.193 V using R1 = 35.7 k Ω and R2 = 8.06 k Ω . Use Equation 3 and Equation 4 to calculate required resistor values for different start and stop voltages.

$$R1 = \frac{V_{START} \left(\frac{V_{ENFALLING}}{V_{ENRISING}} \right) - V_{STOP}}{I_{p} \left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}} \right) + I_{h}}$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1 (I_{p} + I_{h})}$$
(3)

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)}$$
(4)



1.3.5 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. During normal operation, the PVIN and VIN inputs are connected using a jumper across JP1. The single input voltage is supplied at J1. If desired, these two input voltage rails may be separated by removing the jumper across JP1. Two input voltages must then be provided at both J1 and J2.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54821EVM-049 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input/Output Connections

The TPS54821EVM-049 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 4 A must be connected to J1 through a pair of 20 AWG wires. The jumper across JP1 must be in place. See Section 1.3.5 for split-input voltage rail operation. The load must be connected to J4 through a pair of 20 AWG wires. The maximum load current capability must be 8 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP9 is used to monitor the output voltage with TP10 as the ground reference.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	PVIN input voltage connector. (See Table 1 for V _{IN} range.)
J2	VIN input voltage connector. Not normally used.
J3	2-pin header for tracking voltage input and ground
J4	V _{OUT} , 3.3 V at 8 A maximum
J5	2-pin header for tracking output and ground
JP1	PVIN to VIN jumper. Normally closed to tie VIN to PVIN for common rail voltage operation.
JP2	2-pin header for enable. Connect EN to ground to disable, open to enable.
TP1	PVIN test point at PVIN connector
TP2	GND test point at PVIN connector
TP3	VIN test point at VIN connector
TP4	GND test point at VIN connector
TP5	Test point provided to connect external voltage source for PWRGD pullup.
TP6	PWRGD test point
TP7	PH test point
TP8	Test point between voltage divider network and output. Used for loop response measurements.
TP9	Output voltage test point at VOUT connector
TP10	GND test point at VOUT connector



www.ti.com Test Setup and Results

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 2 A and then decreases as the load current increases toward full load. Figure 1 shows the efficiency for the TPS54821EVM-049 at an ambient temperature of 25°C.

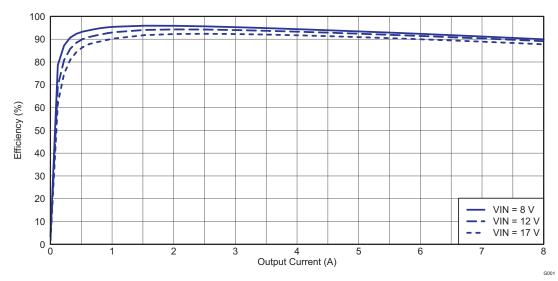


Figure 1. TPS54821EVM-049 Efficiency

Figure 2 shows the efficiency for the TPS54821EVM-049 using a semi-log scale to more easily show efficiency at lower output currents. The ambient temperature is 25°C.

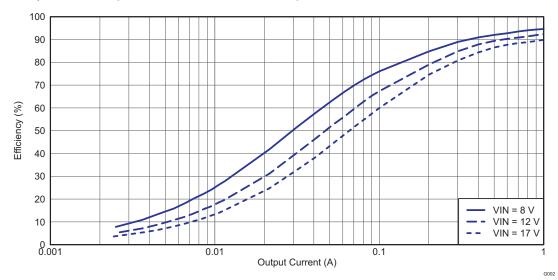


Figure 2. TPS54821EVM-049 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.



2.3 Output Voltage Load Regulation

Figure 3 shows the load regulation for the TPS54821EVM-049.

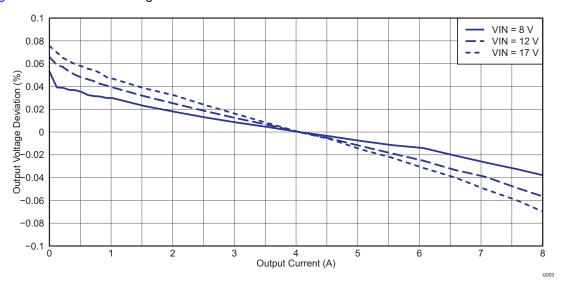


Figure 3. TPS54821EVM-049 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 4 shows the line regulation for the TPS54821EVM-049.

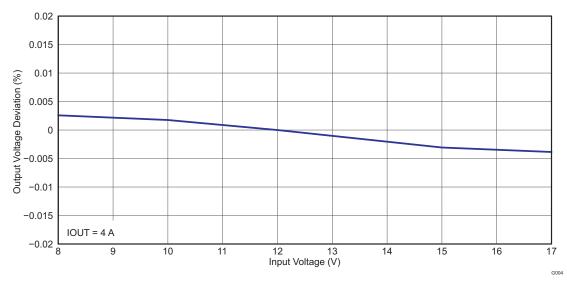


Figure 4. TPS54821EVM-049 Line Regulation



www.ti.com Test Setup and Results

2.5 Load Transients

Figure 5 shows the TPS54821EVM-049 response to load transients. The current step is from 25% to 75% of maximum rated load at 12-V input. The current step slew rate is 1 A/μs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

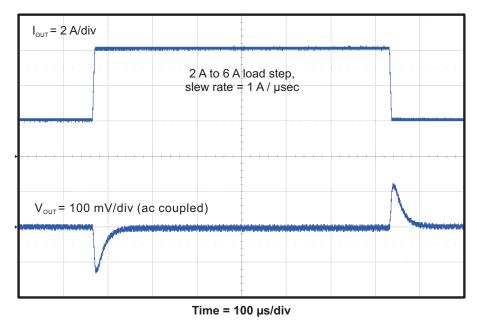


Figure 5. TPS54821EVM-049 Transient Response

2.6 Loop Characteristics

Figure 6 shows the TPS54821EVM-049 loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 8 A.

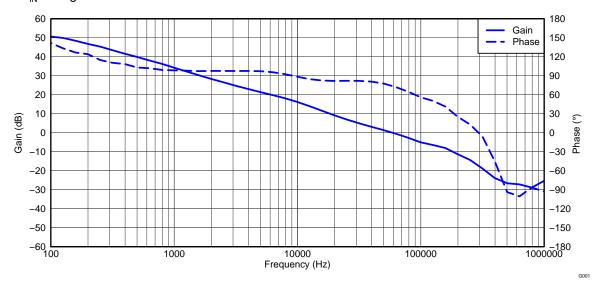


Figure 6. TPS54821EVM-049 Loop Response



2.7 Output Voltage Ripple

Figure 7 shows the TPS54821EVM-049 output voltage ripple. The output current is the rated full load of 8 A and $V_{\text{IN}} = 12 \text{ V}$. The ripple voltage is measured directly across the output capacitors.

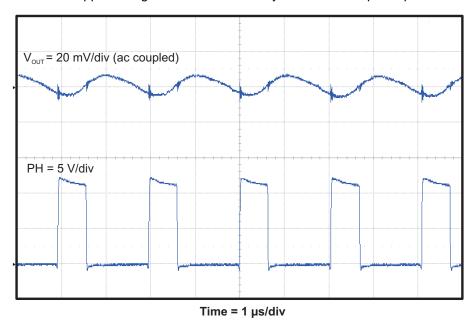


Figure 7. TPS54821EVM-049 Output Ripple

2.8 Input Voltage Ripple

Figure 8 shows the TPS54821EVM-049 input voltage. The output current is the rated full load of 8 A and $V_{IN} = 12$ V. The ripple voltage is measured directly across the input capacitors.

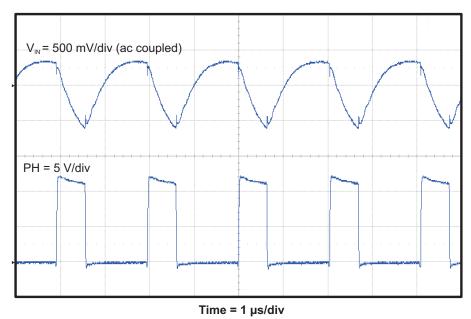


Figure 8. TPS54821EVM-049 Input Ripple



www.ti.com Test Setup and Results

2.9 Powering Up

Figure 9 and Figure 10 show the start-up waveforms for the TPS54821EVM-049. In Figure 9, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R1 and R2 resistor divider network. In Figure 10, the input voltage is initially applied and the output is inhibited by using a jumper at JP2 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 3.3 V. The input voltage for these plots is 12 V and the load is 1 Ω . PWRGD is pulled up to an external 5 V supply at TP5.

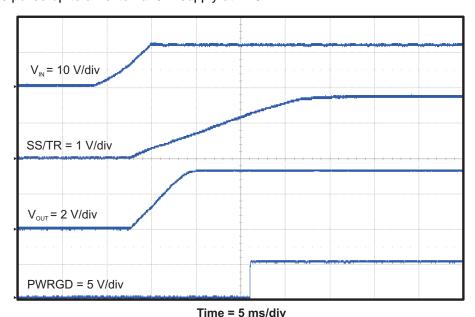


Figure 9. TPS54821EVM-049 Start-Up Relative to VIN

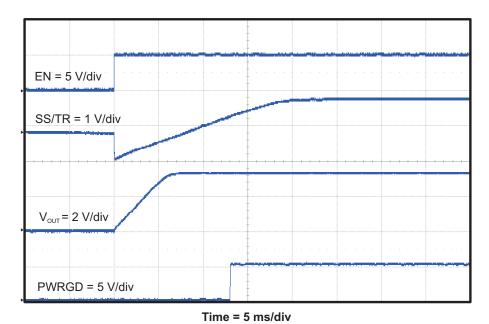


Figure 10. TPS54821EVM-049 Start-Up Relative to Enable



2.10 Pre-Bias Start-Up

The TPS54821 is designed to start up into a pre-biased output. The output voltage is not discharged to ground at the beginning of the slow-start sequence. Figure 11 shows the start-up waveform with the output voltage pre-biased to 1 V.

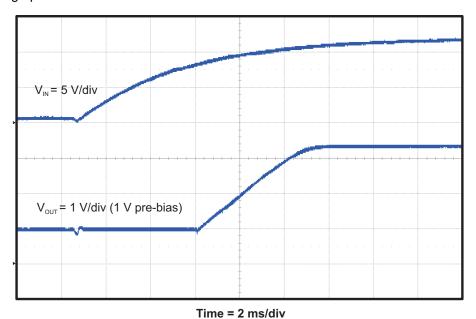


Figure 11. TPS54821EVM-049 Start-Up Into Pre-Bias

2.11 Hiccup-Mode Current Limit

The TPS54821 features hiccup-mode current limit. When an overcurrent event occurs, the TPS54821 shuts down and restarts. Figure 12 shows restart sequence in an over-current condition.

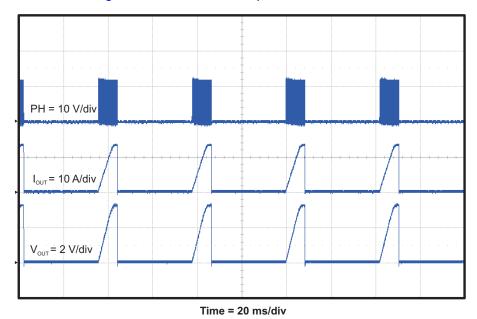


Figure 12. TPS54821EVM-049 Hiccup-Mode Current Limit



www.ti.com Board Layout

3 Board Layout

This section provides a description of the TPS54821EVM-049 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS54821EVM-049 is shown in Figure 13 through Figure 17. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for PVIN, VIN, V_{OUT} , and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54821 and a large area filled with ground. The internal layer-2 is primarily ground with additional fill areas for PVIN, VIN, and V_{OUT} . The bottom and internal layer-2 contain ground planes only. The top-side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board including five vias directly under the TPS54821 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane.

The input decoupling capacitors (C2 and C4) and bootstrap capacitor (C5) are all located as close to the IC as possible. Additionally, the voltage setpoint resistor divider components are kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the J4 output connector. For the TPS54821, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply. Critical analog circuits such as the voltage setpoint divider, frequency set resistor, slow-start capacitor, and compensation components are terminated to ground using a wide ground trace separate from the power ground pour.

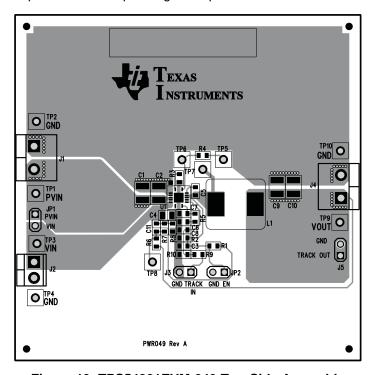


Figure 13. TPS54821EVM-049 Top-Side Assembly



Board Layout www.ti.com

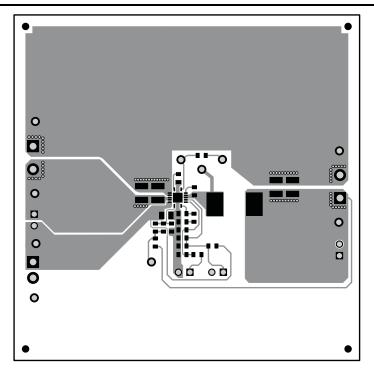


Figure 14. TPS54821EVM-049 Top-Side Layout

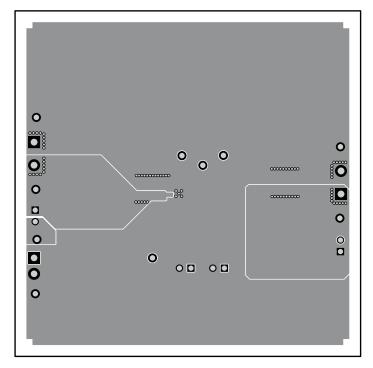


Figure 15. TPS54821EVM-049 Internal Layer-1 Layout



www.ti.com Board Layout

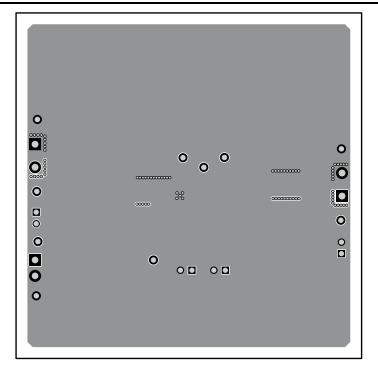


Figure 16. TPS54821EVM-049 Internal Layer-2 Layout

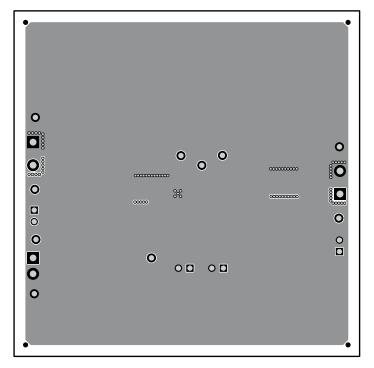


Figure 17. TPS54821EVM-049 Bottom-Side Layout



4 Schematic and Bill of Materials

This section presents the TPS54821EVM-049 schematic and bill of materials.

4.1 Schematic

Figure 18 is the schematic for the TPS54821EVM-049.

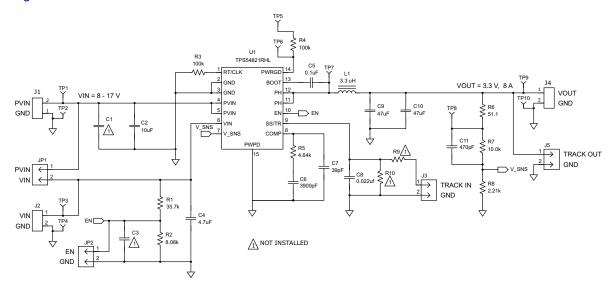


Figure 18. TPS54821EVM-049 Schematic



4.2 Bill of Materials

Table 5 presents the bill of materials for the TPS54821EVM-049.

Table 5. TPS54821EVM-049 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
0	C1	Open	Capacitor, Ceramic	1210	Std	Std
1	C2	10μF	Capacitor, Ceramic, 25V, X5R, 20%	1210	Std	Std
0	C3		Capacitor, Ceramic	0603	Std	Std
1	C4	4.7µF	Capacitor, Ceramic, 25V, X5R, 10%	0805	Std	Std
1	C5	0.1µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
1	C6	3900pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C7	39pF	Capacitor, Ceramic, 50V, COG, 10%	0603	Std	Std
1	C8	0.022µF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std
2	C9, C10	47µF	Capacitor, Ceramic, 10V, X5R, 10%	1210	Std	Std
0	C11	470pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	J2	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
2	J1, J4	ED120/2DS	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	OST
4	JP1, JP2,J3, J5	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	L1	3.3µH	Inductor, SMT, 10-A, 13.7milliohm	0.400 x 0.453 inch	IHLP4040DZ ER3R3M01	Vishay
1	R1	35.7k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	8.06k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R3, R4	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	4.64k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	51.1	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	2.21k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R9, R10	Open	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	TP1, TP3, TP7, TP9	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
6	TP2, TP4, TP5, TP6, TP8, TP10	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	U1	TPS54821RHL	IC, 1.6V-17V Synchronous Buck PWM Converter with Integrated MOSFET	3.5mm x 3.3mm QFN14	TPS54821RG HL	ТІ
2	_		Shunt, 100-mil, Black	0.100	929950-00	3M
1	_		Label (see note 5)	1.25 x 0.25 inch	THT-13-457- 10	Brady
1	_		PCB, 2.5" x 2.5" x 0.062"		PWR049	Any

Notes

- 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
- Ref designators marked with an asterisk (***) cannot be substituted. All other components can be substituted with equivalent MFG's components.
- 5. Install label in silkscreened box after final wash. Text shall be 8 pt font

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT**, **DEMONSTRATION**, **OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 4.5 V to 17 V and the output voltage range of 0.6 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products Applications

Audio www.ti.com/audio Communications and Telecom www.ti.com/communications **Amplifiers** amplifier.ti.com Computers and Peripherals www.ti.com/computers dataconverter.ti.com Consumer Electronics www.ti.com/consumer-apps **Data Converters DLP® Products** www.dlp.com **Energy and Lighting** www.ti.com/energy DSP dsp.ti.com Industrial www.ti.com/industrial Clocks and Timers www.ti.com/clocks Medical www.ti.com/medical Interface interface.ti.com Security www.ti.com/security

Logic Space, Avionics and Defense <u>www.ti.com/space-avionics-defense</u>

Power Mgmt power.ti.com Transportation and Automotive www.ti.com/automotive
Microcontrollers microcontroller.ti.com Video and Imaging www.ti.com/video

RFID <u>www.ti-rfid.com</u>
OMAP Mobile Processors www.ti.com/omap

Wireless Connectivity <u>www.ti.com/wirelessconnectivity</u>

TI E2E Community Home Page <u>e2e.ti.com</u>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated