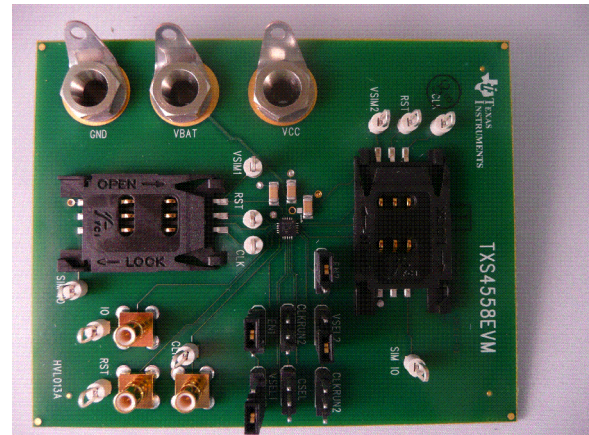


TXS4558 Evaluation Module

1 Features

- Dual 1.8V/3V Sim card power supply with translator
- On board SIM sockets for easy evaluation
- SMB and testpoint options for signal connections
- Jumpers provided for manipulation of device control signals
- Multiple test points for evaluation and signal probing



2 EVM Description

The Texas Instruments TXS4558 Evaluation Module (EVM) is designed to showcase the TXS4558, a complete dual-supply standby Smart Identity Module (SIM) card solution for interfacing wireless baseband processors with two individual SIM subscriber cards to store data for mobile handset applications. This device is targeted to GPIO control and communication, where GPIO signals are used to switch between SIMs and SIM modes, allowing a single interface to support two SIMs.

The TXS4558 also incorporates shutdown sequence for the SIM card pins based on the ISO 7816-3 specification for SIM cards. It has 8kV HBM protection for the SIM card pins and standard 2kV HBM protection for all the other pins.

This EVM includes two sockets for SIM cards, as well as test points interfacing all device signals. Jumpers, connectors and test points are all labeled with device signal names.

3 Jumper Configurations

Seven of the control pins are interfaced using three pin headers. The seven signals are EN1, EN2, VSEL1, VSEL2, CLKRUN1, CLKRUN2, and CSEL.

Three pin headers are configured such that center pin corresponds to the labeled signal. Left pin is tied to VCC. Right pin of the three pins is GND. This allows easy placement of jumpers for input configuration, while giving the option of external signal connection directly to header pin if required.

4 Setup Procedure

4.1 Power Supply Connections

J11 is labeled GND. This should be connected to the GND of both power supplies.

J13 is labeled VCC, which can support 1.65 V to 3.3 V.

J12 is labeled VBAT. VBAT supports 2.3 V to 5.5 V.

4.2 Jumper Settings

To enable both LDOs at the 2.95V setting

J3 is EN2. A jumper should be placed connecting the center and left pin. This connects EN2 to VCC and enables VSIM2.

J1 is EN1. A jumper should be placed connecting the center and left pin. This connects EN2 to VCC and enables VSIM2.

J2 is VSEL1. A jumper should be placed connecting the center and left pin. This connects VSEL1 to VCC and sets the LDO to output 2.95V.

J4 is VSEL2. A jumper should be placed connecting the center and left pin. This connects VSEL2 to VCC and sets the LDO to output 2.95V.

These settings can be changes according to LDO requirements.

4.3 General Settings

When connecting signals, minimize connection length and keep GND leads short when probing. This will ensure minimal capacitive, resistive and inductive loading caused by the connection and connectors. For more information about the device please see the TXS4558 datasheet, or TI's support forum e2e.ti.com

5 PCB Layout

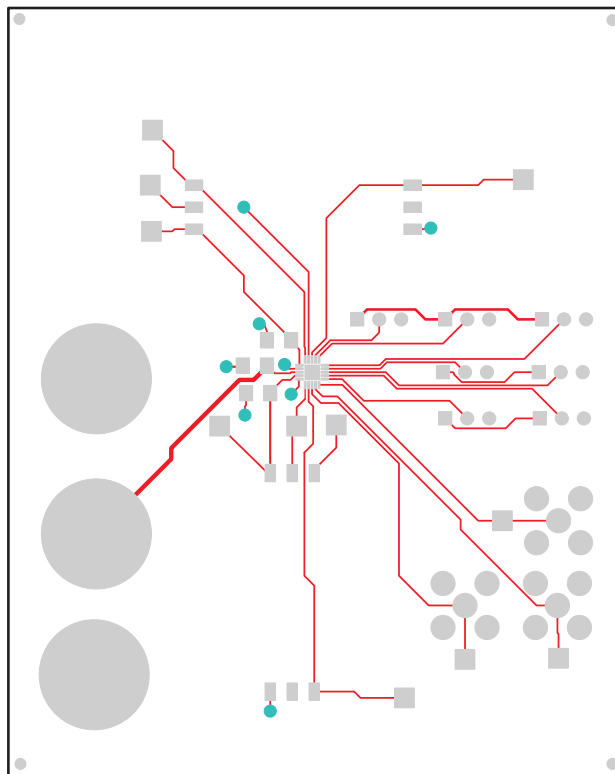


Figure 1. Top Layer

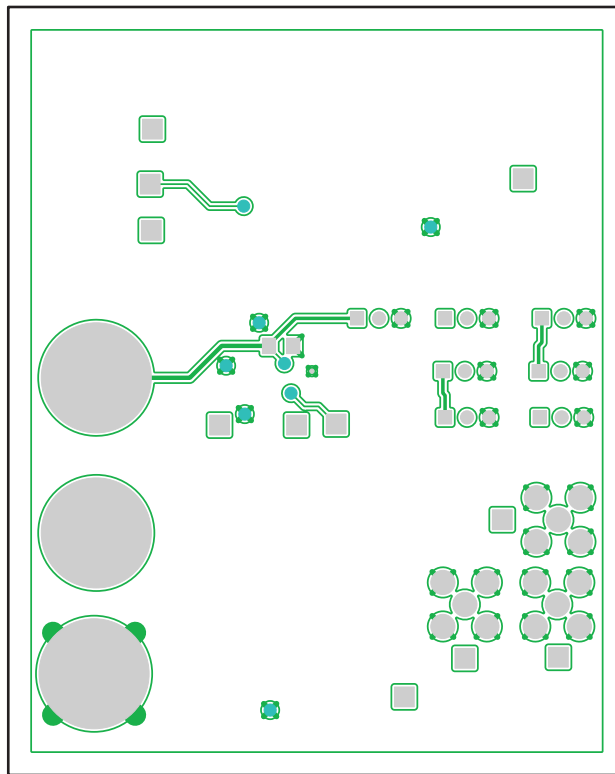


Figure 2. Bottom Layer

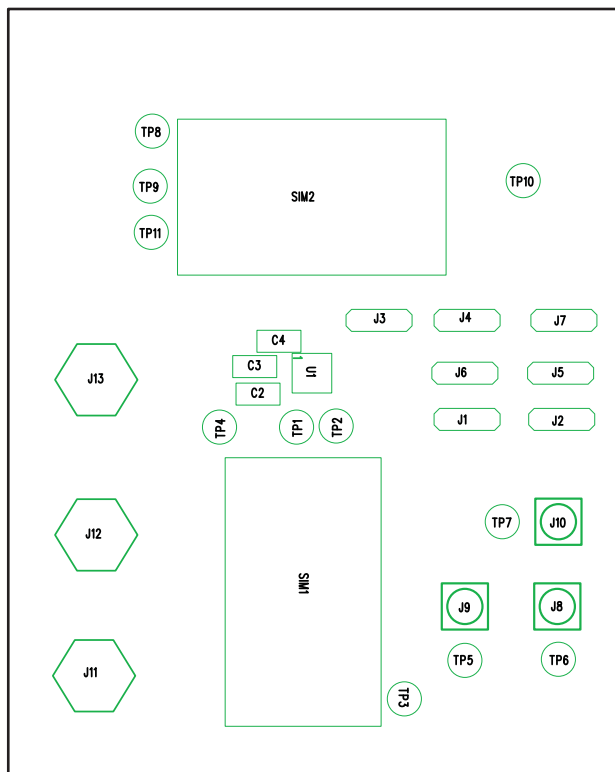


Figure 3. Assembly Top Layer

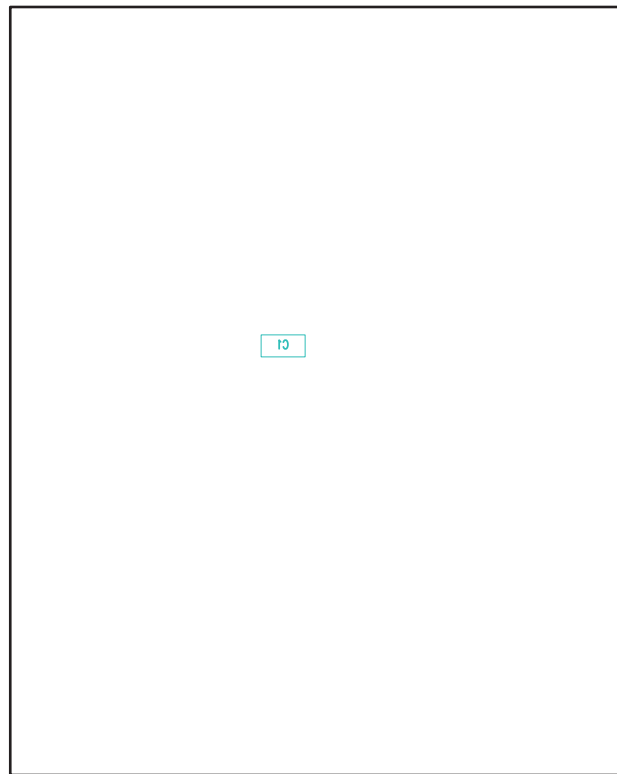


Figure 4. Assembly Bottom Layer

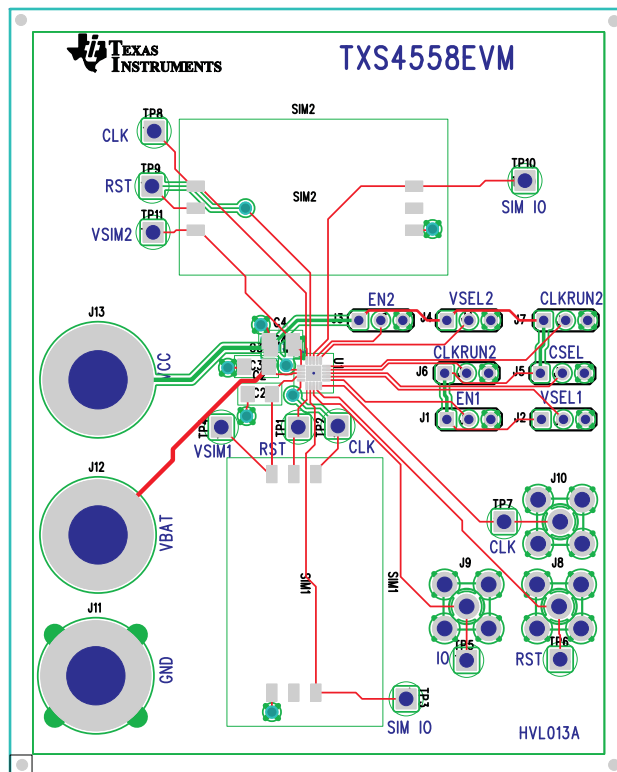


Figure 5. Composite

Table 1. Bill of Materials⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	0.1 μ F	Capacitor, Ceramic, 50V, X7R, \pm 10%	1206	GRM319R71H104KA01D	STD
3	C2, C3, C4	1 μ F	Capacitor, Ceramic, 16V, X7R, \pm 20%	1206	GRM319R71C105MC11D	STD
4	J1, J2, J3, J4, J5, J6, J7	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
3	J11, J12, J13		Connector, Banana Jack, Uninsulated	0.500 dia. inch	108-0740-001	Emerson
3	J8, J9, J10		Connector, SMB, Straight, PC mount	0.210 sq inch	131-3701-261	Emerson
2	SIM1, SIM2	7111S2015X02	Socket , SIM	17.20 X 29.70 mm	7111S2015X02LF	FCI
11	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11	5012	Test Point, 0.062 Hole	0.250 inch	5012	Keystone
1	U1	TXS4558RUK	IC, Dual-SIM Card P/S With Level Translator and Dedicated Dual LDO	QFN	TPS4558RUK	TI
4			Shunts, 100 mil, Black	0.100	929950-00	3M<
1	-		PCB, 3.5 In x 2.9 In x 0.062 In		HVL013	Any

- ⁽¹⁾ These assemblies are ESD sensitive, ESD precautions shall be observed.
- ⁽²⁾ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- ⁽³⁾ These assemblies must comply with workmanship standards IPC-A-610 Class 2.
- ⁽⁴⁾ Ref designators marked with an asterisk (***) cannot be substituted. All other components can be substituted with equivalent MFG's components.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 1.65 V to 3.3 V and the output voltage range of 2.3 V to 5.5 V . Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 75°C. The EVM is designed to operate properly with certain components above 75°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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