User's Guide
SLVU600–December 2011

TPS7A8101EVM Evaluation Module

This user's guide describes the characteristics, operation, and use of the TPS7A8101EVM. This evaluation module (EVM) demonstrates the Texas Instruments TPS7A8101 low-dropout (LDO) linear regulator in a 3-mm x 3-mm, SON-8 package, which is capable of a 1-A output current. This user's guide includes setup instructions, a schematic diagram, thermal guidelines, a bill of materials, and printed-circuit board layout drawings for the evaluation module.

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1 Introduction

The TPS7A8101EVM evaluation module helps designers evaluate the operation and performance of the TPS7A8101 adjustable-output LDO. Because the TPS7A8101 is adjustable, the EVM has been designed to provide several common output voltages which can be selected using an onboard jumper. The EVM can provide output voltages of 1.8 V, 2.5 V, 2.8 V or 3.3 V using the jumper. Other output voltages can be evaluated but require changing the feedback resistors.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS7A8101EVM.

2.1 Input/Output Connector Descriptions

2.1.1 J1 – VIN

This is the positive input supply voltage. The connector for J1 is not populated on the TPS7A8101EVM. This footprint allows the mounting of an SMA-style connector for more accurate PSRR measurements. See the bill of materials (BOM) for the manufacturer and part number of the corresponding connector.

2.1.2 J2 – VOUT

This is the output voltage. The connector for J2 is not populated on the TPS7A8101EVM. This footprint allows the mounting of an SMA-style connector for more accurate PSRR measurements. See the BOM for the manufacturer and part number of the corresponding connector.

2.1.3 J3 – VIN

This is the positive connection to the input power supply. The power supply must be connected between J1 and J8 (GND). Twist the leads to the input supply, and keep them as short as possible. The input voltage must be between 2.2 V and 6.5 V.

2.1.4 J4 – VOUT

This is the positive output voltage of the LDO. The output voltage of the TPS7A8101 is adjustable with feedback resistors. On the EVM, the output voltage is set using J6.

2.1.5 J5 – ENABLE

This jumper is used to enable or disable the output of the TPS7A8101. Placing a shorting jumper between pins 1 and 2 (*ON* position) enables the TPS7A8101. Placing the shorting jumper between pins 2 and 3 (*OFF* position) disables the TPS7A8101.

2.1.6 J6 – Output Voltage Select

This jumper is used to set the desired output voltage from the TPS7A8101. Placing a shorting jumper between the appropriate pins gives the corresponding outputs. The output voltage of the TPS7A8101EVM must only be changed when the TPS7A8101EVM is not powered. Installing and removing the jumper with the board powered can lead to undesired or unregulated output voltage

Short Pins	VOUT (V)
1 and 2	3.3
3 and 4	2.8
5 and 6	2.5
7 and 8	1.8

2.1.7 J7 and J8 – GND

This is the return connection to the input power supply. Connect the power supply between J7 or J8 and J3 (VIN). Twist the leads to the input supply, and keep them as short as possible. The input voltage must be between 2.2 V and 6.5 V.

3 TPS7A8101 Device Operation

This section provides information about the operation of the TPS7A8101EVM.

3.1 Test Procedure

Ensure that the input power supply is off. Connect the positive input power supply to J3. Connect the input power return (ground) to J7. The TPS7A8101 has an absolute maximum input voltage of 7 V. The recommended maximum operating voltage is 6.5 V. The actual highest input voltage may be less than 6.5 V due to thermal conditions. See the Thermal Considerations Section 4 of this manual to determine the highest input voltage.

Connect the desired load between J4 (positive lead) and J8 (negative or return lead). Configure jumper J6 for the desired output voltage. Turn on the input power supply.

3.2 Test Data

Figure 1 through Figure 5 present typical performance curves for the TPS62060EVM. Actual performance data can be affected by measurement techniques and environmental variables; therefore, these curves are presented for reference and may differ from actual results obtained by some users.

3.2.1 PSRR

Figure 1 and Figure 2 show the typical PSRR performance for the TPS7A8101EVM.

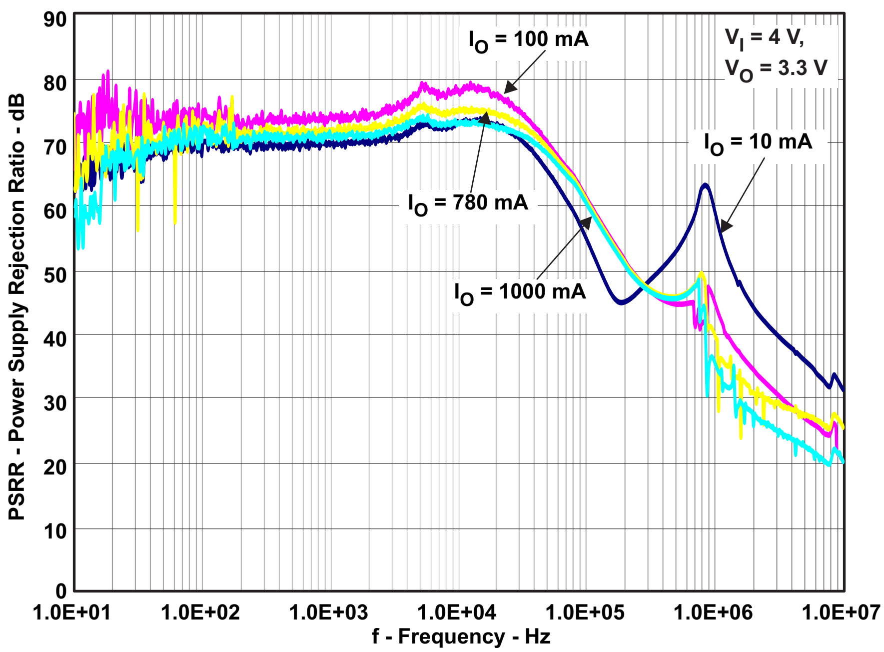

Figure 1. TPS7A8101 PSRR for Variable Output Currents, VDO=0.7 V

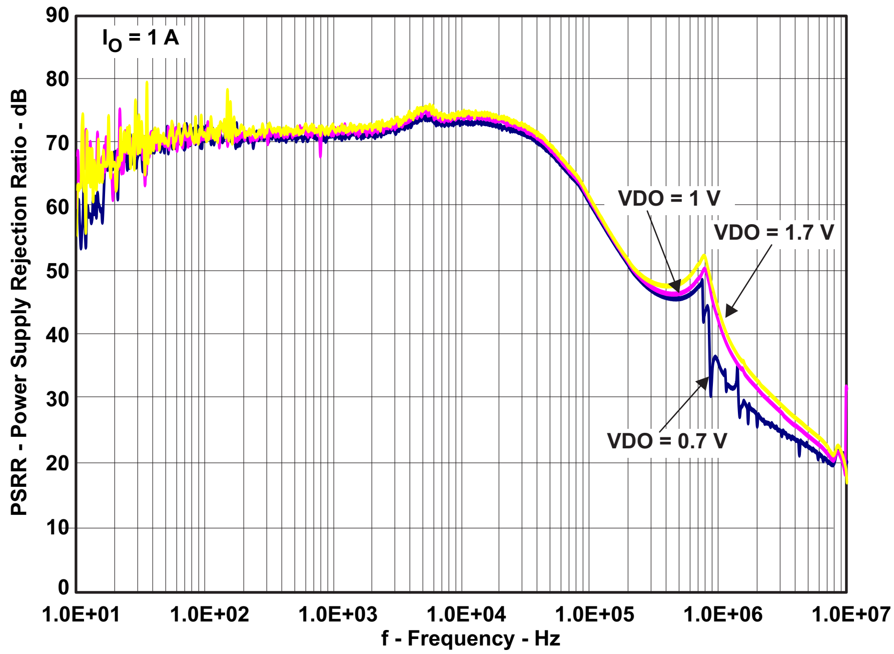

Figure 2. TPS7A8101 PSRR for Variable Dropout Voltage, Iout=1 A

3.2.2 Start-up

Figure 3 shows the typical start-up performance for the TPS7A8101EVM.

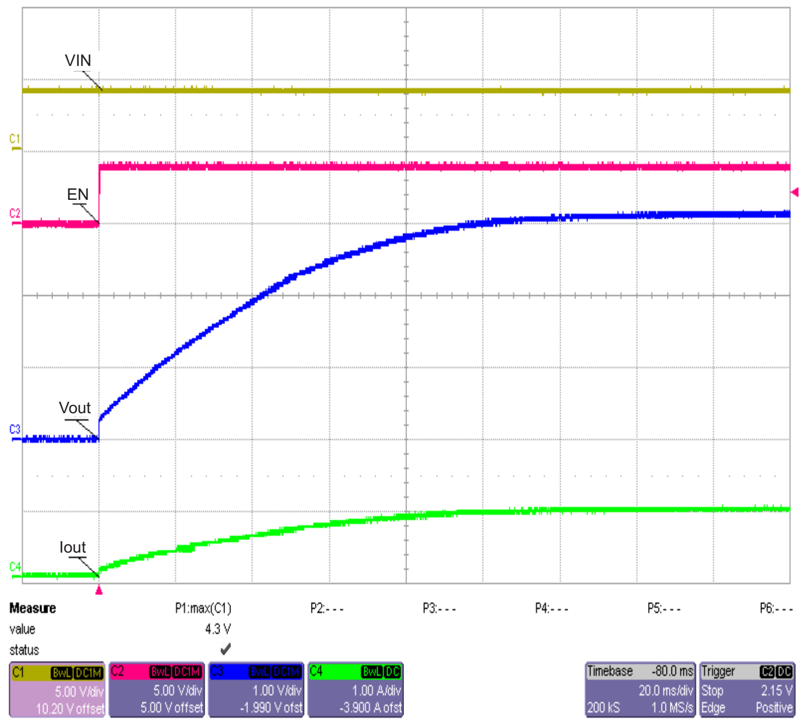

Figure 3. TPS7A8101 Start-Up Into Full Load, 1 A

3.2.3 Shutdown

Figure 4 shows the typical shutdown performance for the TPS7A8101EVM.

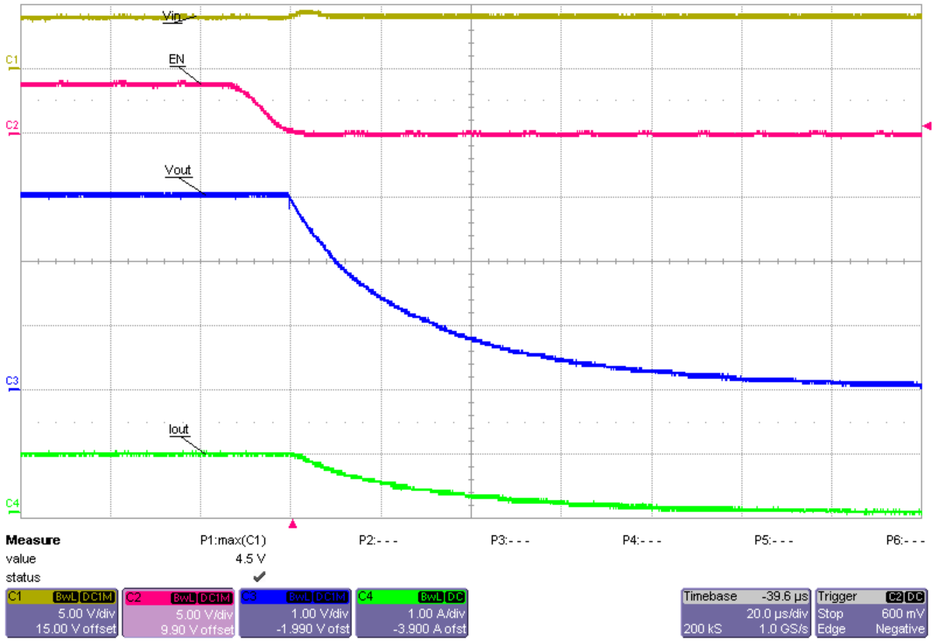

Figure 4. TPS7A8101 Shutdown with 3.3-Ω Load

3.2.4 Transient Performance

Figure 5 shows the load transient response of the TPS7A8101EVM.

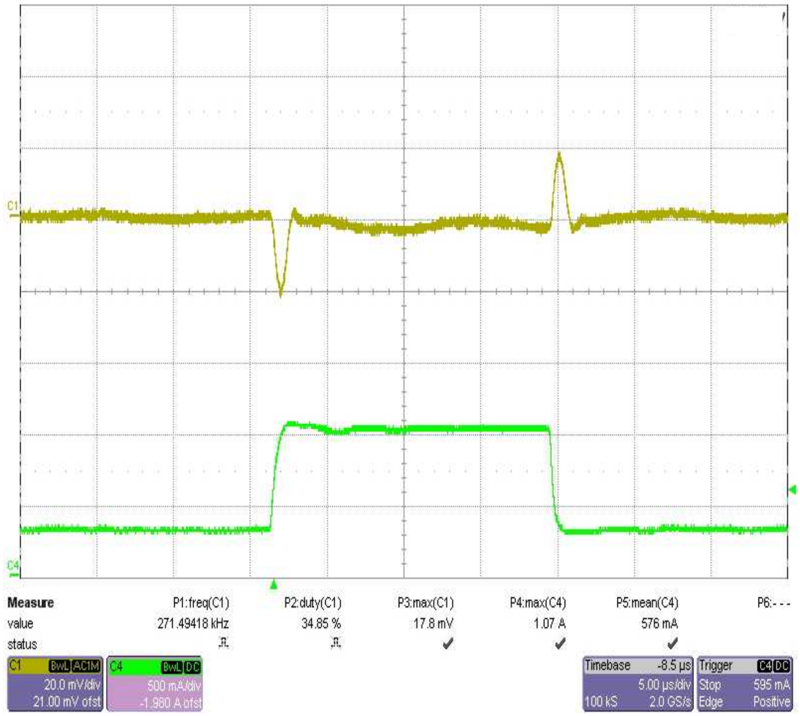

Figure 5. TPS7A8101 Transient Response

4 Thermal Guidelines

This section provides guidelines for the thermal management of the TPS7A81xxDRBEVM board.

4.1 Thermal Considerations

Thermal management is a key design component of any power converter and is especially important when the power dissipation in the LDO is high. To better help you design the TPS7A81xxDRB family into your application, use Equation 1 to approximate the maximum power dissipation at a particular ambient temperature:

$$T_J = T_A + P_d \times \theta_{JA} \quad (1)$$

where T_J is the junction temperature, T_A is the ambient temperature, P_d is the power dissipation in the integrated circuit (IC) and θ_{JA} is the thermal resistance from junction to ambient. All temperatures are in degrees Celsius.

The measured thermal resistance from junction to ambient for the TPS7A8101EVM has a typical value of 45.7°C/W. The recommended maximum operating junction temperature specified in the data sheet for the TPS7A8101 is 125°C. With this information, the maximum power dissipation can be found by using Equation 1.

Table 1 shows the maximum input voltage that can be applied to the input of the TPS7A8101EVM and still provide the full 1 A of output current. Table 1 shows the input voltage versus the output voltage setting and two ambient temperatures (25°C and 85°C). The maximum input voltage shown provides the rated output current while keeping the junction temperature at or below the recommended 125°C.

Table 1. Maximum Input Voltage vs Ambient Temperature and Output Voltage

		Selected Output Voltage (V)			
Ambient Temp	**Iout (A)**	**1.8**	**2.5**	**2.8**	**3.3**
25	1.00	3.98	4.68	4.98	5.48

Table 1. Maximum Input Voltage vs Ambient Temperature and Output Voltage (continued)

		Selected Output Voltage (V)			
Ambient Temp	**Iout (A)**	**1.8**	**2.5**	**2.8**	**3.3**
85	1.00	2.67	3.37	3.67	4.17

5 Board Layout

5.1 Layout

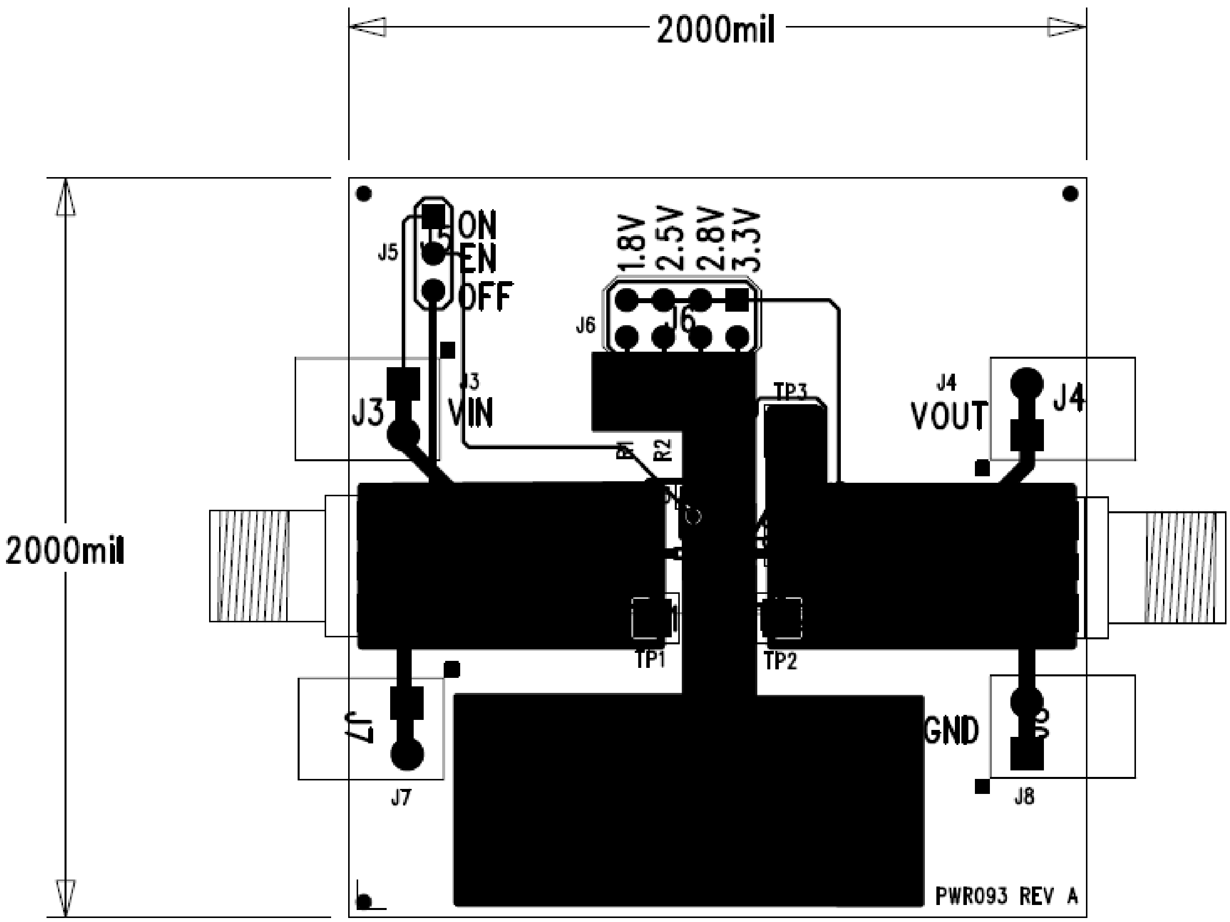

Figure 6. Top Layer Assembly

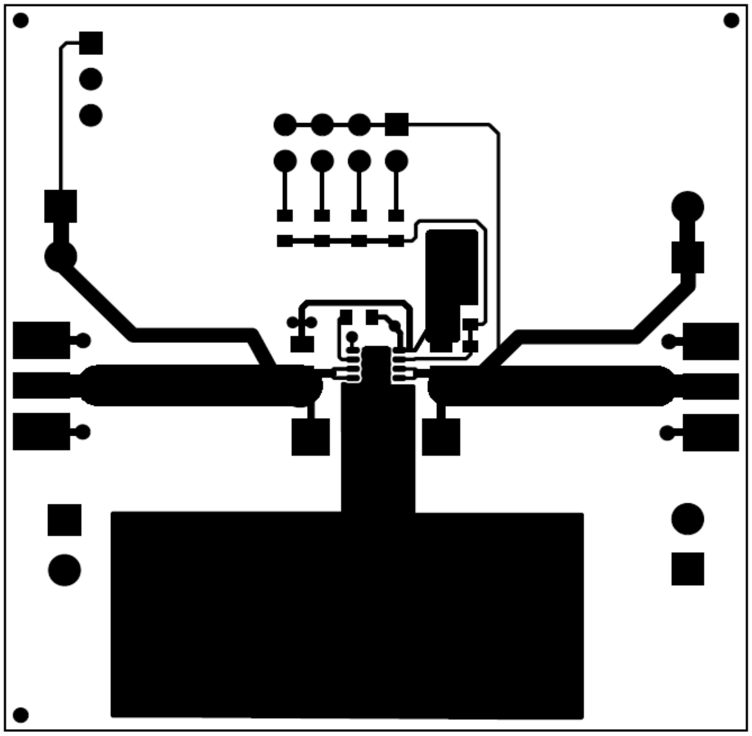

Figure 7. Top Layer Routing

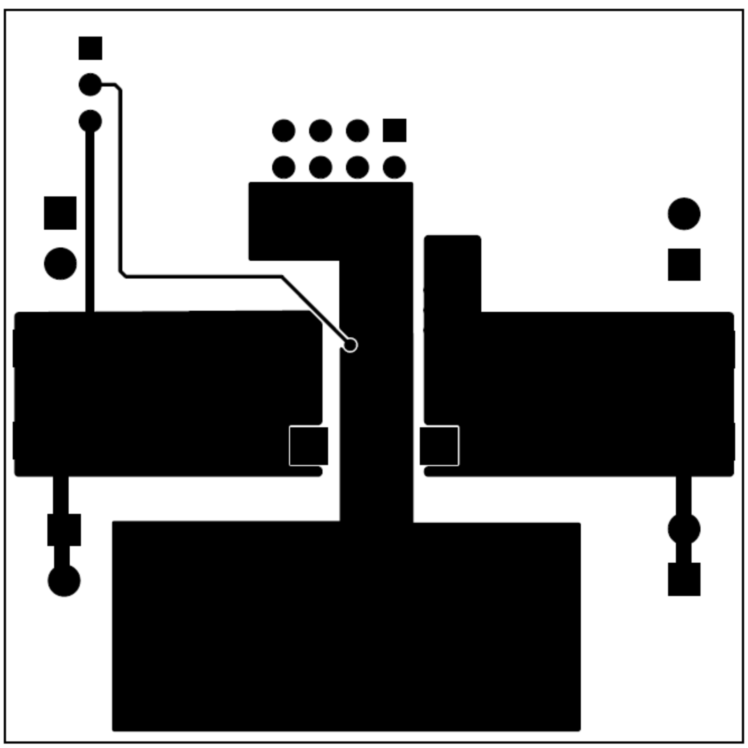

Figure 8. Bottom Layer Routing

6 Schematic and Bill of Materials

This section provides the TPS7A8101EVM board schematic and BOM.

6.1 Schematic

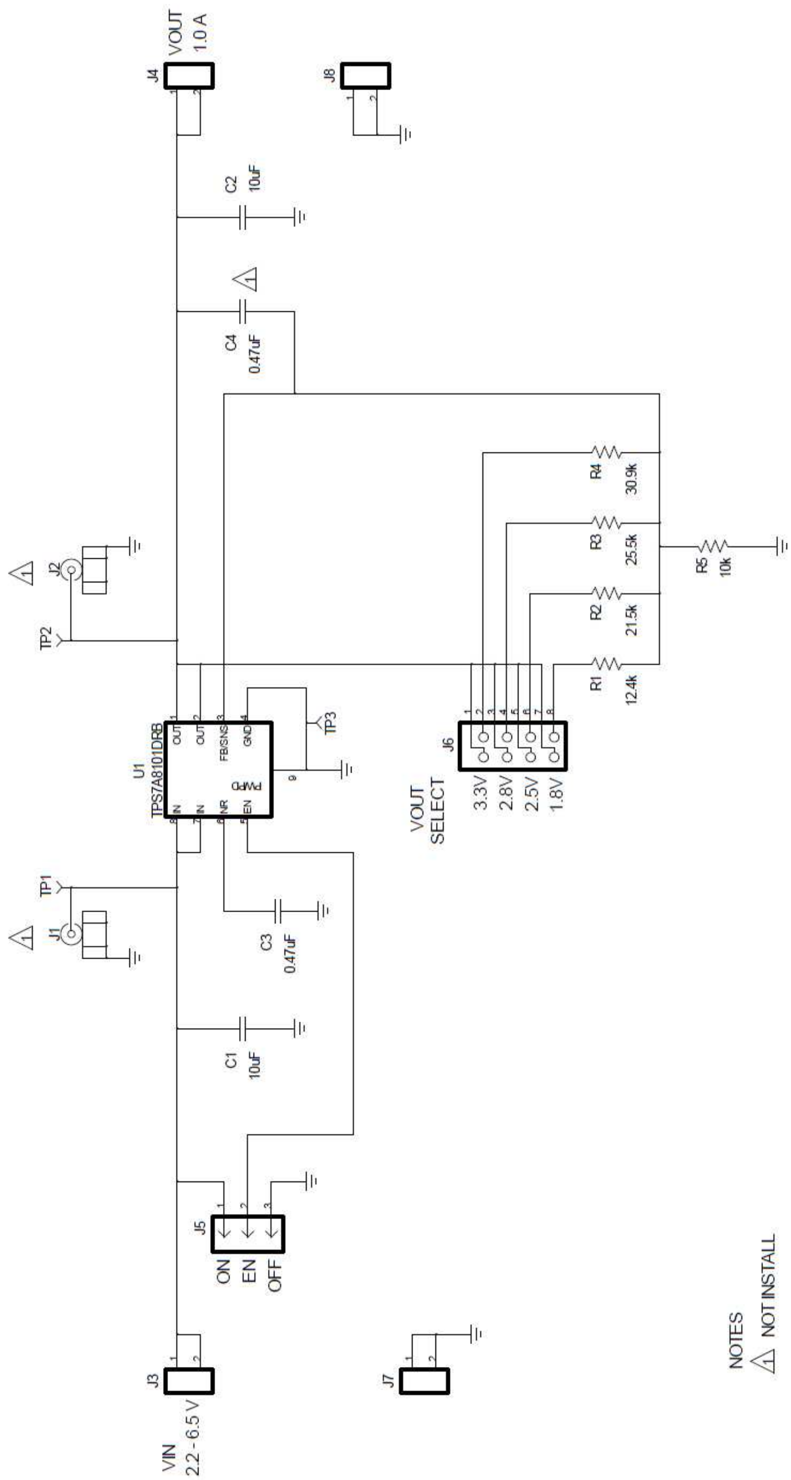

Figure 9. TPS7A8101EVM Schematic

6.2 Bill of Materials

Table 2. Bill of Materials

Count	RefDes	Value	Description	Size	Part No.	MFR
2	C1, C2	10µF	Capacitor, Ceramic, 10V, X7R, 10%	0805	Std	Std
2	C3, C4	0.47µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
0	J1, J2	142-0711-821	CONNECTOR, SHIELDED, END LAUNCH JACK, GOLD PLATED, FOR 0.062 PCB, EDGE MOUNTED	0.250 SQ	142-0711-821	STD
4	J3, J4, J7, J8	ED550/2DS	Terminal Block, RA 2-pin, 6-A, 3.5mm	7.0 x 8.2 mm	ED550/2DS	OST
1	J5	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	J6	PEC04DAAN	Header, Male 2x4-pin, 100mil spacing	0.20 x 0.40 inch	PEC04DAAN	Sullins
1	R1	12.4k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	21.5k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	25.5k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	30.9k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	10k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	TP1	5010	Test Point, Red, Thru Hole	0.125 x 0.125 inch	5010	Keystone
1	TP2	5013	Test Point, Orange, Thru Hole	0.125 x 0.125 inch	5013	Keystone
1	TP3	5011	Test Point, Black, Thru Hole	0.125 x 0.125 inch	5011	Keystone
1	U1	TPS7A8101DRB	IC, Low Noise, High-Bandwidth PSRR LDO 1A Linear Regulator	DRB-8	TPS7A8101DRB	TI
1	–		PCB, 2 In x 2 In x 0.62 In		PWR093	Any
2		15-29-1025	Shunt, 2 pos 0.100 In Gold		15-29-1025	Molex

Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable..
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2.2 V to 6.5 V and the output voltage range of 0.8 V to 6 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85° C. The EVM is designed to operate properly with certain components above 85° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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