Texas Instruments

User's Guide
SLVU602–November 2011

TPS7A3301EVM-061

This User's Guide describes operational use of the TPS7A3301EVM-061 Evaluation Module (EVM) as a reference design for engineering demonstration and evaluation of the TPS7A3301, low-dropout negative-voltage linear regulator (LDO). Included in this user's guide are setup instructions, a schematic diagram, layout and thermal guidelines, a bill of materials, and test results.

Contents

List of Figures

List of Tables

1 Introduction

The Texas Instruments TPS7A3301EVM-061 EVM helps design engineers to evaluate the operation and performance of the TPS7A33xx family of linear regulators for possible use in their own circuit applications. This particular EVM is preconfigured to output –15 V and contains a single linear regulator (LDO) with internal current limit and thermal shutdown protection. The TPS7A33xx family of low-dropout regulators allows input voltages from –3 V to –36 V and can be adjusted to any output voltage between –1.2 V and –20 V by only changing a resistor value in accord with the given equation. The regulator, including external components, is capable of delivering up to 1 A to the load depending on the input-output power dissipation across the part. The TPS7A33xx has been optimized for ac performance, including PSRR and load transient response, using capacitors rated over the full voltage range of the regulator. The TPS7A33xx family is available in a TO220-7 KVT bent-lead package.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS7A3301EVM.

2.1 Input/Output Connectors and Jumper Descriptions

2.1.1 J1 — (–)Vin

Negative input power supply voltage connector. The negative input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize EMI transmission. Additional bulk capacitance should be added between J1 and J3 if the supply leads are greater than six inches. For example, an additional 47-µF electrolytic capacitor connected from J1 to ground can improve the transient response of the TPS7A3301 while eliminating unwanted ringing on the input due to long wire connections. A (+) power supply may be used if the (+) lead is connected to J2 (GND) and the GND lead is connected to J1 (–VIN).

2.1.2 J2 — GND

Ground-return connector for the input power supply

2.1.3 J3 — (–)Vout

Regulated (–) output voltage connector

2.1.4 J4 — GND

Output ground-return connector

2.1.5 JP1 — EN

Output enable. To enable the output, connect a jumper to short the ON pin 1 to the EN center pin 2. To disable the output, connect a jumper to short EN pin 2 to OFF pin 3.

2.2 Equipment Setup

- Turn off the input power supply after verifying that its output voltage is set to greater than –15 V (–18 V recommended; –36 V maximum). Connect the negative voltage lead from the input power supply to –VIN, at the J1 connector of the EVM. Connect the ground lead from the input power supply to GND at the J2 connector of the EVM. If using a (+) power supply, connect the (+) lead is to J2 (GND) and the GND lead J1 (–VIN).
- Connect desired (≤1 A) load between the –VOUT pin at connector J3, and the GND pin at connector J4. Be careful to calculate the power dissipation across the part for the desired –VIN level.

3 Operation

- Turn on the input power supply. For initial operation, it is recommended that the input power supply, –VIN on J1, be set to –18 V.
- Vary the load and –VIN voltage as necessary for test purposes.

4 Adjustable Operation

The nominal output voltage for the typical LDO circuit employing the TPS7A3301 is set by two external resistors, R1and R2, as illustrated in Figure 1. R1 and R2 can be calculated for any output voltage using Equation 1 and the Vref voltage found in the device data sheet under the Electrical Characteristics.

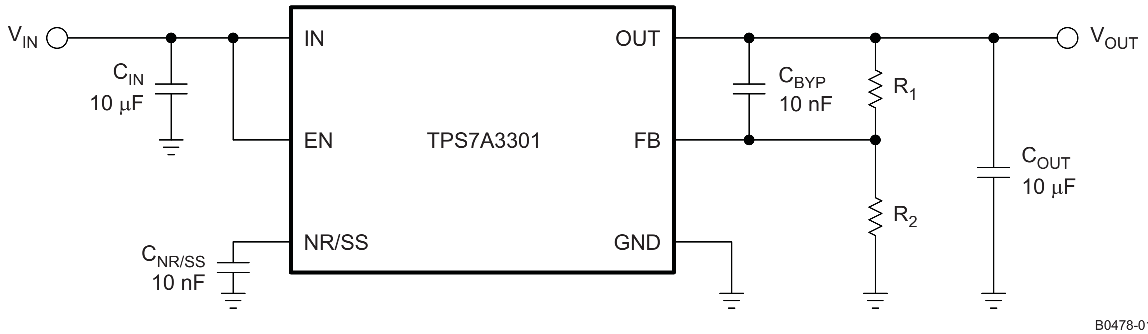


Figure 1. TPS7A3301 LDO Schematic Showing Adjustment Resistors

$$R_2 = R_1 \div ((V_{OUT}/V_{FB}) - 1), \quad \text{where} \quad V_{OUT} / (R_1 + R_2) \geq 5\ \mu A \tag{1}$$

Once the resistor values have been calculated, the new resistors can be installed appropriately in the correct place using the PCB and schematic diagrams of Figure 4 5 through Figure 7.

Suggestion: When recalculating the resistor values for a particular desired output voltage, change only the R2 value in order to maintain the frequency-domain zero formed by R1 and C_{BYP} in accord with Equation 2.

$$F_Z = 1 / (2 \times \pi \times R_1 \times C_{BYP}) \tag{2}$$

For additional information on adjustable operation, see the TPS7A3301 data sheet (SBVS169).

5 Test Results

This section provides typical performance waveforms for the TPS7A3301EVM-061 printed circuit board.

5.1 Turnon Sequence

Figure 2 shows the hard turnon characteristic where –VIN is –18 V, EN (C1, yellow) is switched on to –18 V and the output drives a 1-A load (C4, green). The output (C3, blue) shows a fairly monotonic rise time of approximately 800 ms.

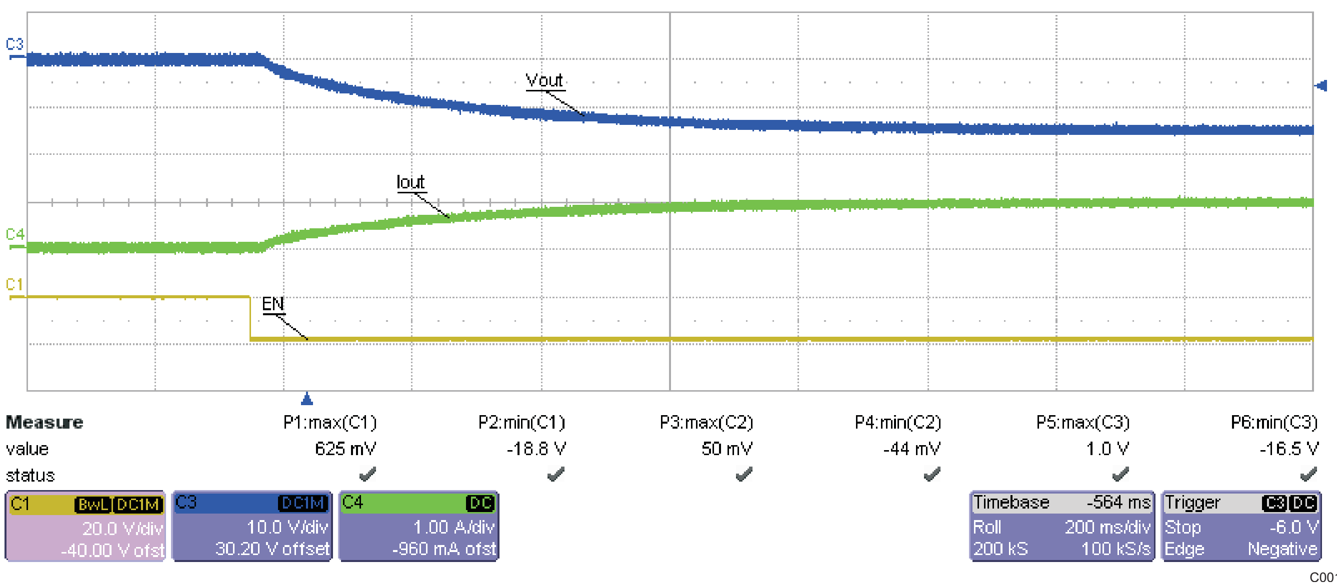
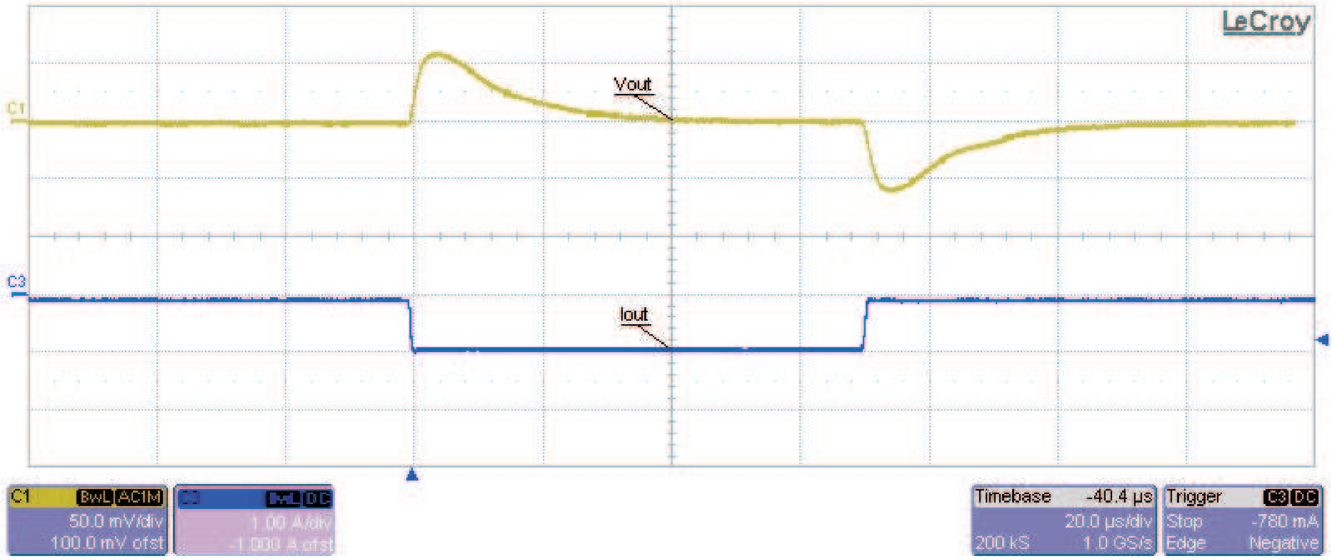


Figure 2. Turnon Sequence

5.2 Output Load Transient

Figure 3 shows the load transient response (Vout - C1, yellow) for a full-load step transient from 100 mA to 1 A (C3, blue). This test was run with the EVM set up for –5-V –VOUT and –VIN was set at –8 V.



C002

Figure 3. Load Step and Transient Response

6 Thermal Guidelines and Layout Recommendations

Thermal management is a key component of the design of any power converter and is especially important when the power dissipation in the LDO is high. Use the following formula to approximate the maximum power dissipation for the particular ambient temperature:

$$T_J = T_A + P_D \times \theta_{JA} \qquad (3)$$

where T_J is the junction temperature, T_A is the ambient temperature, P_D is the power dissipation in the device (watts), and θ_{JA} is the thermal resistance from junction to ambient. All temperatures are in degrees Celsius. The maximum silicon junction temperature, T_J, must not be allowed to exceed 150°C. The layout design must use copper trace and plane areas smartly, as thermal sinks, in order not to allow T_J to exceed the absolute maximum rating under all temperature conditions and voltage conditions across the part. The designer must consider carefully the thermal design of the PCB for optimal performance over temperature. The actual allowable power dissipation on a PCB is a strong function of its layout.

Heat flows from the device to the ambient air through many paths, each of which represents resistance to the heat flow; this resistance is called thermal resistance.

The total thermal resistance of a system is defined by Equation 4:

$$\theta_{JA} = \frac{(T_J - T_A)}{P_D} \qquad (4)$$

where θ_{JA} is the thermal resistance (in °C/W), T_J is the allowable junction temperature of the device (in °C), T_A is the maximum temperature of the ambient cooling air (in °C), and P_D is the amount of power (heat) generated by the device (in W).

Whenever a heatsink is installed, the total thermal resistance (θ_{JA}) is the sum of all the individual resistances from the device, going through its case and heatsink to the ambient cooling air.

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \qquad (5)$$

Realistically, the user can only control two resistances, θ_{CS} and θ_{SA}. Therefore, for a device with a known θ_{JC}, θ_{CS} and θ_{SA} become the main design variables in selecting a heat sink.

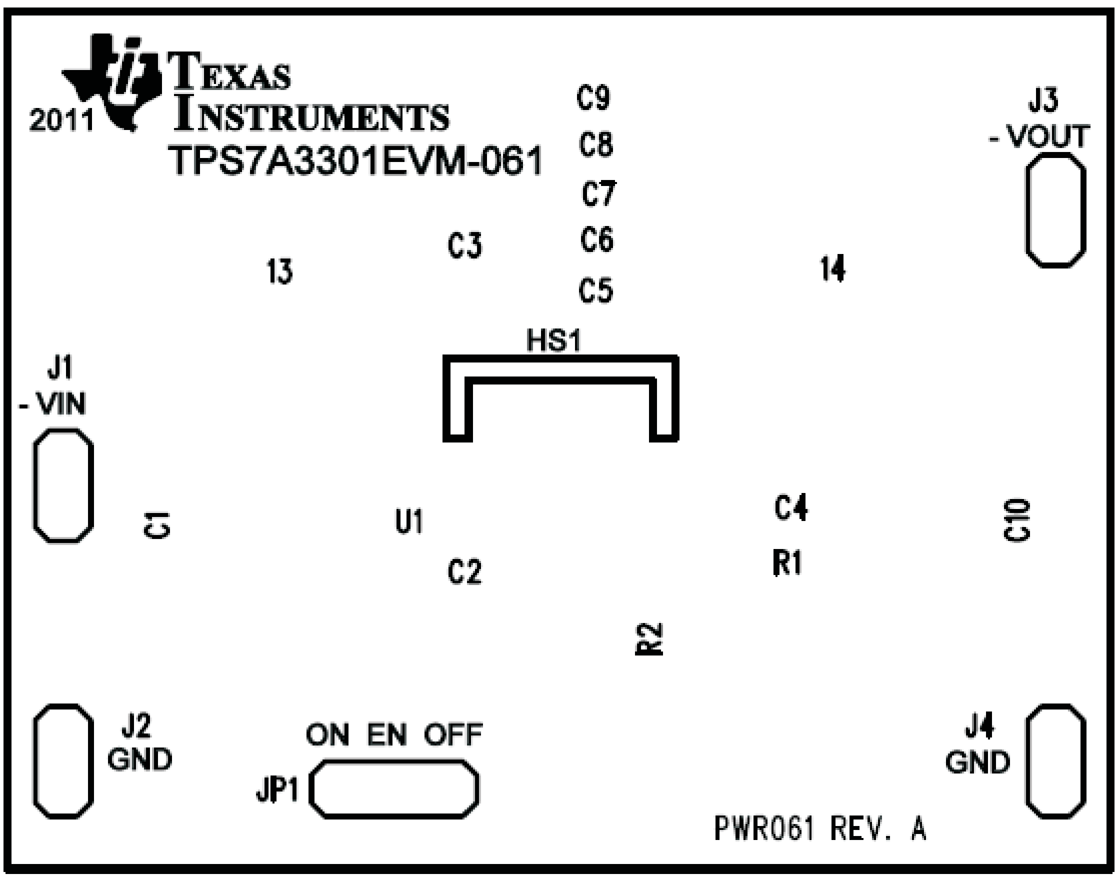
The thermal interface between the case and the heat sink, θ_{CS}, is controlled by selecting the right heat conducting material. Once the θ_{CS} is selected, the required thermal resistance from the heatsink to ambient is calculated by Equation 6:

$$\theta_{SA}\left[\frac{(T_J - T_A)}{P_D}\right] - (\theta_{JC} + \theta_{CS}) \tag{6}$$

This information allows the user to select the most appropriate heatsink for any particular application.

The heat sink chosen for the TPS7A3301EVM-061 (507302B00000G from Aavid) has a specified thermal resistance (θ_{SA}) of 24°C/W. There is also an option of using the two large mounting holes (13 and 14 – see Figure 4) to mount a heat sink with a smaller thermal resistance. The mounting holes are sized for the use of any heat sink with solderable mounting tab spacing of 1 inch (25.4 mm). The 5310 series from Aavid is one example and has a specified thermal resistance (θ_{SA}) of 13.4°C/W.

7 Board Layout



K001

Figure 4. Top Layer Silkscreen

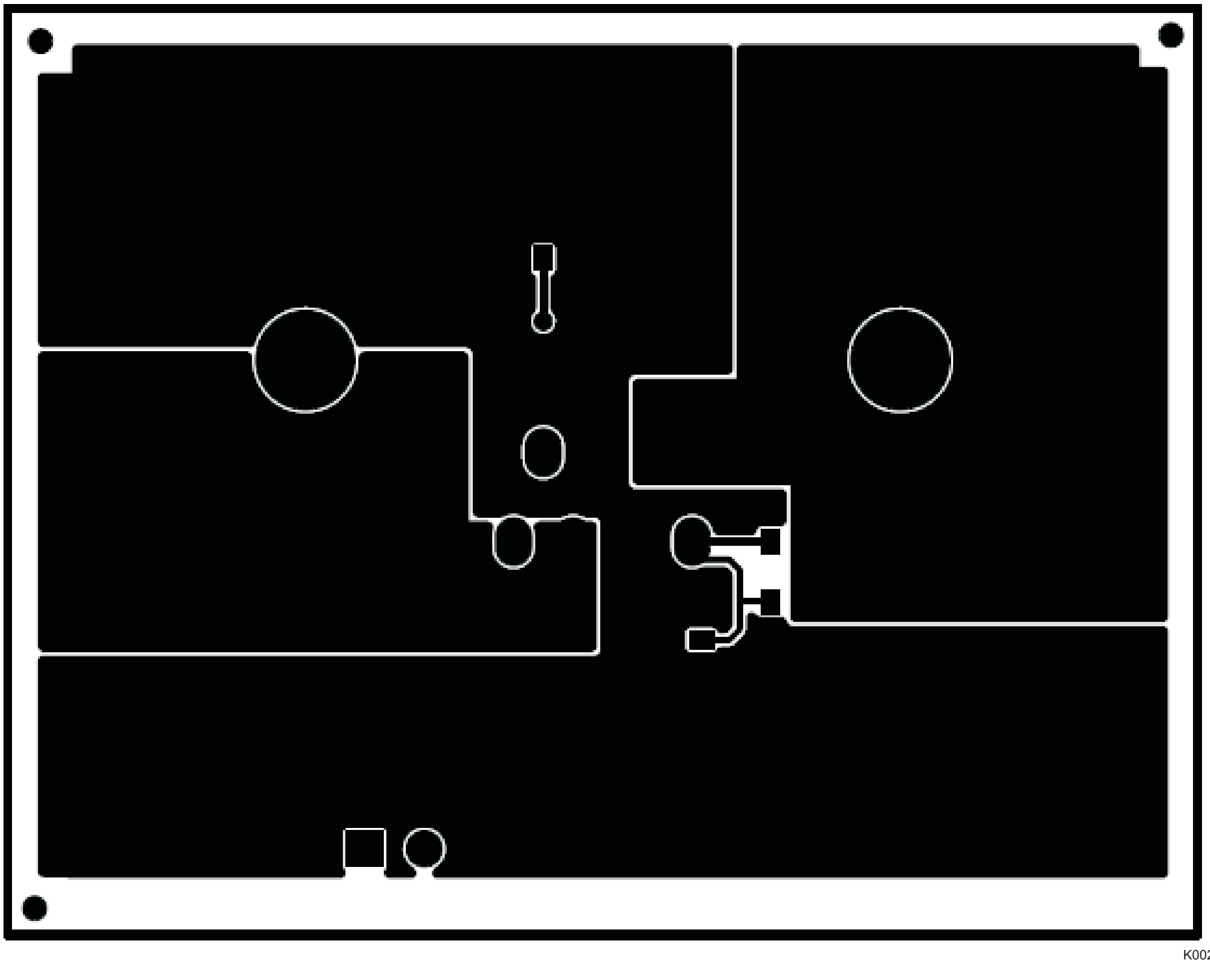


Figure 5. Top Layer Routing

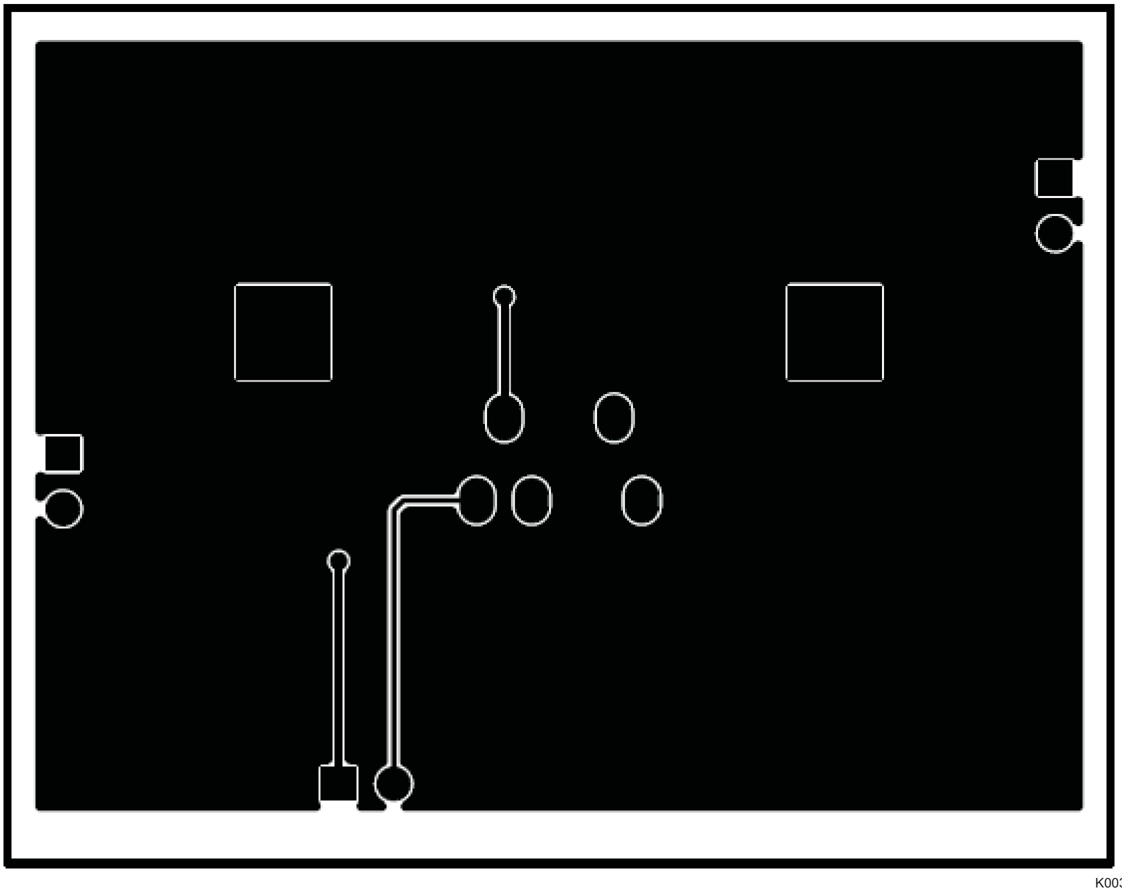


Figure 6. Bottom Layer Routing

8 Schematic and Bill of Materials

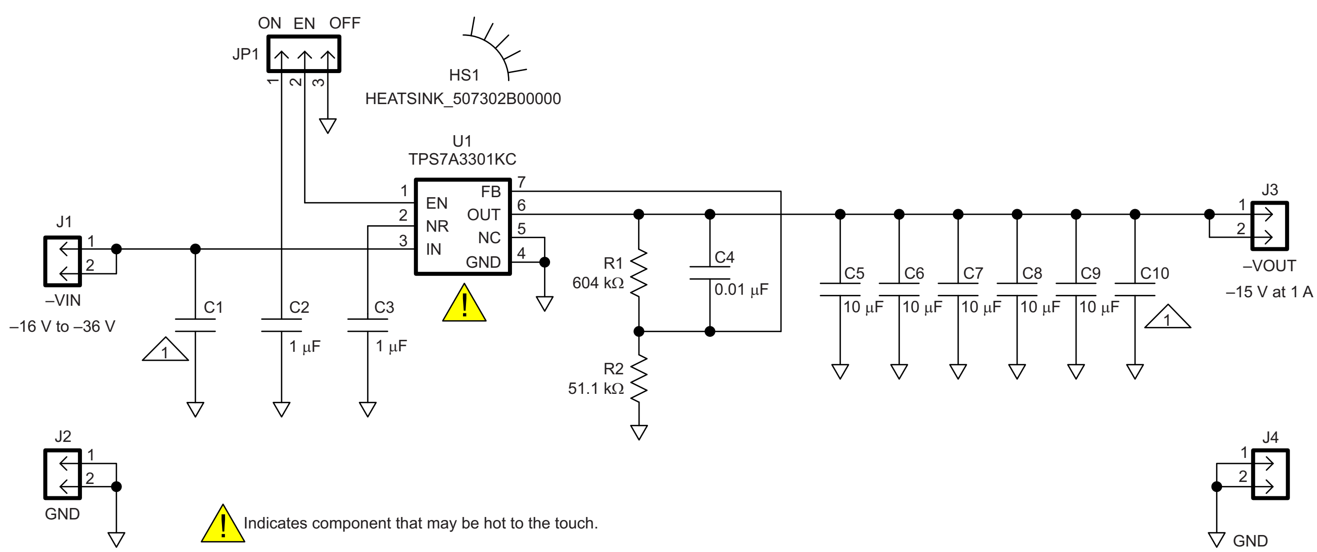


Figure 7. TPS7A3301EVM-061 Schematic

Table 1. TPS7A3301EVM-061 Bill of Materials

RefDes	COUNT	Value	Description	Size	Part Number	MFR
C1	0	47 µF	Capacitor, ceramic, 50 V, X5R, 10%	2220	STD	STD
C2	1	1 µF	Capacitor, ceramic, 50 V, X5R, 10%	0805	STD	STD
C3	1	1 µF	Capacitor, ceramic, 50 V, X5R, 10%	0603	STD	STD
C4	1	0.01 µF	Capacitor, ceramic, 25 V, X5R, 10%	0603	STD	STD
C5–C9	5	10 µF	Capacitor, ceramic, 25 V, X5R, 10%	0805	STD	STD
C10	0	47 µF	Capacitor, ceramic, 16 V, X5R, 10%	2220	STD	STD
HS1	1	13.4°C/W	Heatsink, TO-220, vertical-mount	1 inch × 1.375 inch (2.54 cm × 2.49 cm)	507302B00000G	Aavid
J1–J4	4	PEC02SAAN	Header, male 2-pin, 100-mil (2.54-mm) spacing	0.1 inch (2.54 mm) × 2	PEC02SAAN	Sullins
JP1	1	PEC03SAAN	Header, male 3-pin, 100-mil (2.54-mm) spacing	0.1 inch (2.54 mm) × 3	PEC03SAAN	Sullins
R1	1	604 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
R2	1	51.1 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
U1	1	TPS7A3301KC	IC, –36-V, –1-A, ultralow-noise negative linear regulator	TO-220	TPS7A3301KC	TI
–	1	–	Shunt, black	100 mil (2.54 cm)	929950-00	3M
–	1	–	Screw, hex mach. 4-40 × 1/2 S/S	4-40 × 1/2 S/S	HMSSS 440 0050	STD
–	1	–	Hdwr. mtg. nut, 0.062-inch × 0.184-inch (1.59-mm × 4.67-mm)	0.062 inch × 0.184 inch (1.59 mm × 4.67 mm)	7248-3	STD
–	1	PCB	PCB, 1.555-inch × 2-inch × 0.062-inch (3.95-cm × 5.08-cm × 1.59-mm)	1.5 inch × 2 inch × 0.062 -inch (3.81 cm × 5.08 cm × 1.59 mm)	PWR061	Any

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of –3 V to –36 V and the output voltage range of –1.2 V to –20 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 100 °C. The EVM is designed to operate properly with certain components above 100 °C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265