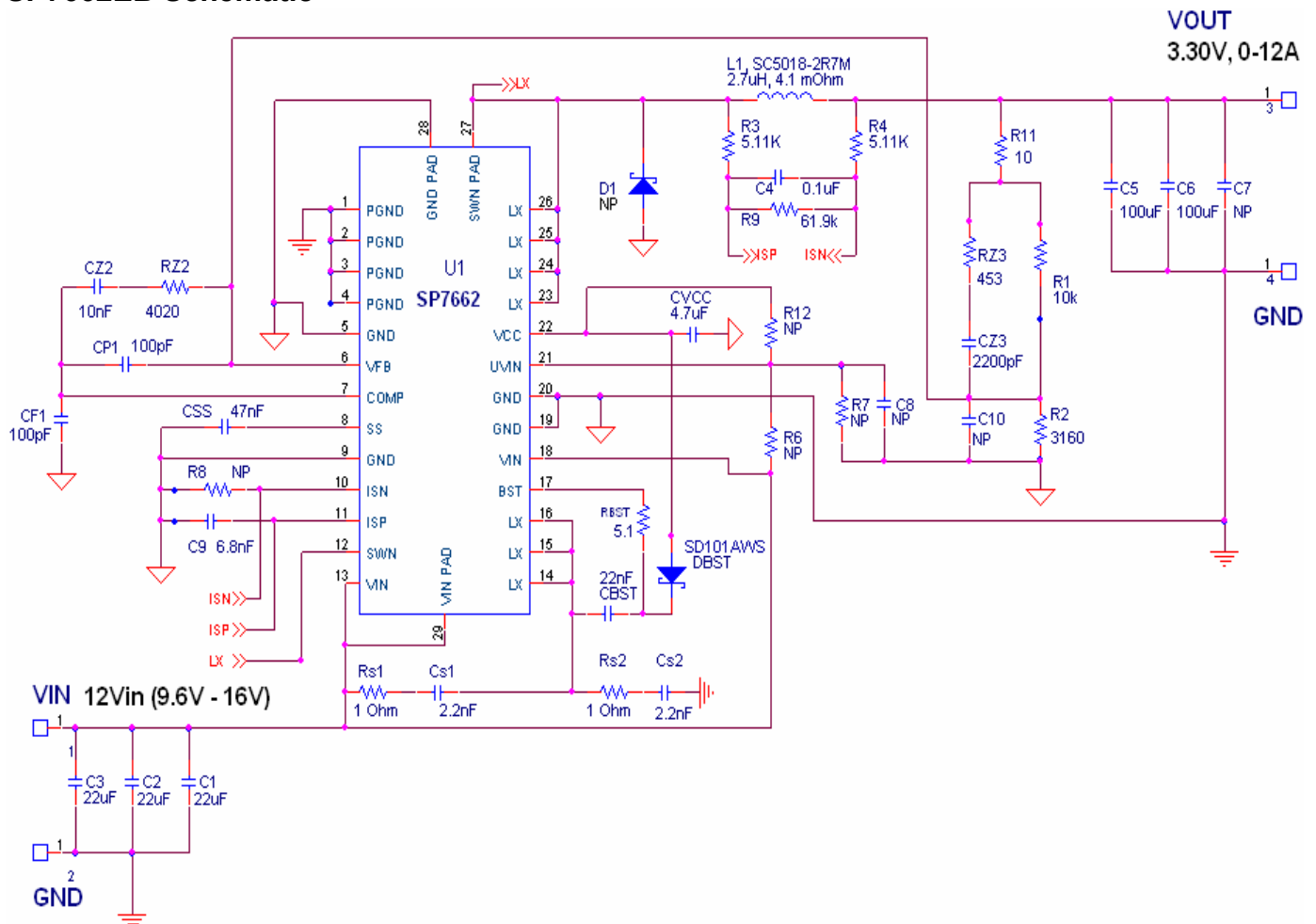


- Easy Evaluation of the SP7662ER 0 to 12A Output Synchronous Buck Converter
- Built in Low RDS(ON) Power FETs
- UVLO Detects Both VCC and VIN
- Highly Integrated Design, Minimal Components
- High Efficiency: up to 93%
- Feature Rich: UVIN, Programmable Soft Start, Built In VCC Supply Output Short Circuit Protection and Current Limiting



SP7662EB Schematic



Using the Evaluation Board

1) Powering Up the SP7662EB Circuit

Connect the SP7662 Evaluation Board with an external +12V power supply. Connect with short leads and large diameter wire directly to the “VIN” and “GND” posts. Connect a Load between the VOUT and GND posts, again using short leads with large diameter wire to minimize inductance and voltage drops. Provide $\geq 100\text{lfm}$ of airflow if powering the evaluation board beyond 10 Amps for extended periods.

2) Measuring Output Load Characteristics

VOUT ripple can best be seen by touching the probe tip to the pad for C5 and the scope GND collar touching the Output GND post – avoid a GND lead on the scope which will increase noise pickup.

3) Using the Evaluation Board with Different Output Voltages

While the SP7662 Evaluation Board has been tested and delivered with the output set to 3.30V, by simply changing one resistor, R2, the SP7662 can be set to other output voltages. The relationship in Equation 1 is based on a voltage divider from the output to the feedback pin V_{FB}, which is set to an internal reference voltage of 0.80V. Note, due to the common mode voltage range of the current sense amplifier, output voltages greater than 3.3V are only possible if the current sense is disabled. To disable current limit, remove R3 and R4. Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$R2 = \frac{R1}{\left[\frac{V_{out}}{.80V} - 1 \right]} \quad \text{Equation 1}$$

Where R1 = 10k Ω and for V_{OUT} = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of the R1 and R2 combination to meet the exact output voltage setting by restricting R1 resistance range such that 10K Ω \leq R1 \leq 100K Ω for overall system loop stability.

Note that since the SP7662 Evaluation Board design was optimized for 12V down conversion to 3.30V, changes of output voltage and/or input voltage will alter performance from the data given in the Power Supply Data section. In addition, the SP7662ER provides short circuit protection by sensing V_{OUT} at GND. The current limit of the converter is set to about 17A which is accomplished by sensing the current through the inductor. To adjust the current limit, follow Equations 2 and 3 to set the current limit accordingly. The current limit should be set to about 50% higher than the maximum output current that is desired. This will prevent the part from accidentally triggering the current limit during large transient load steps.

Adjusting the Current upward is done by adjusting resistor R9.

$$R9 = \frac{60\text{mV} \cdot (R3 + R4)}{I_{max} \cdot (DCR - 60\text{mV})} \quad \text{Equation 2}$$

Where DCR is the Inductor winding resistance
IMAX is the desired output current

Adjusting the Current downward is controlled by adjusting R8.

$$R8 = R4 \cdot \left(\frac{(V_{out} - 60mV) + (I_{max} \cdot DCR)}{60mV - (I_{max} \cdot DCR)} \right) \quad \text{Equation 3}$$

Where DCR is the Inductor winding resistance
 I_{MAX} is the desired output current

Further details on the current limit can be found in the SP7662 data sheet.
 For the Inter-Technical Inductor on this demo board DCR= 4.1mΩ nominal.

POWER SUPPLY DATA

The SP7662ER is designed with an very accurate 2.0% reference over line, load and temperature. Figure 1 data shows a typical SP7662 evaluation board efficiency plot, with efficiencies up to 93% and output currents up to 12A. The output voltage ripple of less than 30mV at full load and the LX node are shown in figure 2. Figures 3 and 4 illustrate a 6A-to-12A and 0A-to-12A Load Step. Short circuit and current limit are shown in Figures 5 and 6. Typical startup characteristics into a full load and no load are shown in figures 7 and 8. All data was taken at 12VIN.

While data on individual power supply boards may vary, the capability of the SP7662ER of achieving high accuracy over a range of load conditions shown here is quite impressive and desirable for accurate power supply design.

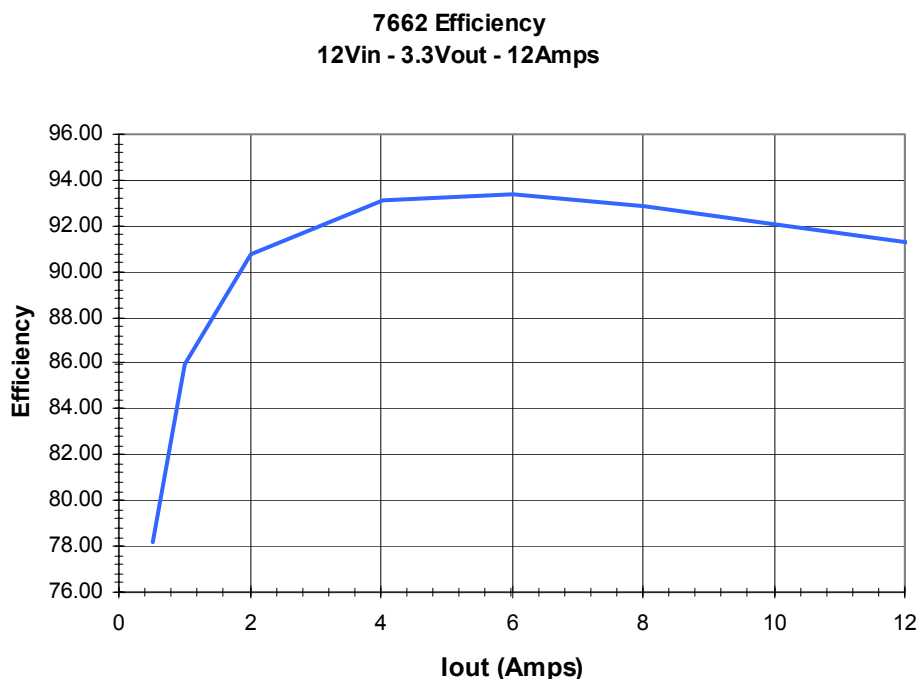


Figure 1. Efficiency vs Load

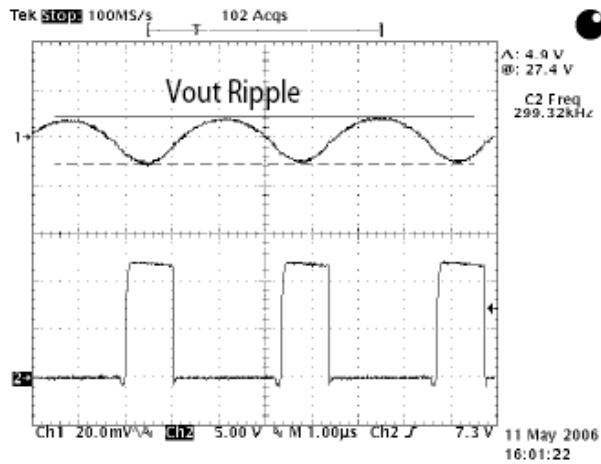


Figure 2. LX node output ripple voltage

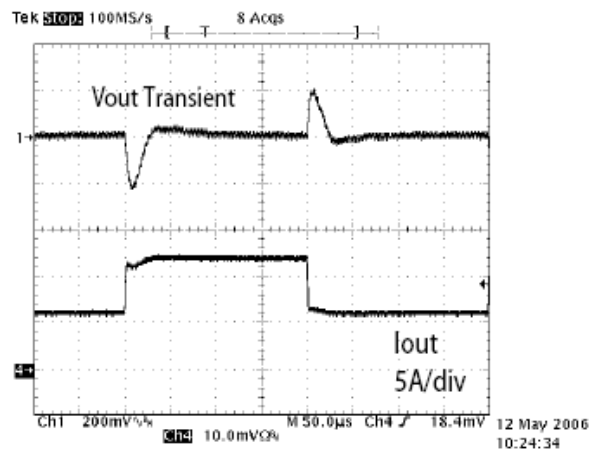


Figure 3. Load Step Response: 6->12A

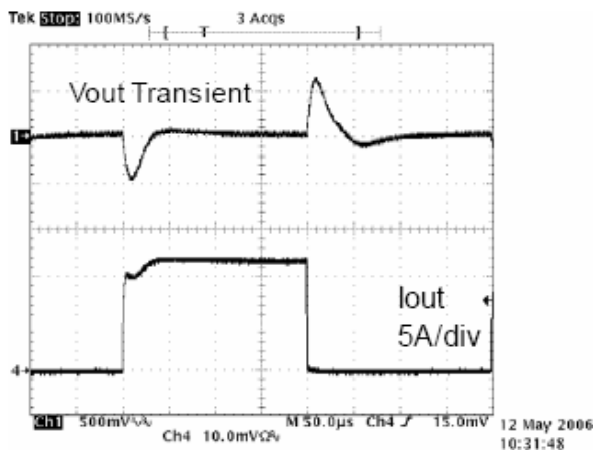


Figure 4. Load Step Response 0->12A

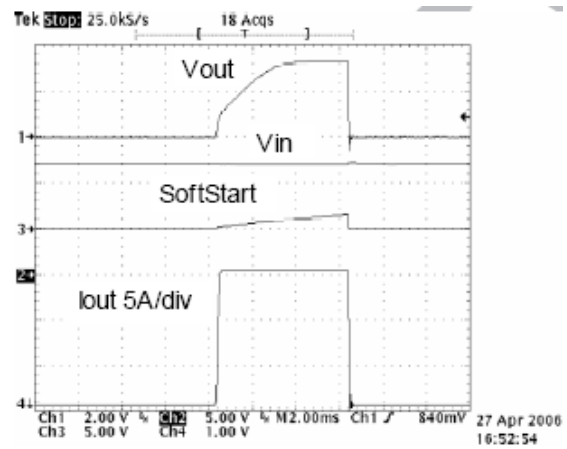


Figure 5. Current limit set point 17A

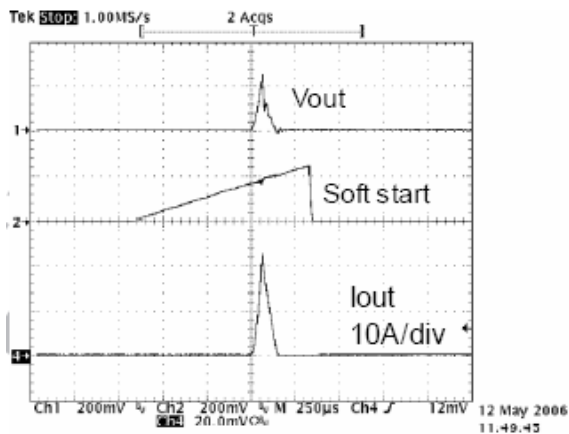


Figure 6. Output load Short Circuit

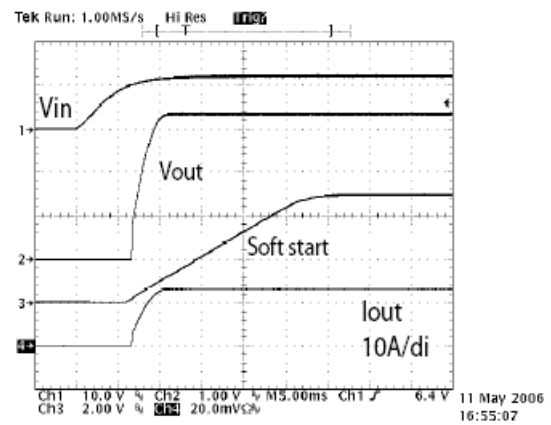


Figure 7. Startup into full load

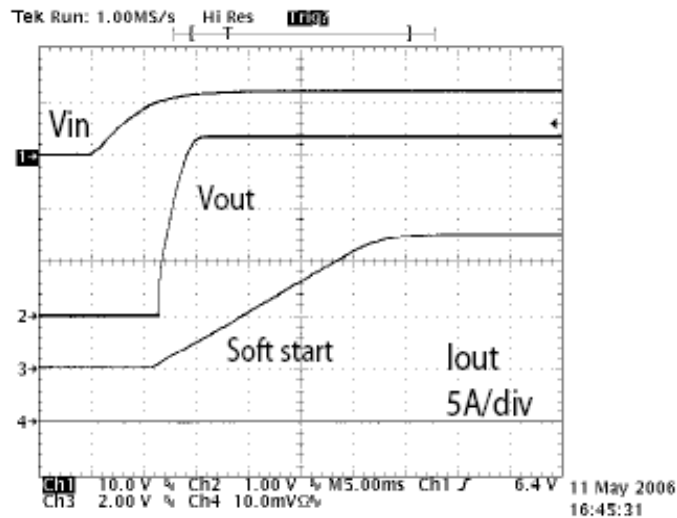


Figure 8. Startup into no load

TYPE III LOOP COMPENSATION DESIGN

The open loop gain of the SP7662EB can be divided into the gain of the error amplifier $G_{amp}(s)$, PWM modulator G_{pwm} , buck converter output stage $G_{out}(s)$, and feedback resistor divider G_{fbk} . In order to cross over at the selecting frequency f_{co} , the gain of the error amplifier must compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate the open loop frequency response such that its gain crosses over 0dB at a slope of -20dB/dec . The open loop crossover frequency should be higher than the ESR zero of the output capacitors but less than $1/5$ to $1/10$ of the switching frequency f_s to insure proper operation. Since the SP7662EB is designed with Ceramic Type output capacitors, a Type III compensation circuit is required to give a phase boost of 180° in order to counteract the effects of the output LC underdamped resonance double pole frequency.

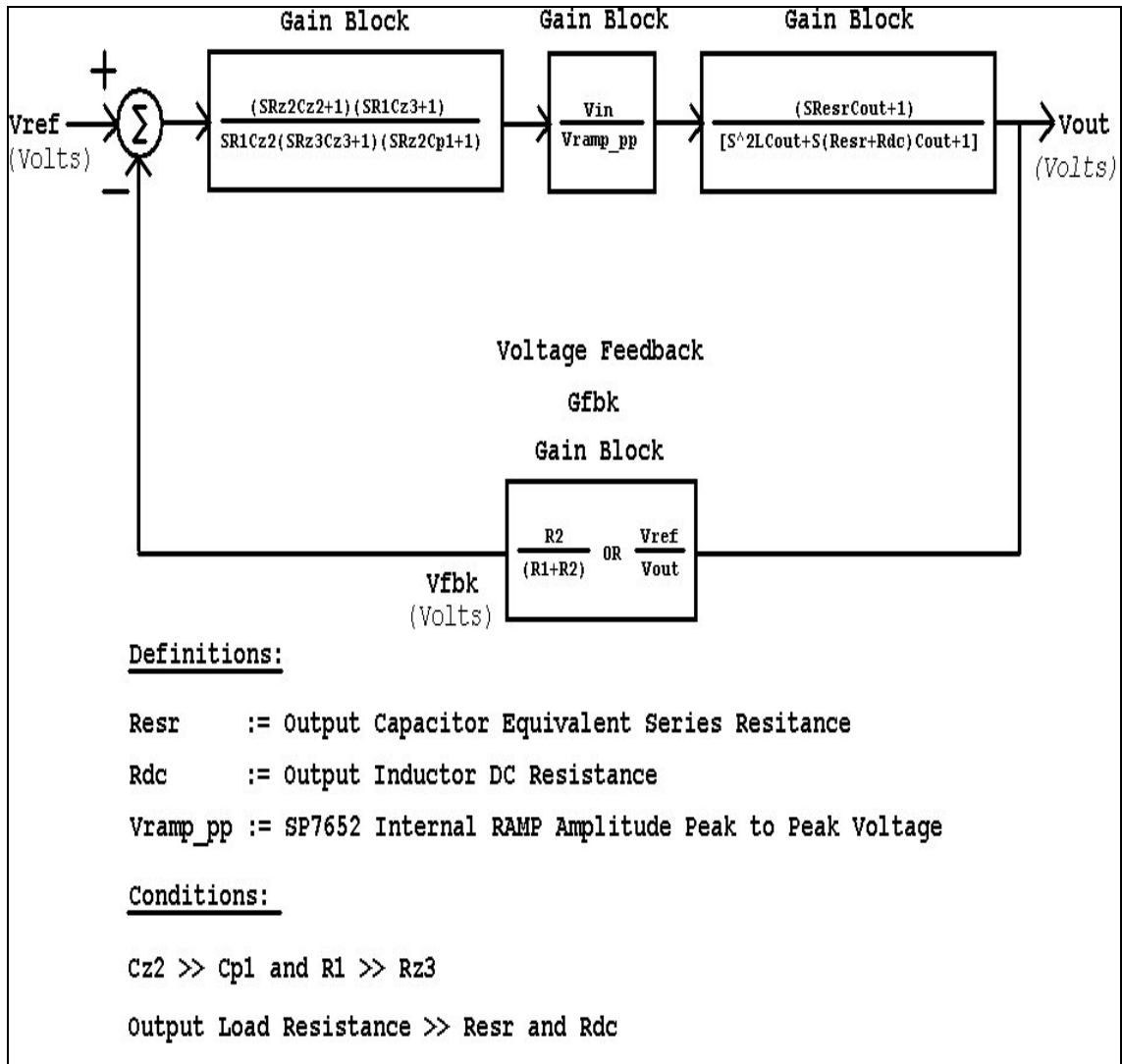


Figure 9. Voltage Mode Control Loop with Loop Dynamic for Type III Compensation

The simple guidelines for positioning the poles and zeros and for calculating the component values for Type III compensation are as follows. As a particular example, consider for the following SP7662EB with a **Type III** Voltage Loop Compensation component selections:

Input requirements and inductor selection

VIN = 12V, we will use 12V as VIN max for this design

VOUT = 3.30V @ 0 to 12A load

Select L = 2.7uH => yield ≈ 25% of maximum 12A output current ripple

Select COUT = 100uF Ceramic capacitor (RESR ≈ 3mΩ)

fs = 300kHz SP7662 internal Oscillator Frequency

VRAMP_PP = 1.0V SP7662 internal Ramp Peak-to-Peak Amplitude

Step by step design procedures:

Note: Loop Compensation component calculations discussed in this section can be quickly iterated with the Type III Loop Compensation Calculator on the web at:

www.sipex.com/files/Application-Notes/TypeIIICalculator.xls

Choose $f_{co} = f_s/10$

$$f_{co} = 300\text{kHz}/10 = 30\text{kHz}$$

Calculate f_{p_LC} the double pole frequency of the filter

$$f_{p_LC} = \frac{1}{2\pi(\sqrt{L \cdot C})}$$

$$f_{p_LC} = \frac{1}{2\pi \cdot \sqrt{2.7\mu\text{H} \cdot 200\mu\text{F}}} = 6852\text{hz} \approx 7\text{kHz}$$

Calculate f_{z_ESR} the ESR zero frequency

$$f_{z_ESR} = \frac{1}{2\pi \cdot C_{esr} \cdot C_{out}}$$

$$f_{z_ESR} = \frac{1}{2\pi \cdot (3\text{m}\Omega / 2) \cdot (200\mu\text{F})} = 530\text{kHz}$$

Select **R1** component value such that $10\text{k}\Omega \leq R1 \leq 100\text{k}\Omega$

R1 = 10k Ω , 1%

Calculate **R2** based on the desired V_{OUT}

$$R2 = \frac{R1}{\left[\frac{V_{out}}{.8V} \right] - 1}$$

$$R2 = \frac{68.1\text{K}\Omega}{\left[\frac{3.3V}{.8V} \right] - 1} = 3200\Omega \approx 3160\Omega$$

Select the ratio of **RZ2 / R1** gain for the desired gain bandwidth (we will use slightly higher than 30kHz @ 33kHz)

$$RZ2 = R1 \cdot \left[\frac{V_{ramp_pp}}{V_{in_max}} \right] \cdot \left(\frac{f_{co}}{fp_LC} \right)$$

$$RZ2 = R1 \cdot \left[\frac{1V}{12V} \right] \cdot \left(\frac{33kHz}{7kHz} \right) = 3928\Omega \cong 4020\Omega$$

Calculate **CZ2** by placing the zero at ½ of the output filter pole frequency

$$CZ2 = \frac{1}{\pi \cdot RZ2 \cdot fp_LC}$$

$$CZ2 = \frac{1}{\pi \cdot 4020\Omega \cdot 7kHz} = 11nF \approx 10nF$$

Calculate **CP1** by placing the first pole at ESR zero frequency

$$CP1 = \frac{1}{2\pi \cdot (Rz2 \cdot fz_ESR)}$$

$$CP1 = \frac{1}{2\pi \cdot (4020 \cdot 530KHz)} = 133pF \approx 100pF$$

Calculate **RZ3** by setting the second pole at ½ of the switching frequency and the second zero at the output filter double pole frequency

$$RZ3 = \frac{2 \cdot (R1) \cdot (fp_LC)}{fs - 2fp_LC}$$

$$RZ3 = \frac{2 \cdot (10k\Omega) \cdot (7kHz)}{300KHz - 2 \cdot 7kHz} = 489\Omega \cong 453\Omega$$

Calculate **CZ3** from **RZ3** component value above

$$CZ3 = \frac{1}{\pi \cdot RZ3 \cdot fs}$$

$$CZ3 = \frac{1}{\pi \cdot 453\Omega \cdot 300KHz} = 2.3nF \approx 2200pF$$

Choose $100pF \leq \mathbf{CF1} \leq 220pF$ to stabilize the SP7662ER internal Error Amplifier . For this example let's select 100pF.

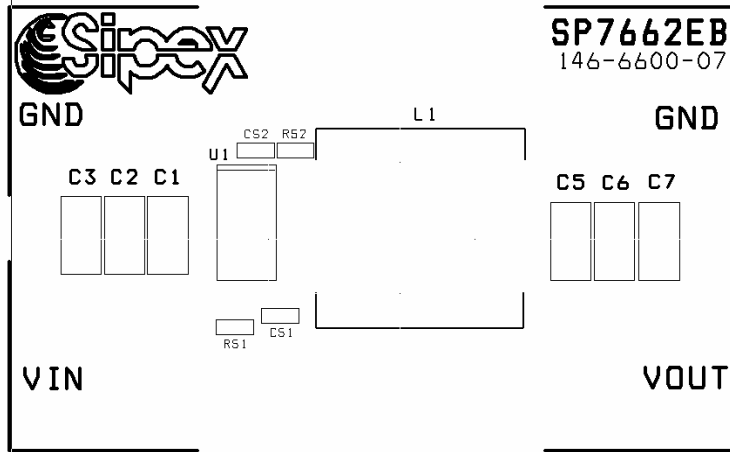


Figure 15. SP7662EB Component Placement

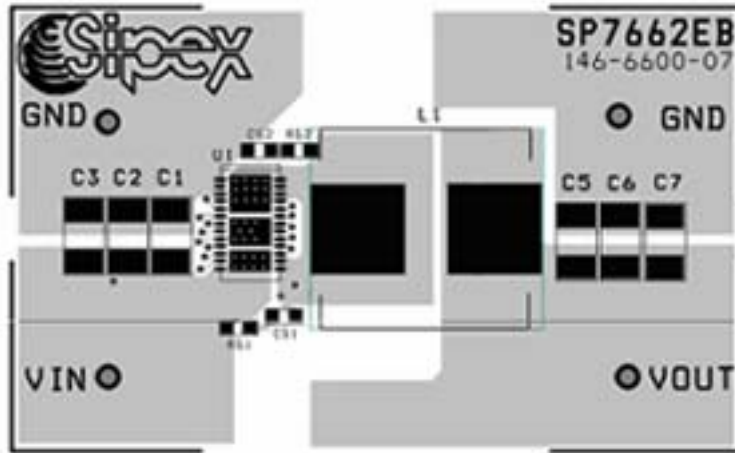


Figure 16. SP7662EB PC Layout Top Side



Figure 17. SP7662EB PC Layout 2nd Layer Side

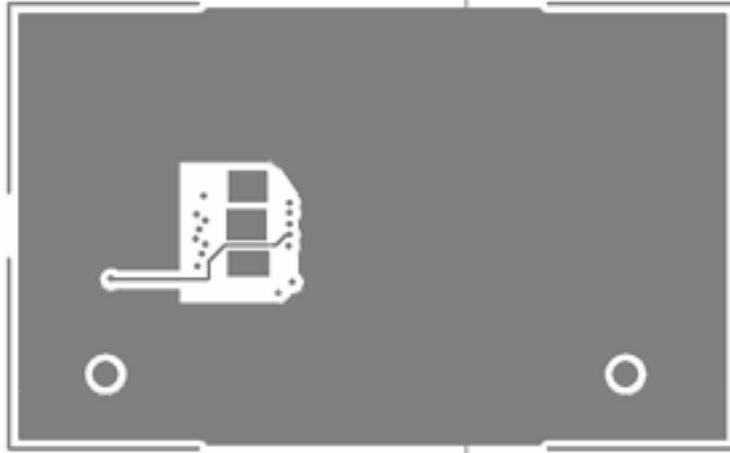


Figure 18. SP7662EB PC Layout 3rd Layer Side

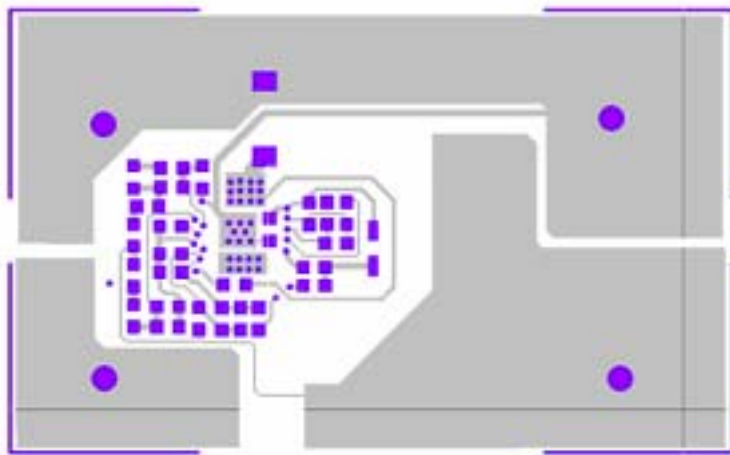


Figure 19. SP7662EB PC Layout Bottom Side

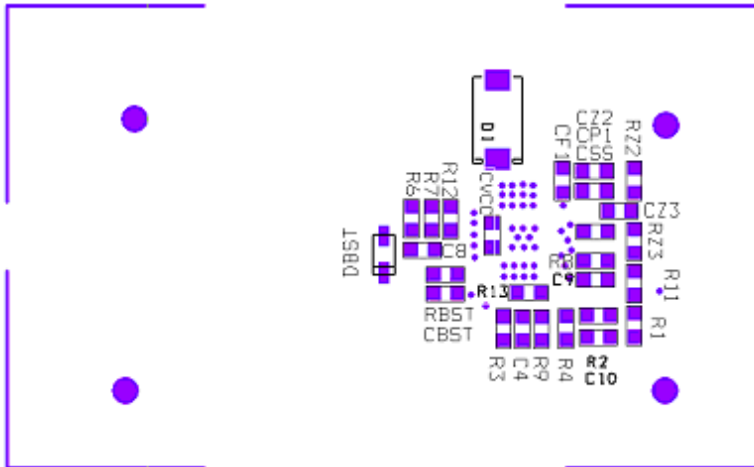


Figure 20. SP7662EB PC Layout Bottom Side Components

7662		12Vin 3V3out					
Line No.	Ref. Des.	Qty.	Manufacturer	Manuf. Part Number	Layout Size	Component	Vendor Phone #
1	PCB	1	Sipex	146-6600-07		SP7662EB	978-667-8700
2	U1	1	Sipex	SP7662EU	DFN-26	Synchronous Buck Regulator	978-667-8700
3	DBST	1	Vishay Semi	SD101AWS	SOD-323	15mA-30V Schottky Diode	800-344-4539
4	L1	1	Itechnical	SC5018-2R7	5050	2.7uH Coil, 15A, 4.1mOhm	860-974-2735
4b	L1	0	Würth	744318270	5050	2.7uH Coil, 20A, 4.0mOhm	201-785-8800
5	C1, C2, C3	3	Murata	GRM32ER61C226KE20L	1210	22uF Ceramic X5R 16V	770-436-1300
6	C5, C6	2	Murata	GRM32ER60J107ME20L	1210	100uF Ceramic X5R 6.3V	770-436-1300
7	C4,	1	Murata	GRM188R71H104KA93D	0603	0.1uF Ceramic X7R 50V	770-436-1300
8	CBST	1	Murata	GRM188R71H223KA01D	0603	22nF Ceramic X7R 50V	770-436-1300
9	C9	1	Murata	GRM188R71H682KA01D	0603	6.8nF Ceramic X7R 50V	770-436-1300
10	CVCC	1	TAIYO YUDEN	LMK107BJ75KA-B	0603	4.7uF Ceramic X5R 10V	800-388-2496
11	CF1	1	Murata	GRM1885C1H101JA01D	0603	100pF Ceramic C0G 50V	770-436-1300
12	Cs1, Cs2	2	Murata	GRM1885C1H222JA01D	0603	2.2nF Ceramic C0G 50V	770-436-1300
13	CSS1	1	Murata	GRM188R71H473KA61D	0603	47nF Ceramic X7R 50V	770-436-1300
14	CP1	1	Murata	GRM1885C1H101JA01D	0603	100pF Ceramic C0G 50V	770-436-1300
15	CZ2	1	TDK	C1608CH1H103J	0603	10nF Ceramic C0G 50V	978-779-3111
16	CZ3	1	Murata	GRM1885C1H222JA01D	0603	2200pF Ceramic C0G 50V	770-436-1300
17	R1	1	Panasonic	ERJ-3EKF1002V	0603	10k Ohm Thick Film Res 1%	800-344-4539
18	R2	1	Panasonic	ERJ-3EKF3161V	0603	3160 Ohm Thick Film Res 1%	800-344-4539
19	R3, R4	2	Panasonic	ERJ-3EKF4991V	0603	5.11k Ohm Thick Film Res 1%	800-344-4539
20	R9	1	Panasonic	ERJ-3EKF6192V	0603	61.9k Ohm Thick Film Res 1%	800-344-4539
21	R11	1	Panasonic	ERJ-3GEYJ10RV	0603	10 Ohm Thick Film Res 1%	800-344-4539
22	RBST	1	Panasonic	ERJ-3GEYJ00R1V	0603	0 Ohm Thick Film Res 1%	800-344-4539
23	Rs1, Rs2	2	Panasonic	ERJ-3GEYJ2R0V	0603	1 Ohm Thick Film Res 1%	800-344-4539
24	RZ2	1	Panasonic	ERJ-3EKF4021V	0603	4020 Ohm Thick Film Res 1%	800-344-4539
25	RZ3	1	Panasonic	ERJ-3EKF4530V	0603	453 Ohm Thick Film Res 1%	800-344-4539
26	VIN, VOUT, GND, GND	4	Vector Electronic	K24C/M	.042 Dia	Test Point Post	800-344-4539

Table 1: SP7662EB Suggested Components and Vendor Lists

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP7662EB.....	-40°C to +85°C.....	SP7662 Evaluation Board
SP7662ER.....	-40°C to +85°C.....	26-pin DFN(option2)