FAIRCHILD
SEMICONDUCTOR®

AN9689
EVALUATION BOARD
APPLICATION NOTE

FEATURES

- Dual Ultra-fast Voltage Comparator
- SMA Connectors for All Nonpower Signals
- Adjustable Voltage on $\overline{LE}$ for Hysteresis

APPLICATIONS

- Evaluation of the SPT9689 Comparator
- Engineering Prototype
- Aid Guide to PCB Layout
- Guide for Design With the SPT9689

GENERAL DESCRIPTION

The EB9689 evaluation board is intended as a tool for device evaluation and characterization and to demonstrate the performance of the SPT9689 (dual ultra-fast voltage comparator). The device-under-test will accept input voltages between -2.5 and +4.0 V (at ±INA and ±INB), input common mode voltage. The output signals are pulled down to the VPD voltage via 100 Ω resistors and the parallel combination of the 50 Ω series resistors and the measuring instrument's input impedance. The latch signals may be driven dynamically using the SMA connectors or statically by applying a DC voltage to the LE pin and setting the voltage on the $\overline{LE}$ pin.

This application note describes in detail the following functional blocks of the evaluation board: power supplies and grounding, inputs, outputs, latches and layout.

BLOCK DIAGRAM

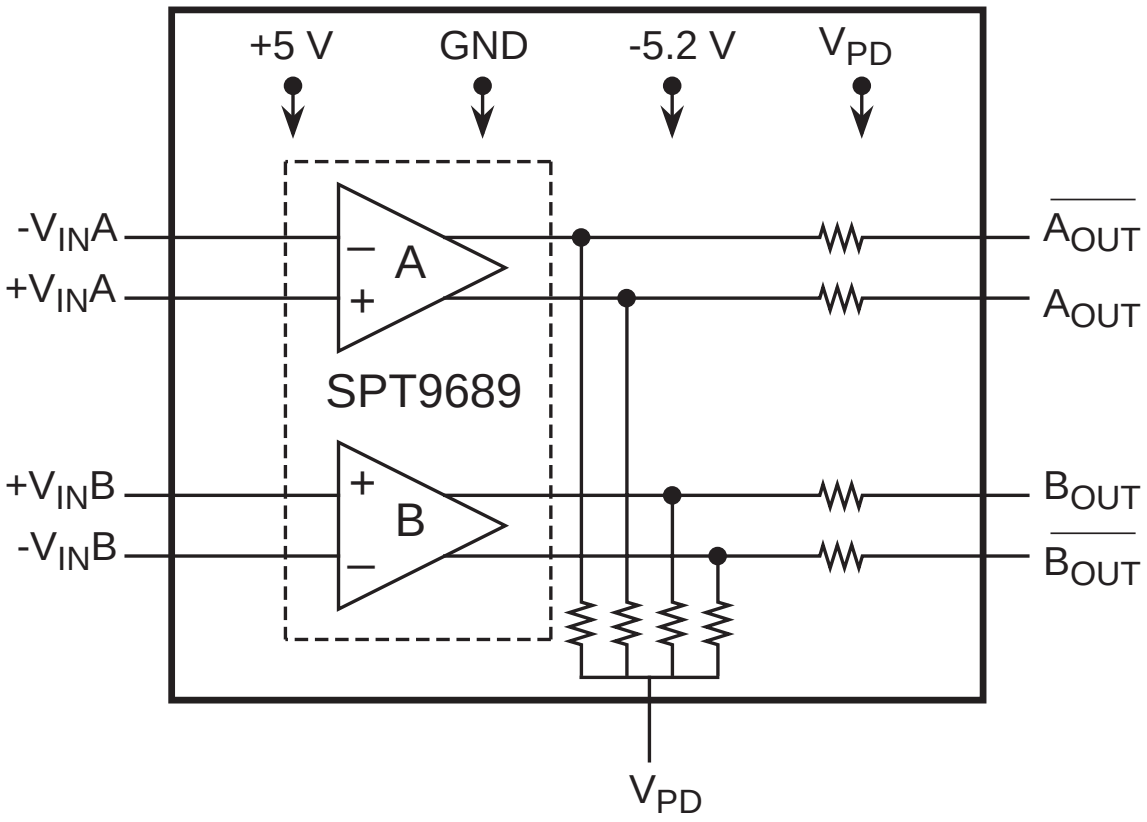
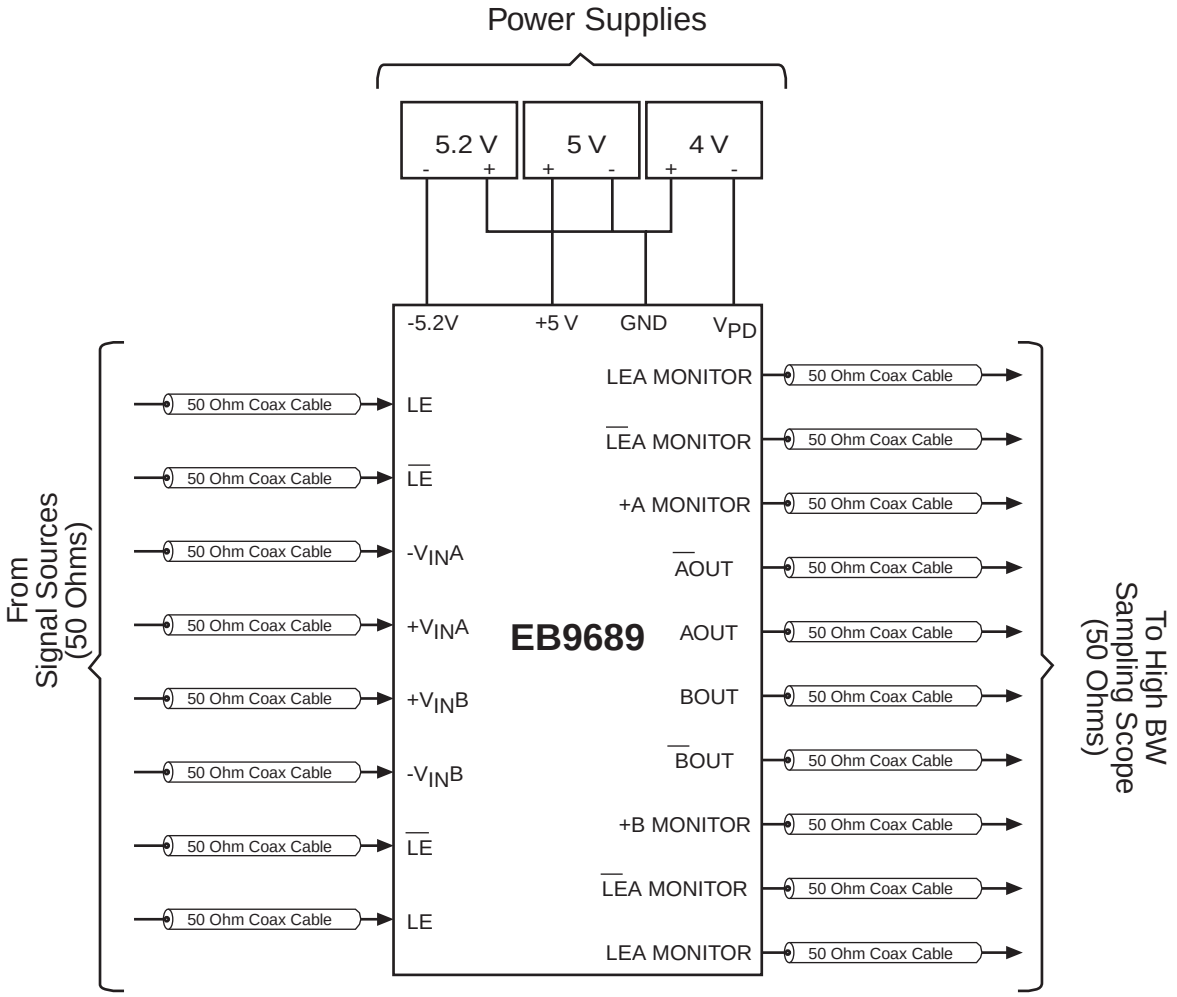


Figure 1 - Block Diagram of Typical Setup



POWER SUPPLIES AND GROUNDING

The EB9689 is powered by +5 V, -5.2 V and VPD (pulldown voltage) supplies. The +5 V and -5.2 V supplies power the SPT9689 only. The VPD supply is used for powering the pulldown resistors at the outputs and for biasing the $\overline{LE}$ pins when using hysteresis or static track mode conditions. VPD should be -4.0 V when using the board in the factory configuration. A ferrite bead is used to isolate the VPD voltage used at the outputs and the VPD voltage used on the $\overline{LE}$ pins. Adequate isolation filtering and decoupling of the power supplies have been incorporated into the design. However, use of low-noise (nonswitching), regulated and low source impedance supplies is recommended. Figure 1 shows a diagram of the power and ground connections.

This device has inputs that are analog in nature, however, there is not a split in the ground plane nor is one recommended.

INPUTS

The SPT9689 has a common mode input voltage range of -2.5 to +4.0 V. A dynamic input signal is typically applied to the +VINA or +VINB SMA connection on the EB9689. Two additional connections are provided for viewing the input signal relative to the output signals. These are +A_MONITOR and +B_ MONITOR. The input impedance of the monitoring instrument should be 50 ohms so that the equivalent input impedance as seen from the +VIN SMA will be 50 Ω.

The -VINA and -VINB SMA connections are used as reference inputs to the comparator. If the input signal applied to the +VIN connection is zero crossing, use a screw-on type SMA 50 Ω termination resistor to hold the -VIN pin at ground. For nonzero crossing input voltages, apply a DC voltage within the common mode voltage range for the device.

OUTPUTS

The Q and $\overline{Q}$ outputs are terminated on-board through 100 Ω to VPD. A 50 Ω resistor is in series with the output. The outputs are intended to be connected to a scope with a 50 Ω input impedance. Use SMA connectors for the outputs.

LATCHES

Latches LE and $\overline{LE}$ can be configures in four ways:

1) *Driving the latches dynamically and monitoring them with a 50 Ω input impedance scope.* This is done by connecting a 50 Ω driving source to the LE and $\overline{LE}$ SMA connectors. Connect a 50 Ω measuring device to the monitor lines and connect a 50 Ω terminating resistor to any unused monitor line. Ensure that the jumper plug on J21 (A-side) or J23 (B-side) is not installed.

2) *Driving the latches dynamically without using the monitor lines.* In this case connect screw-on type 50 Ω terminators on the latch monitor SMA connectors. Another option is to replace R15 and R16 (A-side) and R19 and R20 (B-side) with 50 Ω resistors, which eliminates the need for the screw-on type terminators. In either case the object is to maintain a 50 Ω equivalent termination. Ensure that the jumper plug on J21 (A-side) or J23 (B-side) is not installed.

3) *Operating the device in track mode without use of external latch signals.* This can be done by not applying any signals to the latches or the latch monitor lines. Install the jumper plug on J21 (A-side) and J23 (B-side) to provide a voltage to the $\overline{LE}$ pin. Adjust the $\overline{LE}$ voltage to an ECL low. The LE pin will be at ground which is within the device's Latch Enable Common Mode Range.

4) *Setting up the latches for hysteresis.* This can be done by applying a voltage to the LE pin nominally around -1.3 V. Install the jumper plug on J21 (A-side) and J23 (B-side) to provide a voltage to the $\overline{LE}$ pin. Adjust this voltage (using R17 for the A-side and R22 for the B-side) to be around -1.3 V also. The largest hysteresis will be when the difference between the latch pins (LE and $\overline{LE}$) is zero.

LAYOUT

Careful consideration of the layout of this evaluation board was performed by Fairchild to ensure maximum performance for the part and to aid users in evaluating this device. Some highlights of the EB9689 layout are as follows:

Controlled impedance signal traces and associated termination of signals are a must when operating this device. This is necessary to minimize energy reflections present on signals with very high slew rates. Input termination resistors are placed close to the device as are the power supply decoupling capacitors.

Line lengths for the Input and Latch monitor lines and the outputs are matched to eliminate the concern over skew between signals.

The EB9689 was built with four layers:

- First layer 50 Ω controlled impedance signal
- Second layer GND
- Third layer Powers (+5 V, -5.2 V and VPD)
- Fourthlayer Signal

SETUP AND PERFORMANCE CHECK

NOTE: Before connecting the power supplies, verify that all power sources are set to the correct voltages.

Perform the following steps:

1. Set the +5 V power supply to +5.00 V ±0.05 V. Set the -5.2 V supply to within 50 mV. Turn the power supplies off and connect to the EB9689. Note: Specifications for this device are +5 V ± 0.25 V and -5.2 V ± 0.25 V

2. Set the VPD supply to -4 V ±50 mV. Turn the power supply off and connect to the EB9689.

3. Install the jumper plugs on J21 and J23.

4. Connect the outputs to the 50 Ω input of a scope or add a 50 Ω termination resistor on any unconnected output.

5. Add screw-on type 50 Ω termination resistors to the -VINA and -VINB SMA connections.

6. Turn on the power supplies.

7. Adjust the $\overline{LE}$ pins to -1.8 V using R17 for the A-side and R22 for the B-side.

8. Connect the input signals to the +VIN pins.

9. Observe the output pins; they should track the signal that is switching at the input.

10. This concludes initial setup and operational check.

Figure 3 - Detailed Schematic, Rev. A Board

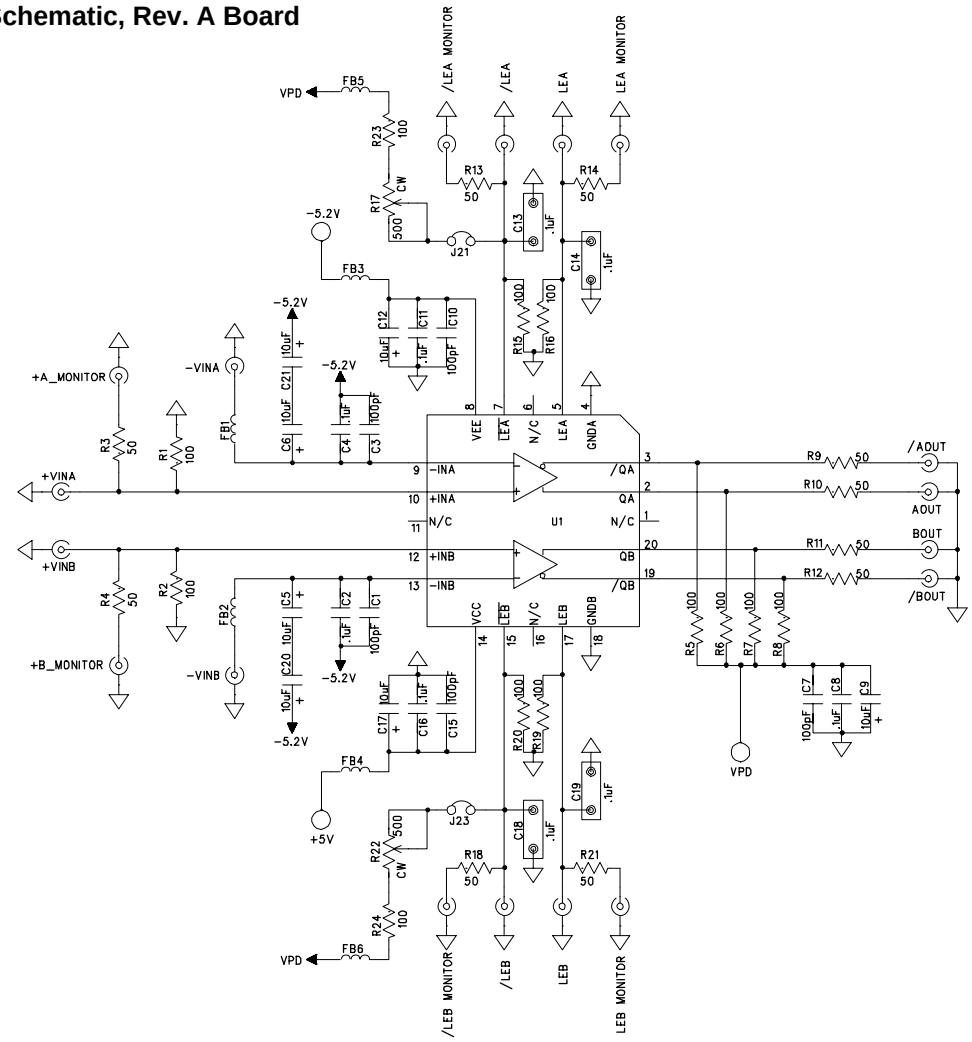


Table I - Bill of Materials

No.	Reference	Part Number	Description	Qty	Manufacturer
1	C1,3,7,10,15	ECU-V1H101JCH	100 pF Chip Capacitor	5	Panasonic/Any
2	C2,4,8,11,16	ECUV1H104KBW	.1 µF Chip Capacitor	5	Panasonic/Any
3	C5,6,20,21	ECS-T1CX106R	10 µF Tantalum Chip Capacitor (Per Assy Dwg)	4	Panasonic/Any
	C9,12,17		10 µF Tantalum Chip Capacitor (As per Board)	3	
4	C13,14,18,19	ECQ-V1H104JL	.1 µF 5% Radial Capacitor	4	Panasonic/Any
5	FB1-6	EXC-ELSA35	Ferrite Bead	6	Panasonic
6	J1-18	901-144-8	SMA Coax Connector	18	Amphenol
7	J19,20,22	108-740-001	Banana Jack	4	Johnson
8	J21,23	PZC36SAAN	Jumper, 2-Pin	1	Sullins
9	R1,2,5-8,15,16, 19,20,23,24	ERJ-8ENF1000	100 Ohm Chip Resistor	12	Panasonic/Any
10	R3,4,9-14,18,21	ERJ-8ENF49R9	49.9 Ohm Chip Resistor	10	Panasonic/Any
11	R17,22	3266-1-501	500 Ohm Variable Resistor	2	Bourns
12	U1	SPT9689/LCC	Dual Sub-ns Volt Comparator	2	Fairchild
13	N/A	929955-06	Shunt for Jumper	2	DIGI-KEY (3M)
14	N/A	ED5044-ND	Pin Receptacle	8	DIGI-KEY
15	N/A	1902EK-ND	1” Nylon Spacer	4	DIGI-KEY
16	N/A	H143-ND	4-40 Pan-head Screw	4	DIGI-KEY
17	EB9689	Rev A	Evaluation Board	1	SAS Circuits

Figure 4 - Component Side

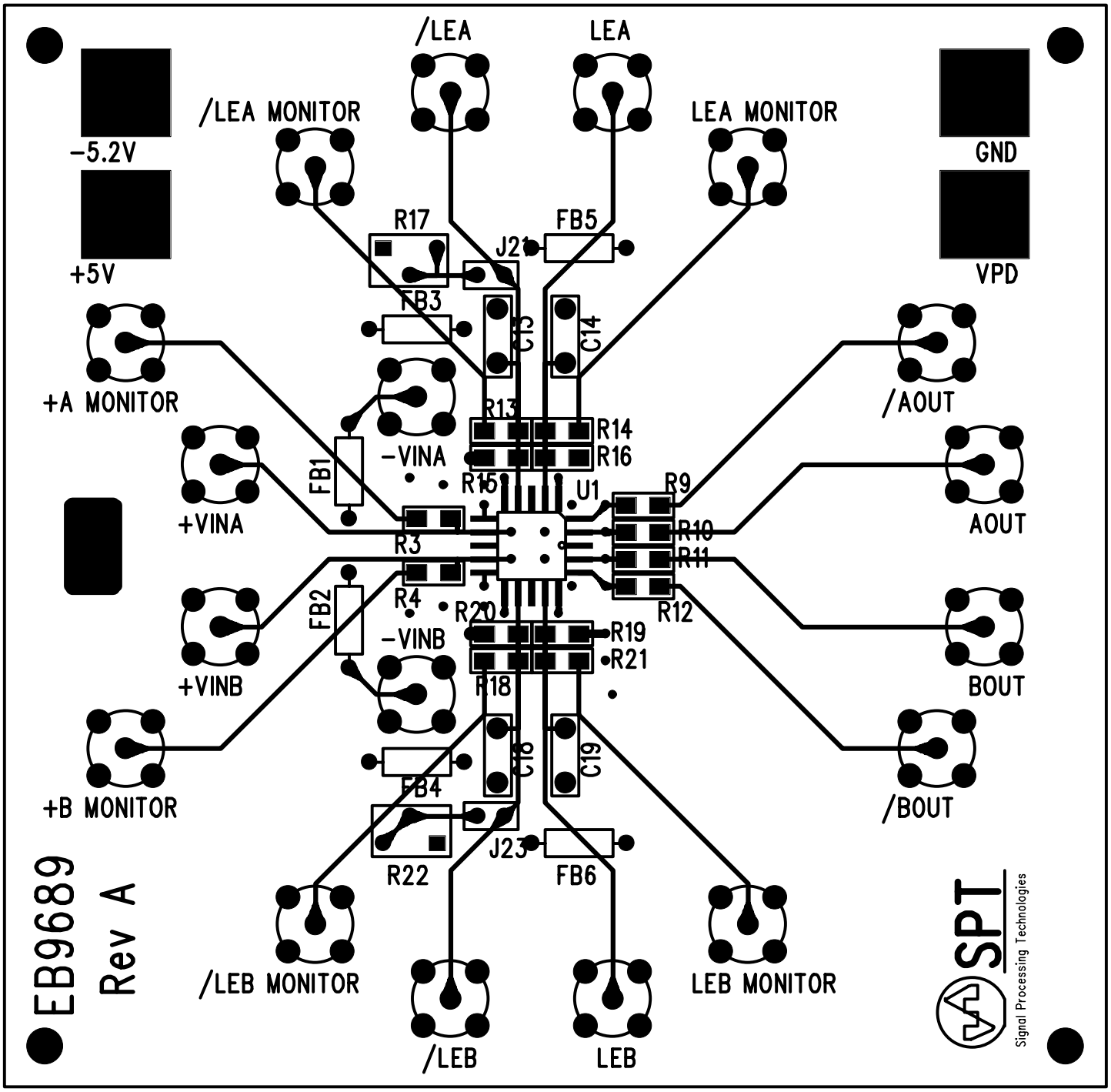


Figure 5 - Ground Layer

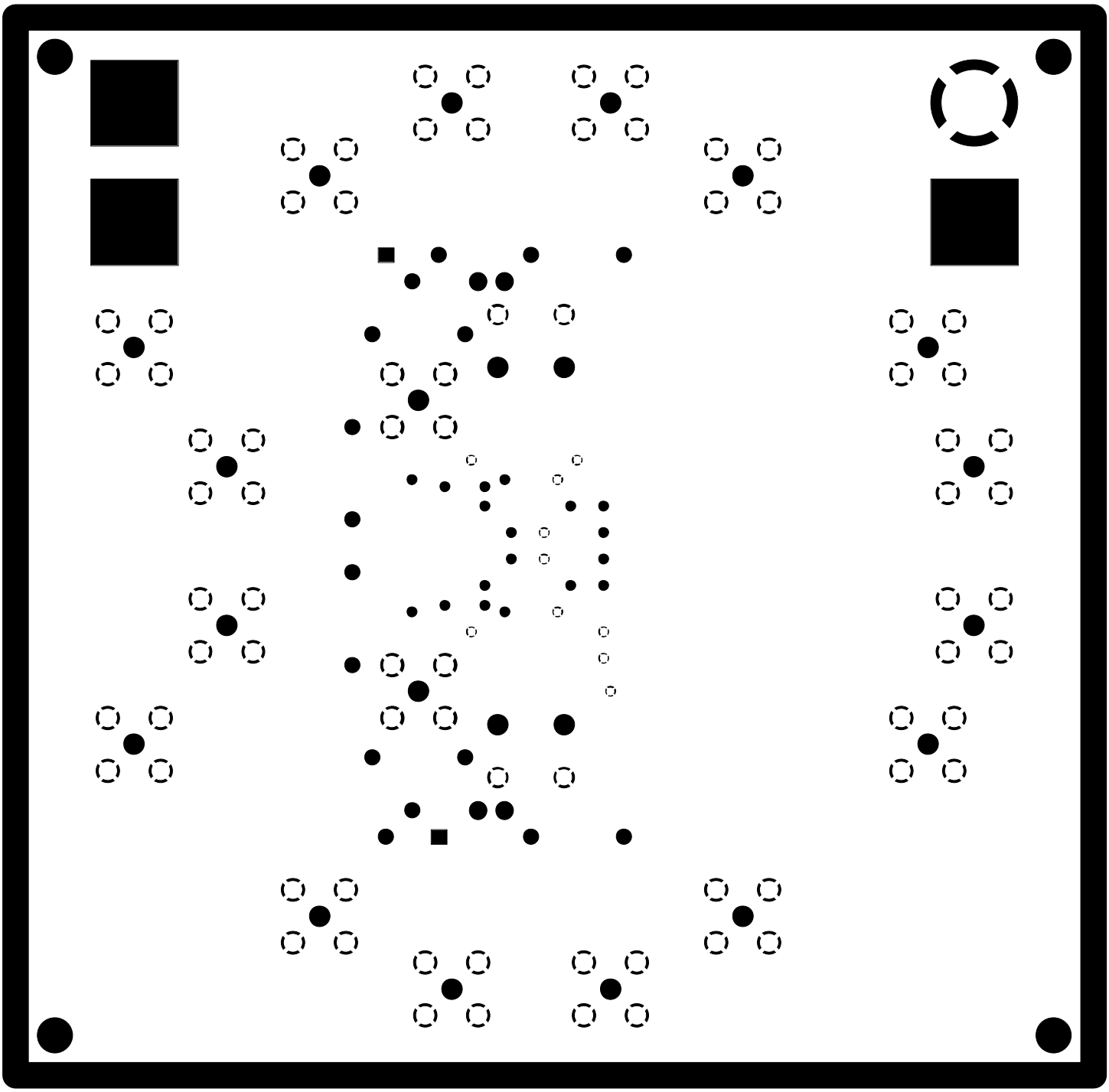


Figure 6 - Power Layer

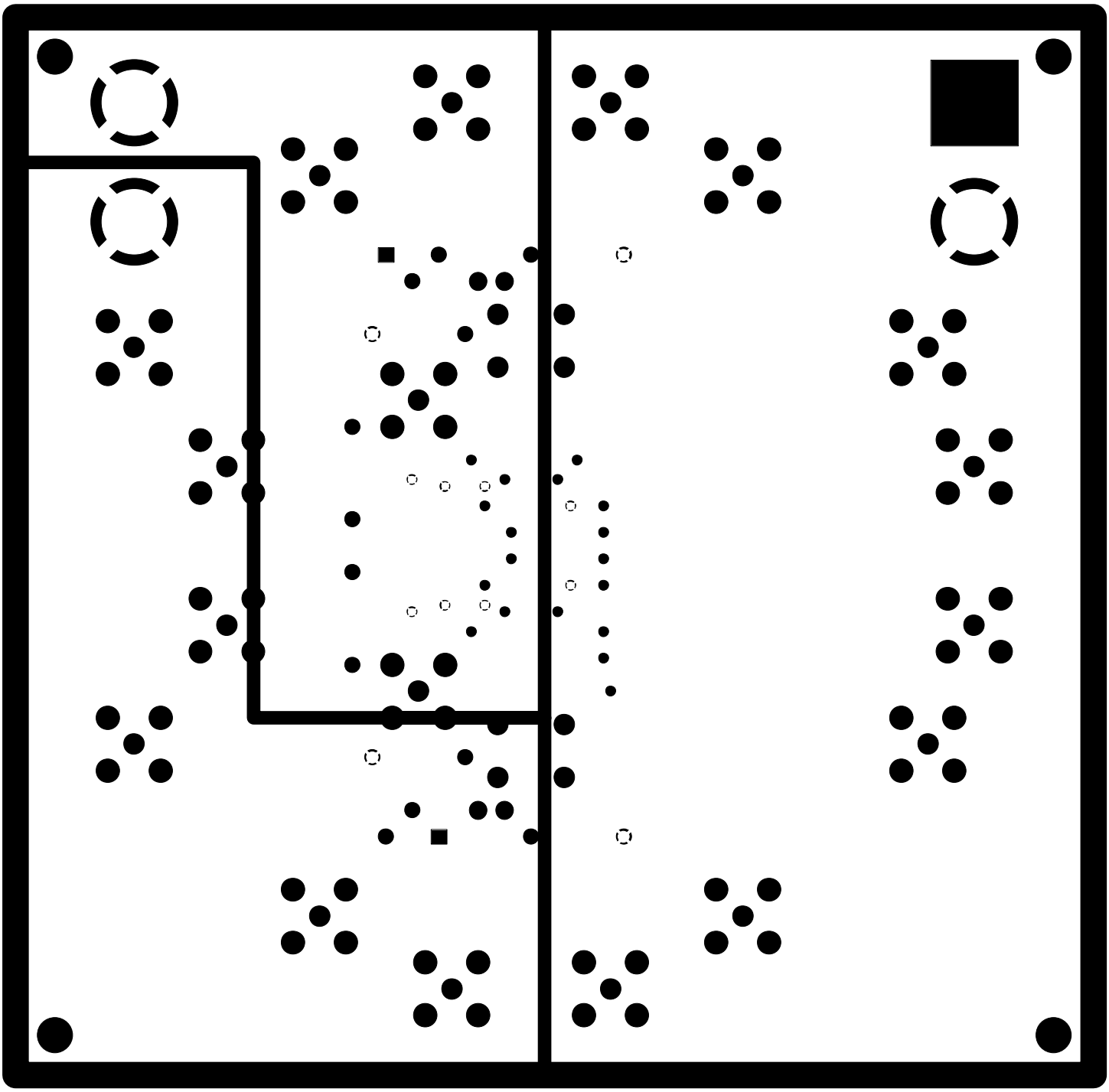
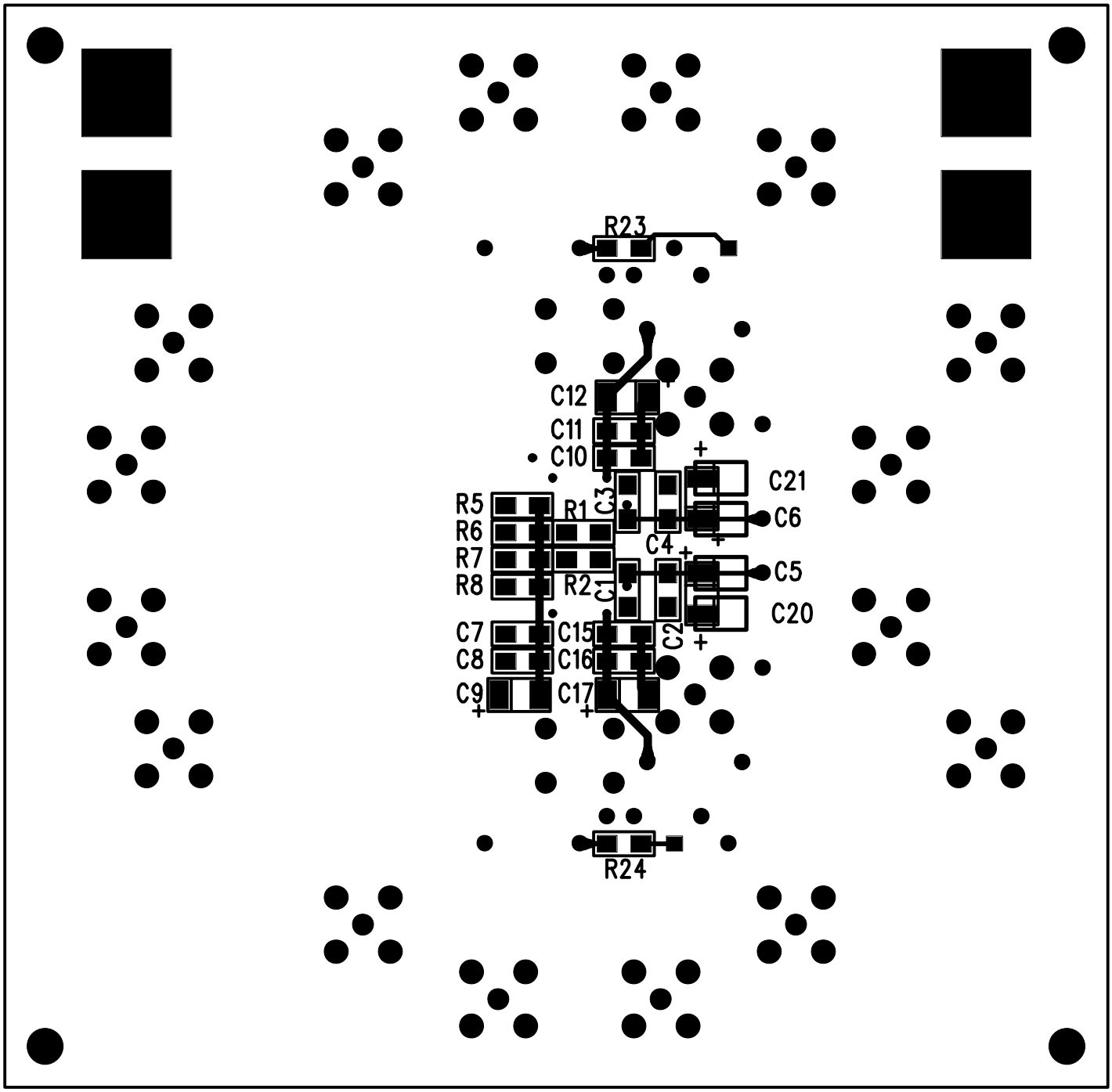


Figure 7 - Solder Side



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