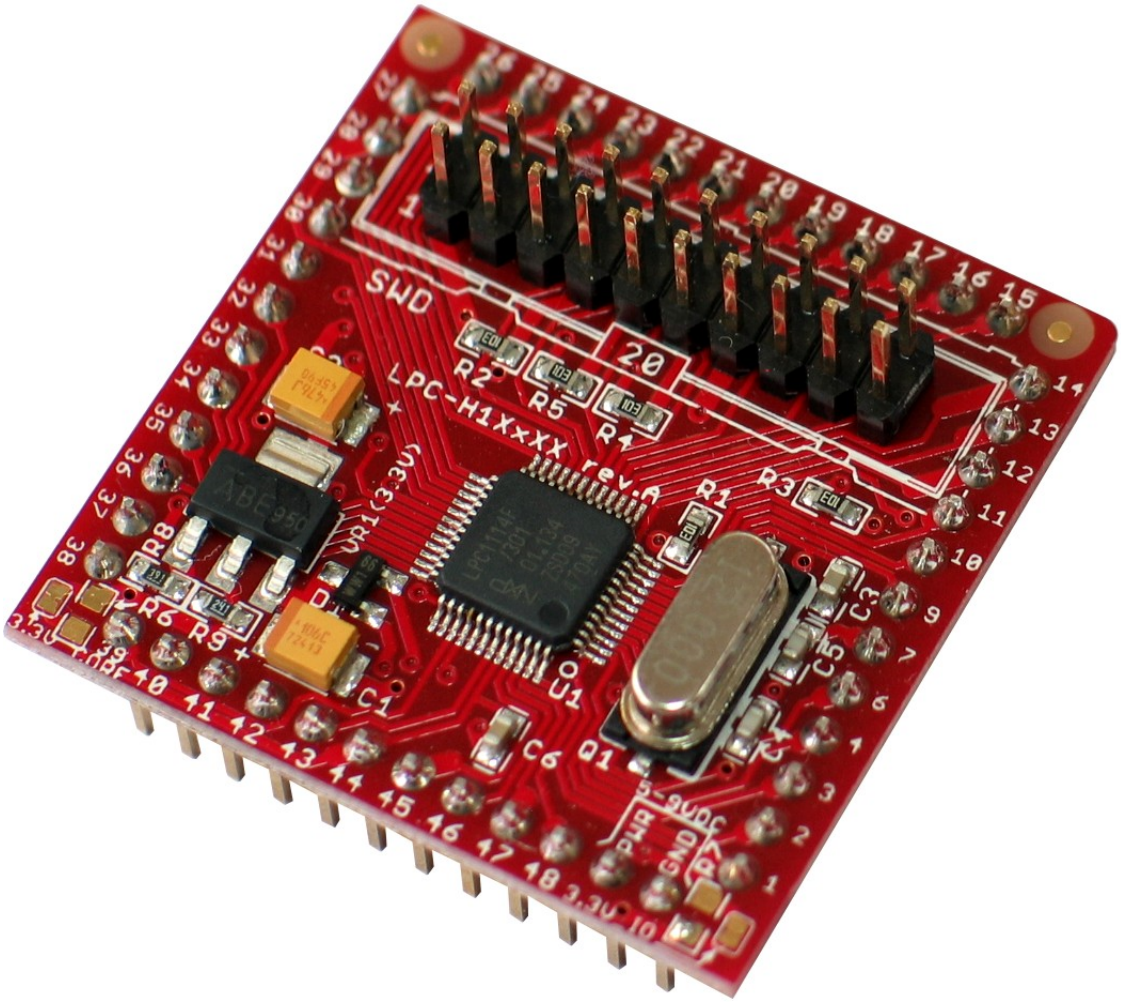


LPC-H1343 development board

Users Manual

Pb-free, Green All boards produced by Olimex are ROHS compliant

Revision Initial, September 2011

INTRODUCTION

LPC-H1343 is header board with LPC1343 ARM Cortex-M3 based microcontroller for embedded applications from NXP. LPC-H1343 features a high level of integration and low power consumption. This microcontroller supports various interfaces such as one Fast-mode Plus I^2C-bus interface, USB, UART, SSP interfaces, four general purpose timers, a 10-bit ADC. On the board are available Debug Interface and extension headers for all microcontroller ports.

BOARD FEATURES

- MCU: **LPC1343FBD48** Cortex-M3, up to 70 Mhz, 32 kB Flash, 8kB SRAM, UART RS-485, USB, SSP, I^2C/Fast+, ADC
- Debug interface – SWD (Serial Wire Debug)
- Extension connectors
- FR-4, 1.5 mm, soldermask, component print
- Dimensions:38.00x38.00mm (1.50 x 1.50")

ELECTROSTATIC WARNING

The **LPC-H1343** board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.

BOARD USE REQUIREMENTS

Cables: The cable you will need depends on the programmer/debugger you use. If you use ARM-JTAG-EW, you will need USB A-B cable.

Hardware: Programmer/Debugger ARM-JTAG-EW or other compatible programming/debugging tool if you work with EW-ARM.

ARM-USB-OCD, ARM-USB-OCD-H, ARM-USB-TINY, ARM-USB-TINY-H - JTAGs + ARM-JTAG-SWD adapter can be used with Rowley Crossworks.

PROCESSOR FEATURES

LPC-H1343 board use ARM Cortex™-M3 microcontroller **LPC1343FBD48** from NXP Semiconductors with these features:

–ARM Cortex-M3 processor, running at frequencies of up to 72 MHz

–ARM Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).

–32kB on-chip flash programming memory. Enhanced flash memory accelerator enables high- peed 72 MHz operation with zero wait states

–In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.

–Serial interfaces:

- USB 2.0 full-speed device controller with on-chip PHY for device

- UART with fractional baud rate generation, modem, internal FIFO and RS-485/EIA-485 support.

- SSP controller with FIFO and multi-protocol capabilities.

- I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.

–Other peripherals:

- 42 General Purpose I/O (GPIO) pins with configurable pull-up/down resistors and a new, configurable open-drain operating mode.

- Four general purpose timers/counters, with a total of four capture inputs and 13 match outputs.

- Programmable WatchDog Timer (WDT).

- System tick timer.

–Serial Wire Debug and Serial Wire Trace Port.

–High-current output driver (20 mA) on one pin.

–High-current sink drivers (20 mA) on two I2C-bus pins in Fast-mode Plus.

–Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.

–Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.

–Single 3.3 V power supply (2.0 V to 3.6 V).

–10-bit ADC with input multiplexing among 8 pins.

–40 GPIO pins can be used as edge and level sensitive interrupt sources.

–Clock output function with divider that can reflect the main oscillator clock, IRC clock, CPU clock, Watchdog clock, and the USB clock.

–Processor wake-up from Deep-sleep mode via GPIO interrupts.

–Brownout detect with four separate thresholds for interrupt and one threshold for forced reset.

–Power-On Reset (POR).

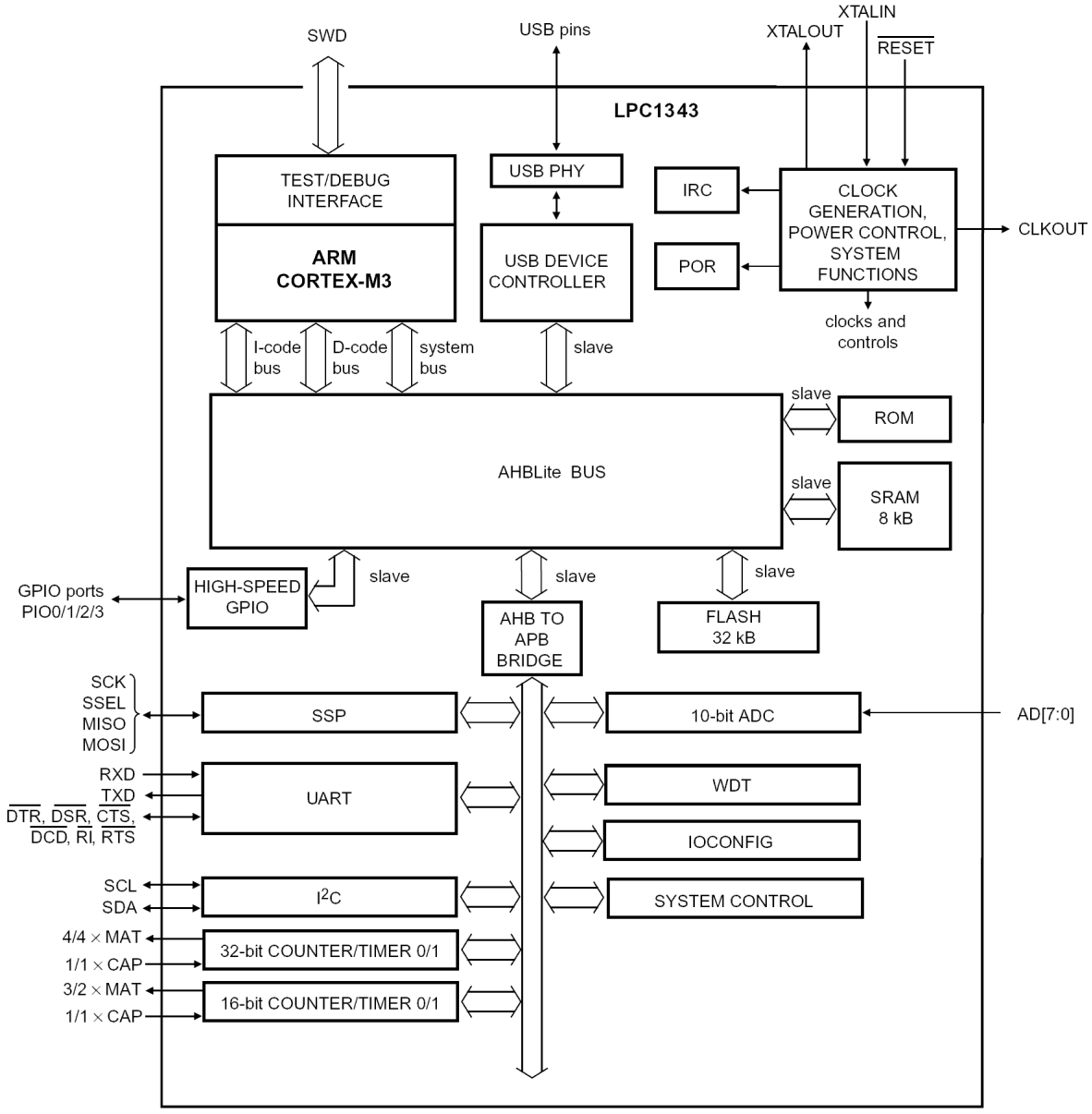
–Crystal oscillator with an operating range of 1 MHz to 25 MHz.

–12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.

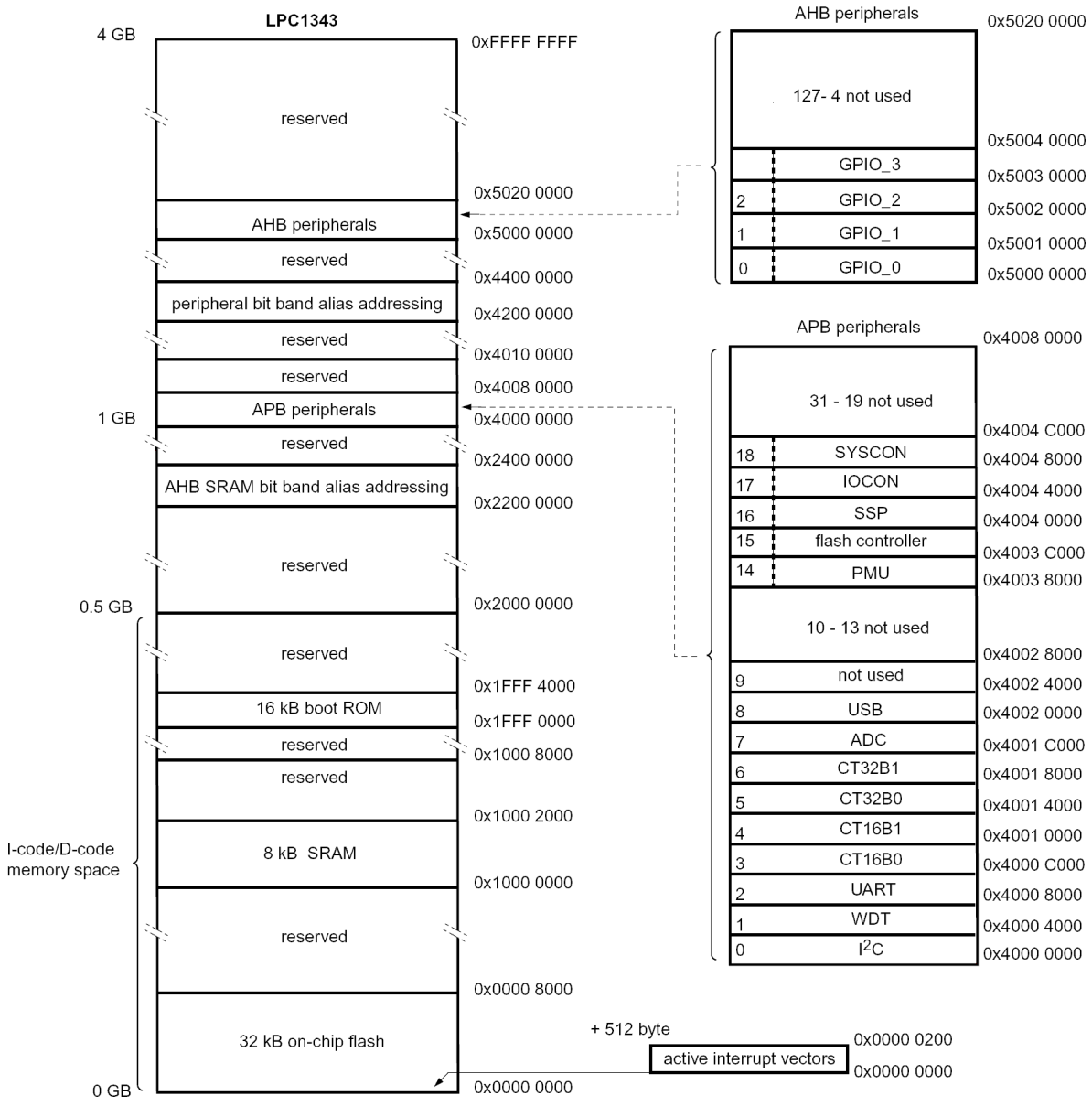
–PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the Watchdog oscillator.

–Code Read Protection (CRP) with different security levels.

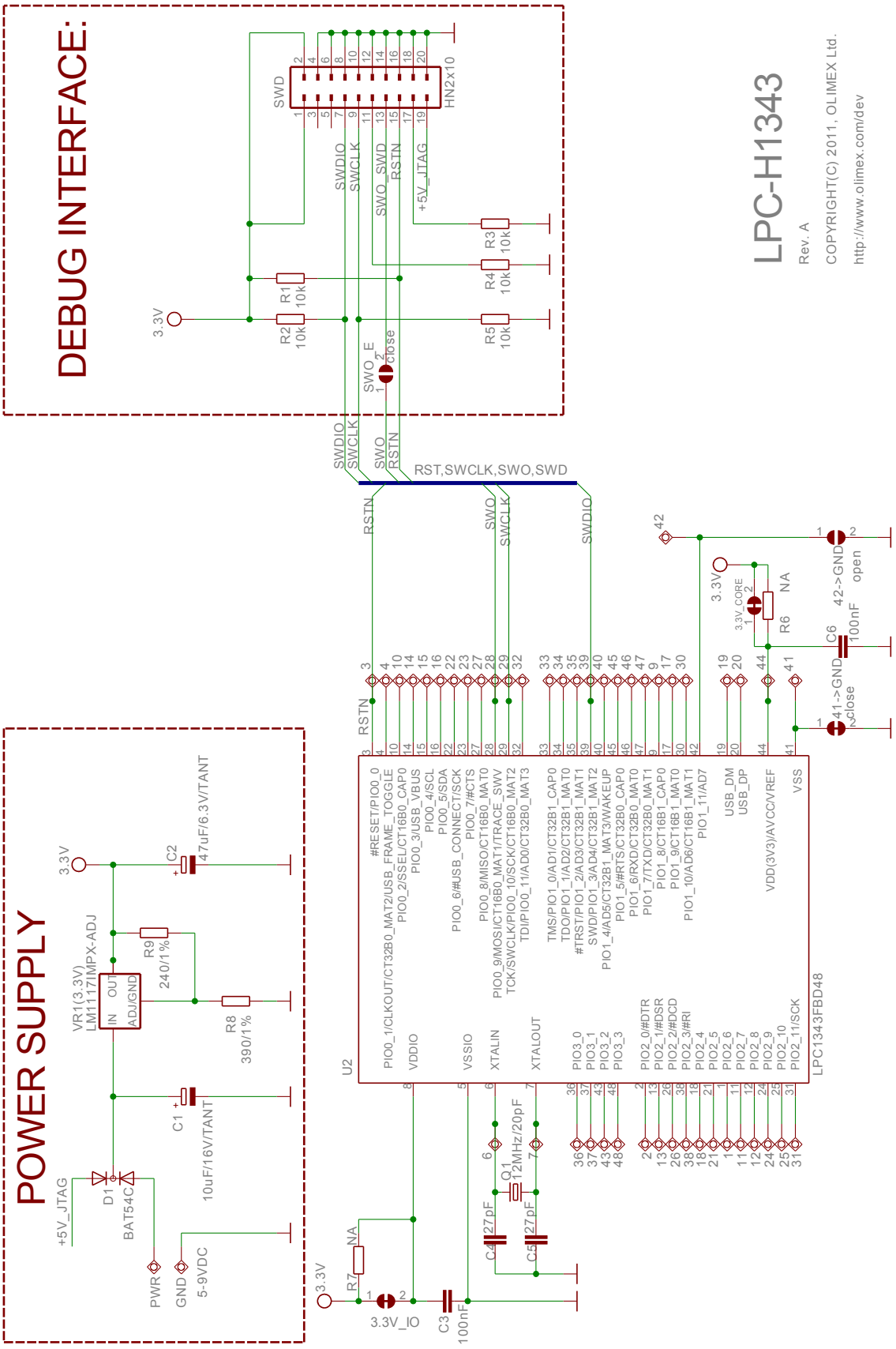
BLOCK DIAGRAM



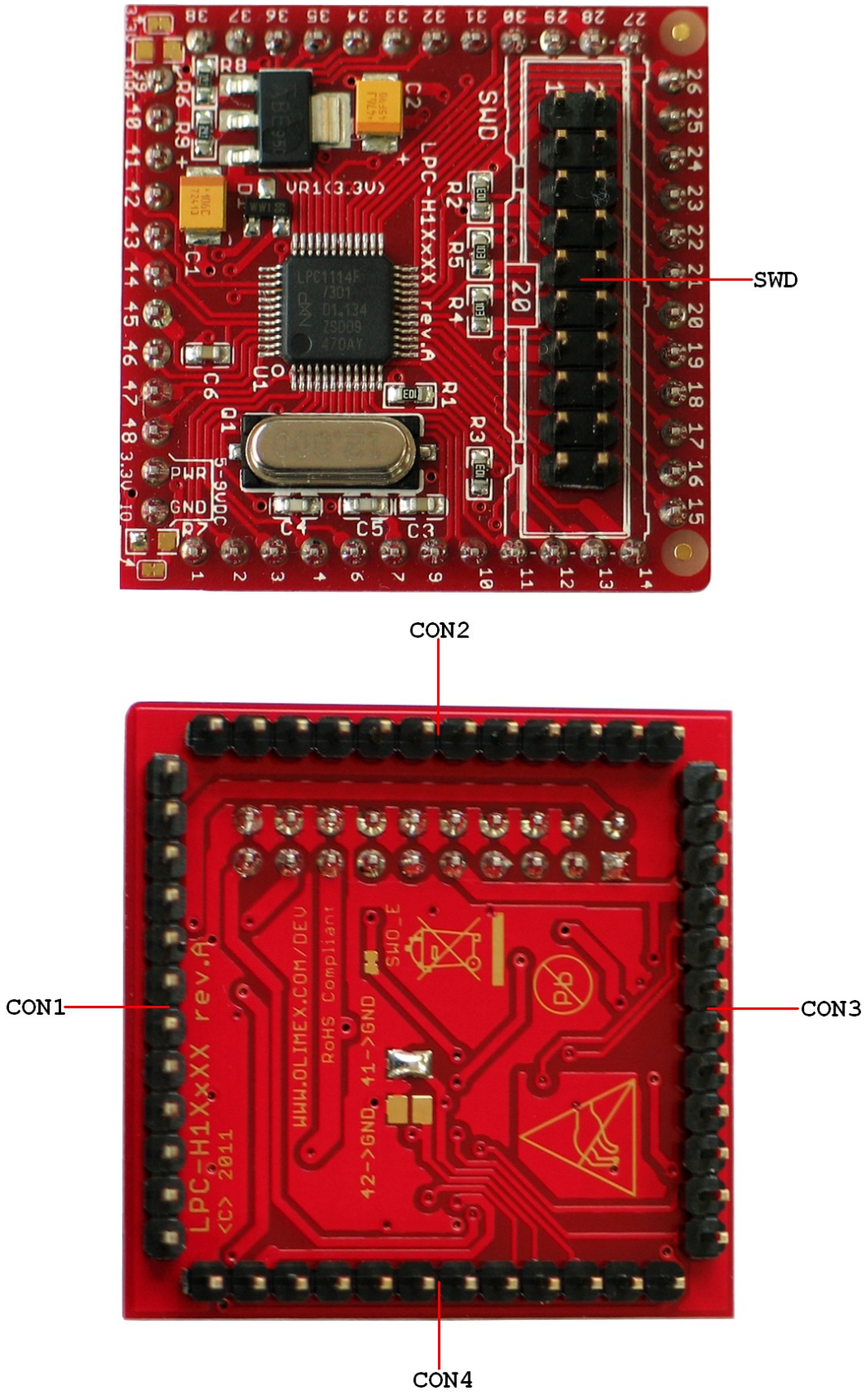
MEMORY MAP


LPC1343
4 GB
1 GB
0.5 GB
0 GB
0xFFFF FFFF
reserved
0x5020 0000
AHB peripherals
0x5000 0000
reserved
0x4400 0000
peripheral bit band alias addressing
0x4200 0000
reserved
0x4010 0000
reserved
0x4008 0000
APB peripherals
0x4000 0000
reserved
0x2400 0000
AHB SRAM bit band alias addressing
0x2200 0000
reserved
0x2000 0000
reserved
0x1FFF 4000
16 kB boot ROM
0x1FFF 0000
reserved
0x1000 8000
reserved
0x1000 2000
8 kB SRAM
0x1000 0000
reserved
0x0000 8000
32 kB on-chip flash
0x0000 0000
I-code/D-code memory space
+ 512 byte
active interrupt vectors
0x0000 0200
0x0000 0000
AHB peripherals
0x5020 0000
127- 4 not used
0x5004 0000
GPIO_3
0x5003 0000
2 GPIO_2
0x5002 0000
1 GPIO_1
0x5001 0000
0 GPIO_0
0x5000 0000
APB peripherals
0x4008 0000
31 - 19 not used
0x4004 C000
18 SYSCON
0x4004 8000
17 IOCON
0x4004 4000
16 SSP
0x4004 0000
15 flash controller
0x4003 C000
14 PMU
0x4003 8000
10 - 13 not used
0x4002 8000
9 not used
0x4002 4000
8 USB
0x4002 0000
7 ADC
0x4001 C000
6 CT32B1
0x4001 8000
5 CT32B0
0x4001 4000
4 CT16B1
0x4001 0000
3 CT16B0
0x4000 C000
2 UART
0x4000 8000
1 WDT
0x4000 4000
0 I2C
0x4000 0000

SCHEMATIC


DEBUG INTERFACE:
SWD
HN2x10
SWDIO
SWCLK
SWO_SWD
RSTN
+5V_JTAG
R1 10k
R2 10k
R3 10k
R4 10k
R5 10k
3.3V
SWO_E
close
RST,SWCLK,SWO,SWD
LPC-H1343
Rev. A
COPYRIGHT(C) 2011, OLIMEX Ltd.
http://www.olimex.com/dev
POWER SUPPLY
VR1(3.3V)
LM1117IMPX-ADJ
IN OUT ADJ/GND
C1 10uF/16V/TANT
C2 47uF/6.3V/TANT
R8 390/1%
R9 240/1%
D1 BAT54C
+5V_JTAG
PWR
GND
5-9VDC
U2
LPC1343FBD48
VDDIO
VSSIO
XTALIN
XTALOUT
VDD(3V3)/AVCC/VREF
VSS
USB_DM
USB_DP
Q1 12MHz/20pF
C4 27pF
C5 27pF
C3 100nF
R7 NA
3.3V_IO
3.3V_CORE
R6 NA
C6 100nF
42->GND
open
41->GND
close

BOARD LAYOUT



POWER SUPPLY CIRCUIT

LPC-H1343 is power supplied with +5V via JTAG and (5÷9)VDC via Extension connector CON4 pins PWR and GND.

The board power consumption is about 20 mA.

RESET CIRCUIT

LPC-H1343 reset circuit includes LPC1343 pin 3 (#RESET/PIO0_0), R1 (10k) and SWD connector pin 15.

CLOCK CIRCUIT

Quartz crystal 12 MHz is connected to LPC1343 pin 6 (XTALIN) and pin 7 (XTALOUT).

JUMPER DESCRIPTION

3.3V_CORE

This jumper, when closed, enables microcontroller 3.3V power supply.
Default state is closed.

3.3V_IO

This jumper, when closed, supplies 3.3 V voltage to LPC1343 pin 8 (VDDIO).
Default state is closed.

SWO_E

This jumper, when closed, connects SWD connector pin 13 (SWO_SWD) to LPC1343 pin 28 (PIO0_9).
Default state is closed.

41->GND

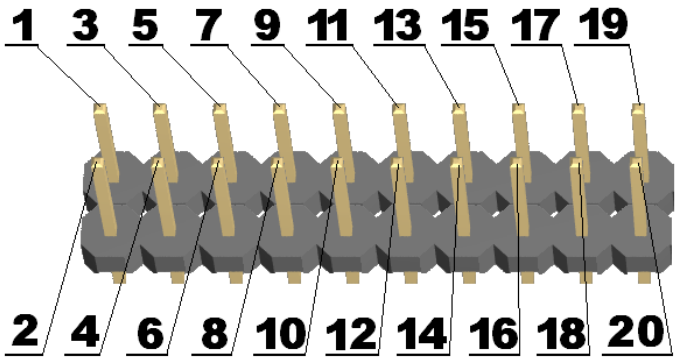
This jumper, when closed, connects LPC1343 pin 41 (VSS) to GND.
Default state is closed.

42->GND

This jumper, when closed, connects LPC1343 pin 42 (PIO1_11) to GND.
Default state is opened.

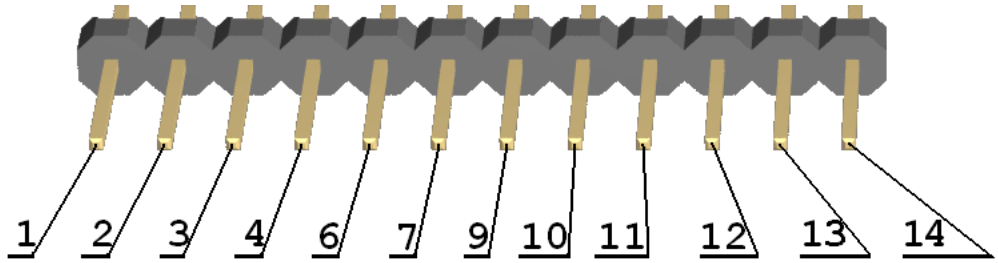
EXTERNAL CONNECTORS DESCRIPTION

SWD



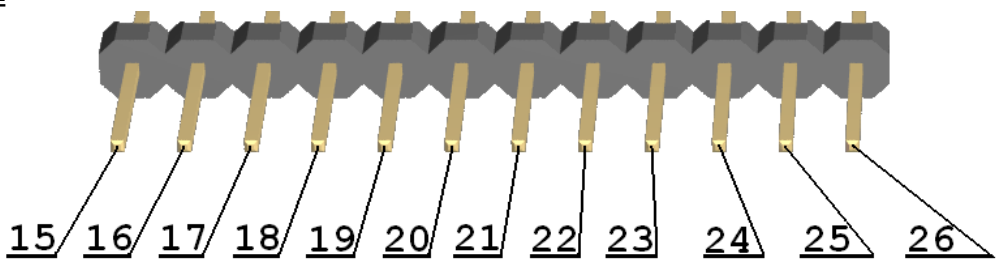
Pin #	Signal Name	Pin #	Signal Name
1	VCC (3.3V)	2	VCC (3.3V)
3	Not Connected	4	GND
5	Not Connected	6	GND
7	SWDIO	8	GND
9	SWCLK	10	GND
11	pull-down	12	GND
13	SWO_SWD	14	GND
15	RSTN	16	GND
17	pull-down	18	GND
19	+5V_JTAG	20	GND

CON1



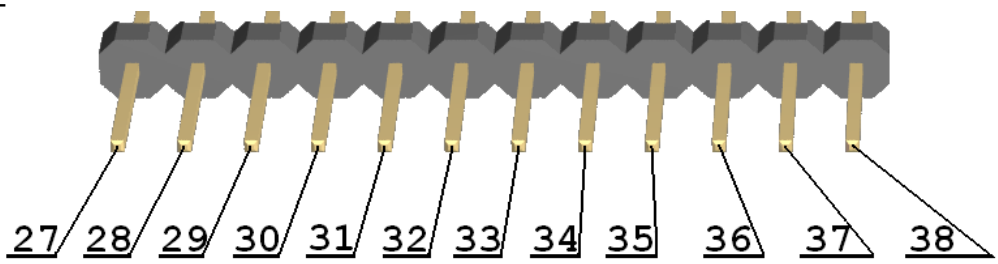
Pin #	Signal Name	Pin #	Signal Name
1	PIO2_6	2	PIO2_0
3	RSTN	4	PIO0_1
6	XTALIN	7	XTALOUT
9	PIO1_8	10	PIO0_2
11	PIO2_7	12	PIO2_8
13	PIO2_1	14	PIO0_3

CON2



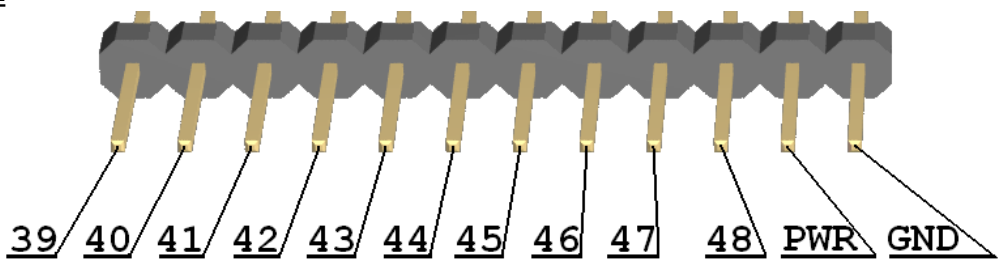
Pin #	Signal Name	Pin #	Signal Name
15	PIO0_4	16	PIO0_5
17	PIO1_9	18	PIO2_4
19	USB_DM	20	USB_DP
21	PIO2_5	22	PIO0_6
23	PIO0_7	24	PIO2_9
25	PIO2_10	26	PIO2_2

CON3



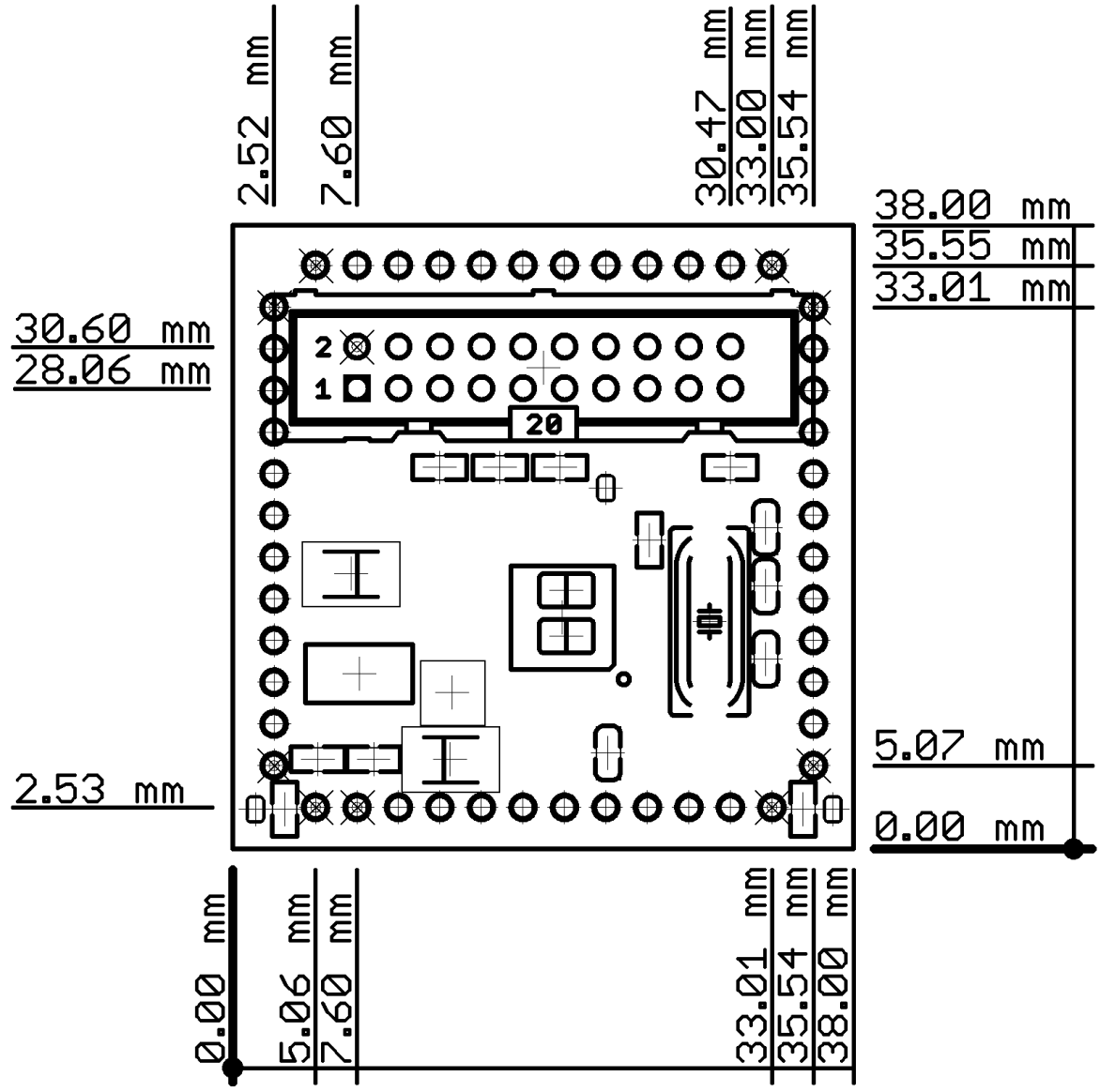
Pin #	Signal Name	Pin #	Signal Name
27	PIO0_8	28	SWO
29	SWCLK	30	PIO1_10
31	PIO2_11	32	PIO0_11
33	PIO1_0	34	PIO1_1
35	PIO1_2	36	PIO3_0
37	PIO3_1	38	PIO2_3

CON4



Pin #	Signal Name	Pin #	Signal Name
39	SWDIO	40	PIO1_4
41	VSS (GND)	42	PIO1_11
43	PIO3_2	44	VDD(3V3)
45	PIO1_5	46	PIO1_6
47	PIO1_7	48	PIO3_3
PWR	PWR	GND	GND

MECHANICAL DIMENSIONS



AVAILABLE DEMO SOFTWARE

- Coming soon at our website.

ORDER CODE

LPC-H1343 - assembled and tested board

How to order?

You can order to us directly or by any of our distributors.
Check our web www.olimex.com/dev for more info.

Revision history

Board's Revision	Rev. A, July 2011
Manual's Revision	Rev. Initial, September 2011

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