... the world's most energy friendly microcontrollers

EFM32ZG222 DATASHEET

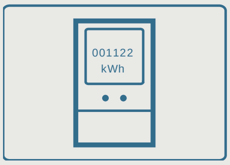
F32/F16/F8/F4

Preliminary

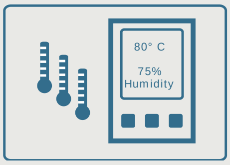
- **ARM Cortex-M0 CPU platform**
  - High Performance 32-bit processor @ up to 32 MHz
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 20 nA @ 3 V Shutoff Mode
  - 0.6 µA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 0.9 µA @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 45 µA/MHz @ 3 V Sleep Mode
  - 130 µA/MHz @ 3 V Run Mode, with code executed from flash
- **32/16/8/4 KB Flash**
- **4/4/2/2 KB RAM**
- **37 General Purpose I/O pins**
  - Configurable Push-pull, Open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 16 asynchronous external interrupts
  - Output state retention and wakeup from Shutoff Mode
- **4 Channel Peripheral Reflex System for autonomous inter-peripheral signaling**
- **Timers/Counters**
  - 2× 16-bit Timer/Counter
    - 2×3 Compare/Capture/PWM channels
  - 24-bit Real-Time Counter
  - 16-bit Pulse Counter
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- **Communication interfaces**
  - Universal Synchronous/Asynchronous Receiver/Transmitter
    - UART/SPI/SmartCard (ISO 7816)/I2S
    - Triple buffered full/half-duplex operation
  - Low Energy UART
  - I^2C Interface with SMBus support
    - Address recognition in Stop Mode
- **Ultra low power precision analog peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter
    - 4 single ended channels/ differential channels
    - On-chip temperature sensor
  - Analog Comparator
    - Capacitive sensing with up to 5 inputs
  - Supply Voltage Comparator
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **2-pin Serial Wire Debug interface**
  - 1-pin Serial Wire Viewer
- **Pre-Programmed Serial Bootloader**
- **Temperature range -40 to 85 ºC**
- **Single power supply 1.8 to 3.8 V**
- **LQFP48 package**

EFM32ZG222 microcontrollers are suited for all battery operated applications

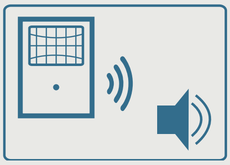
Energy Metering



Industrial/Home Automation



Wireless Alarm/Security



Medical Systems

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32ZG222 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (KB)	RAM (KB)	Max Speed (MHz)	Supply Voltage	Temperature	Package
EFM32ZG222F4-QFP48	4	2	32	1.8 to 3.8V	-40 to 85 ºC	LQFP48
EFM32ZG222F8-QFP48	8	2	32	1.8 to 3.8V	-40 to 85 ºC	LQFP48
EFM32ZG222F16-QFP48	16	4	32	1.8 to 3.8V	-40 to 85 ºC	LQFP48
EFM32ZG222F32-QFP48	32	4	32	1.8 to 3.8V	-40 to 85 ºC	LQFP48

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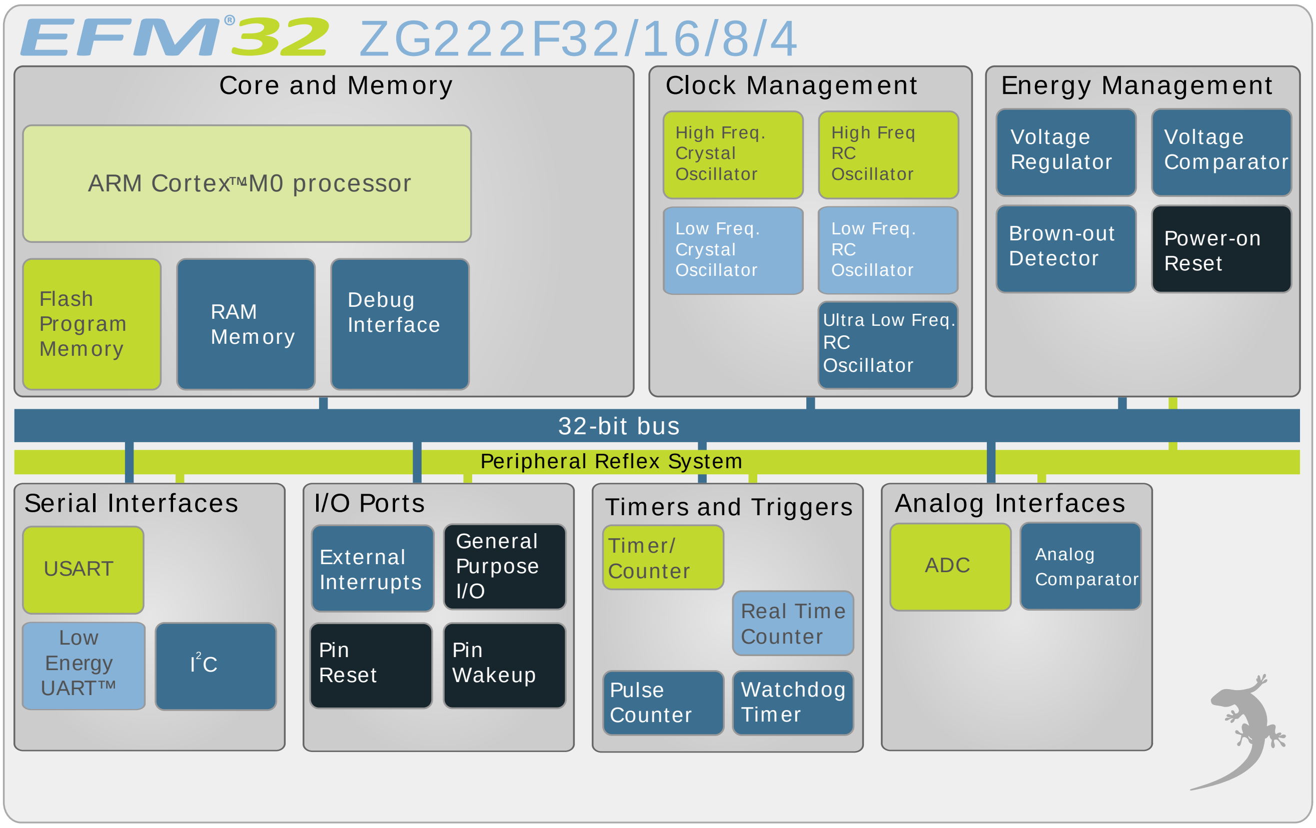
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M0, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32ZG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32ZG222 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32ZG Reference Manual*.

A block diagram of the EFM32ZG222 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M0 Core

The ARM Cortex-M0 includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M0 is described in detail in *EFM32 Cortex-M0 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32ZG microcontroller. The flash memory is readable and writable from the Cortex-M0. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32ZG.

2.1.5 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32ZG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.6 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32ZG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.7 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.8 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.9 Inter-Integrated Circuit Interface (I2C)

The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.10 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, and I2S devices.

2.1.11 Pre-Programmed Serial Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Autobaud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.12 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART^{TM}, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.13 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output.

2.1.14 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.15 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 – EM3.

2.1.16 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.17 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.18 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 4 external pins and 6 internal signals.

2.1.19 General Purpose Input/Output (GPIO)

In the EFM32ZG222, there are 37 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.2 Configuration Summary

The features of the EFM32ZG222 is a subset of the feature set described in the EFM32ZG Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

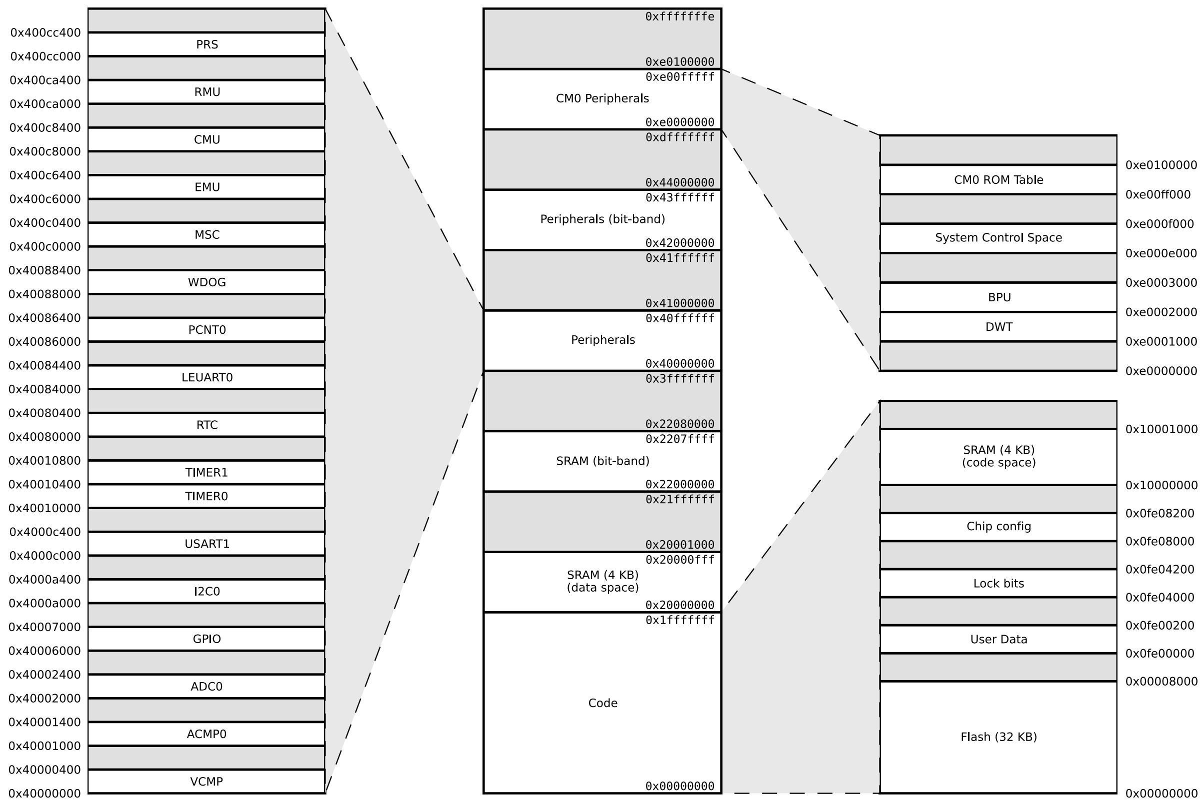
Table 2.1. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M0	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	I2S	US0_TX, US0_RX. US0_CLK, US0_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration	TIM0_CC[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
PCNT0		PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[4:0], ACMP0_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[3:0]
GPIO	37 pins	Available pins are shown in Table 4.3 (p. 41)

2.3 Memory Map

The *EFM32ZG222* memory map is shown in Figure 2.2 (p. 7), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32ZG222 Memory Map with largest RAM and Flash sizes



3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on T_{AMB}=25°C and V_{DD}=3.0 V, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8) .

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150[1]	°C
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	°C
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		V_{DD}+0.3	V

[1]Based on programmed devices tested for 10000 hours at 150ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	°C
V_{DDOP}	Operating supply voltage	1.8		3.8	V
f_{APB}	Internal APB clock frequency			32	MHz
f_{AHB}	Internal AHB clock frequency			32	MHz

3.3.2 Environmental

Table 3.3. Environmental

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ESDHBM}	ESD (Human Body Model HBM)	T_{AMB}=25°C			2	kV
V_{ESDCDM}	ESD (Charged Device Model, CDM)	T_{AMB}=25°C			1	kV

Latch-up sensitivity test passed level A according to JEDEC JESD 78B method Class II, 85°C.

3.4 Current Consumption

Table 3.4. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash.	32 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V		130		µA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		130	169	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		131	170	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		133	175	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		134	177	µA/ MHz
		7 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		137	185	µA/ MHz
		1 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		158		µA/ MHz
I_{EM1}	EM1 current	32 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V		45		µA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		47	62	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		48	64	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		50	69	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		51	72	µA/ MHz
		7 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		56	83	µA/ MHz
		1 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V		103		µA/ MHz
I_{EM2}	EM2 current	EM2 current with RTC at 1 Hz, RTC prescaled to 1kHz, 32 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=25°C		0.9		µA
		EM2 current with RTC at 1 Hz, RTC prescaled to 1kHz, 32 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85°C		3.0	6.0	µA
I_{EM3}	EM3 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.59		µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		2.75	5.8	µA
I_{EM4}	EM4 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.02		µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		0.25	0.7	µA

3.5 Transition between Energy Modes

Table 3.5. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0[1]		HF core CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		µs
t_{EM30}	Transition time from EM3 to EM0		2		µs
t_{EM40}	Transition time from EM4 to EM0		163		µs

[1]Core wakeup time only.

3.6 Power Management

Table 3.6. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage		1.82		1.85	V
$V_{BODintthr-}$	BOD threshold on falling internally regulated supply voltage		1.62		1.68	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage			1.85		V
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		µs
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		µF

3.7 Flash

Table 3.7. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC_{FLASH}	Flash erase cycles before failure		20000			cycles
RET_{FLASH}	Flash data retention	T_{AMB}<150°C	10000			h
		T_{AMB}<85°C	10			years
		T_{AMB}<70°C	20			years
t_{W_PROG}	Word (32-bit) programming time		20			µs
t_{P_ERASE}	Page erase time		20	20.4	20.8	ms
t_{D_ERASE}	Device erase time		40	40.8	41.6	ms
I_{ERASE}	Erase current				7[1]	mA
I_{WRITE}	Write current				7[1]	mA
V_{FLASH}	Supply voltage during flash erase and write		1.8		3.8	V

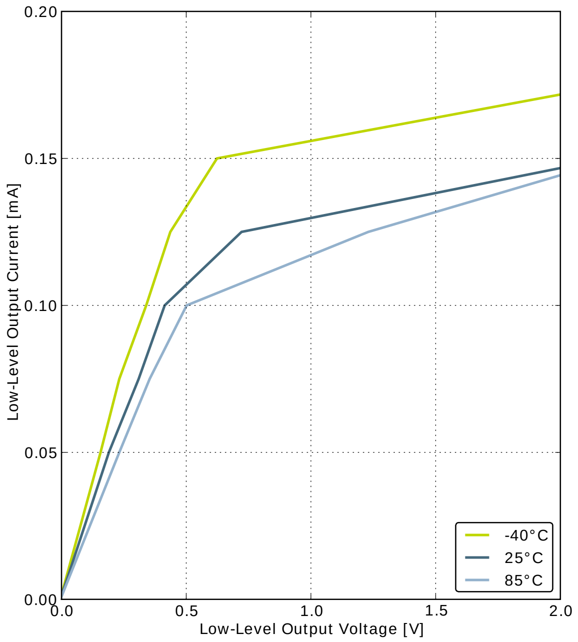
[1]Measured at 25°C

3.8 General Purpose Input Output

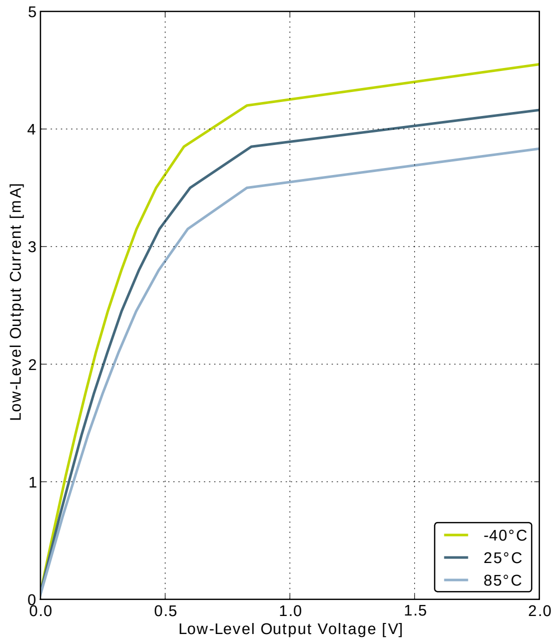
Table 3.8. GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IOIL}	Input low voltage				$0.3V_{DD}$	V
V_{IOIH}	Input high voltage		$0.7V_{DD}$			V
V_{IOOH}	Output high voltage	Sourcing 6 mA, V_{DD}=1.8V, GPIO_Px_CTRL DRIVE-MODE = STANDARD	$0.75V_{DD}$			V
		Sourcing 6 mA, V_{DD}=3.0V, GPIO_Px_CTRL DRIVE-MODE = STANDARD	$0.95V_{DD}$			V
		Sourcing 20 mA, V_{DD}=1.8V, GPIO_Px_CTRL DRIVE-MODE = HIGH	$0.7V_{DD}$			V
		Sourcing 20 mA, V_{DD}=3.0V, GPIO_Px_CTRL DRIVE-MODE = HIGH	$0.9V_{DD}$			V
V_{IOOL}	Output low voltage	Sinking 6 mA, V_{DD}=1.8V, GPIO_Px_CTRL DRIVE-MODE = STANDARD			$0.25V_{DD}$	V
		Sinking 6 mA, V_{DD}=3.0V, GPIO_Px_CTRL DRIVE-MODE = STANDARD			$0.05V_{DD}$	V
		Sinking 20 mA, V_{DD}=1.8V, GPIO_Px_CTRL DRIVE-MODE = HIGH			$0.3V_{DD}$	V
		Sinking 20 mA, V_{DD}=3.0V, GPIO_Px_CTRL DRIVE-MODE = HIGH			$0.1V_{DD}$	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or Vdd			+/-25	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t_{IOOF}	Output fall time	0.5 mA drive strength and load capacitance C_L=12.5-25pF.	$20+0.1C_L$		250	ns
		2mA drive strength and load capacitance C_L=350-600pF	$20+0.1C_L$		250	ns
V_{IOHYST}	I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{DD} = 1.8 - 3.8 V	$0.1V_{DD}$			V

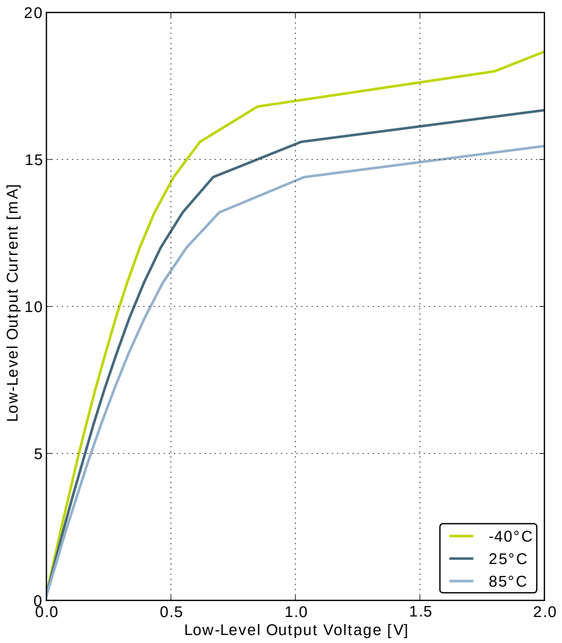
Figure 3.1. Typical Low-Level Output Current, 2V Supply Voltage



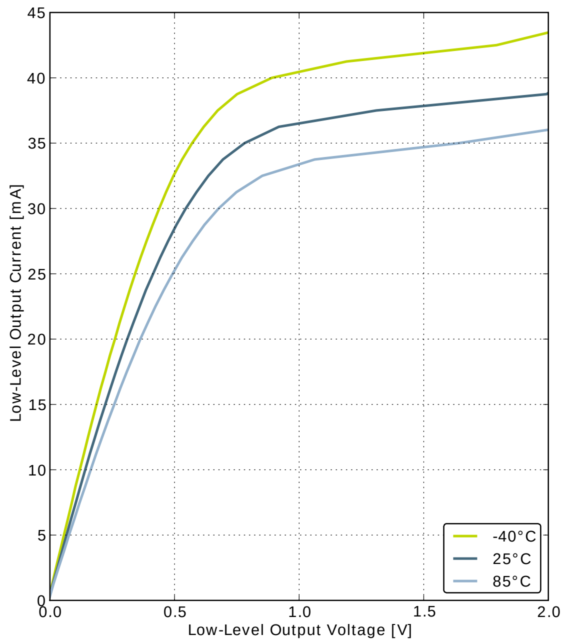
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.2. Typical High-Level Output Current, 2V Supply Voltage

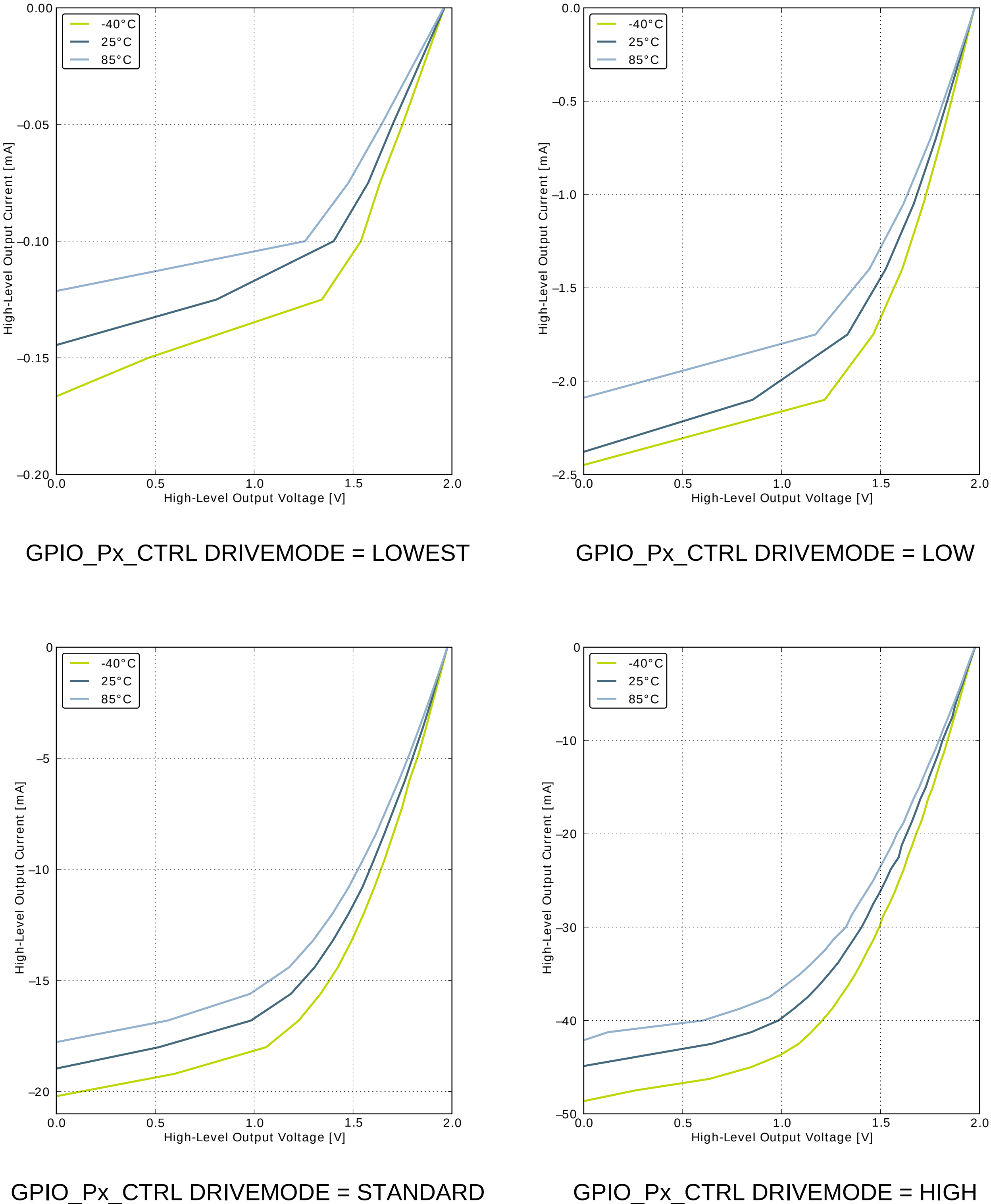
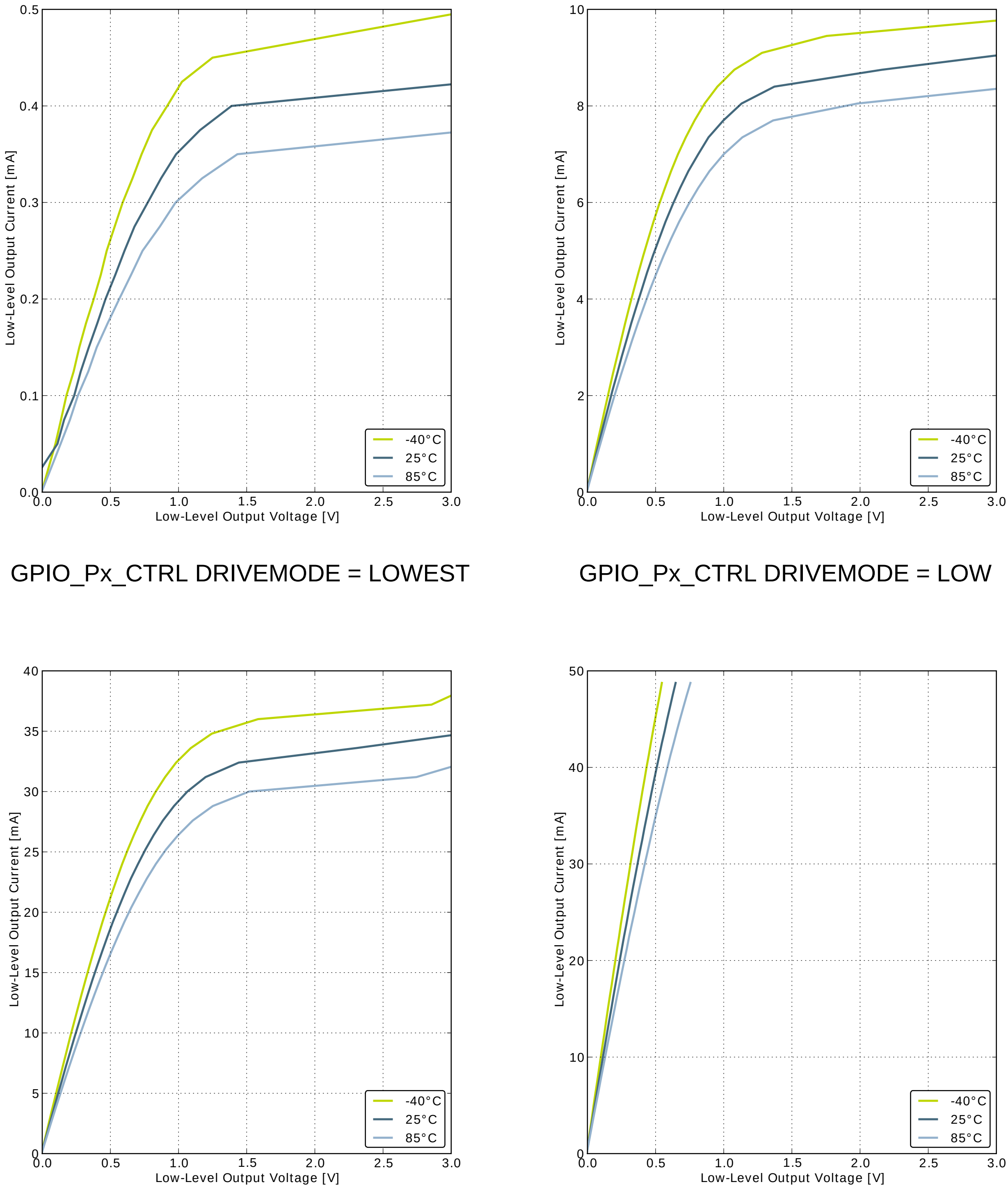


Figure 3.3. Typical Low-Level Output Current, 3V Supply Voltage



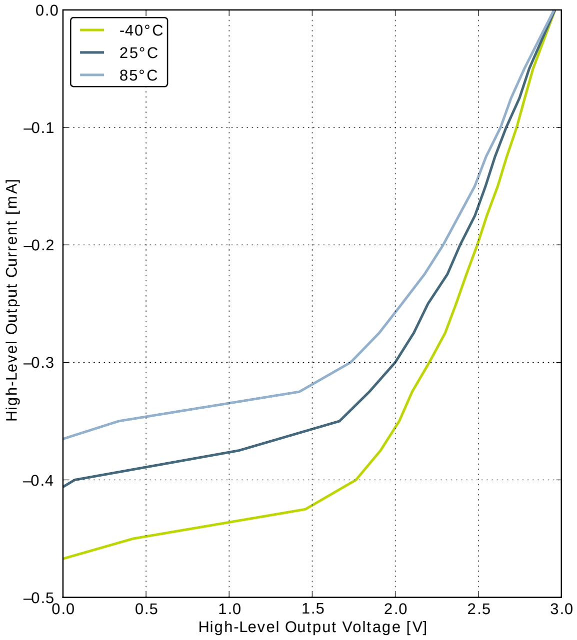
GPIO_Px_CTRL DRIVEMODE = LOWEST

GPIO_Px_CTRL DRIVEMODE = LOW

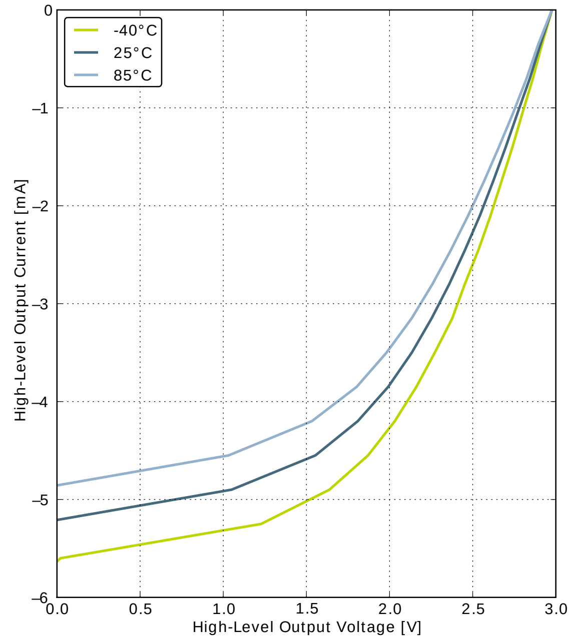
GPIO_Px_CTRL DRIVEMODE = STANDARD

GPIO_Px_CTRL DRIVEMODE = HIGH

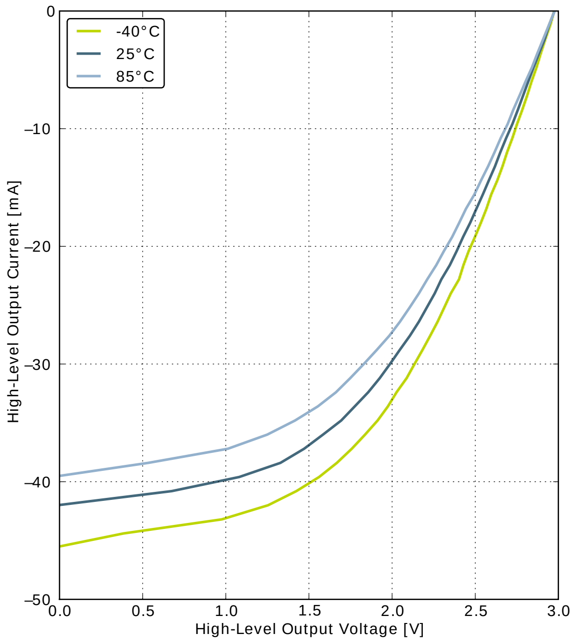
Figure 3.4. Typical High-Level Output Current, 3V Supply Voltage



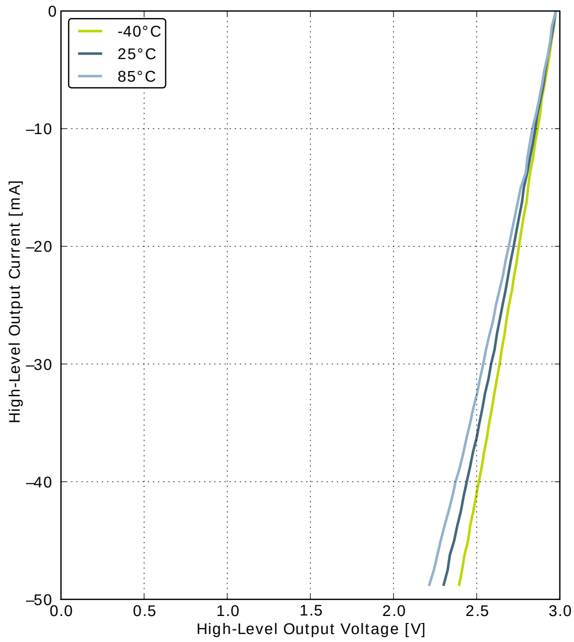
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.5. Typical Low-Level Output Current, 3.8V Supply Voltage

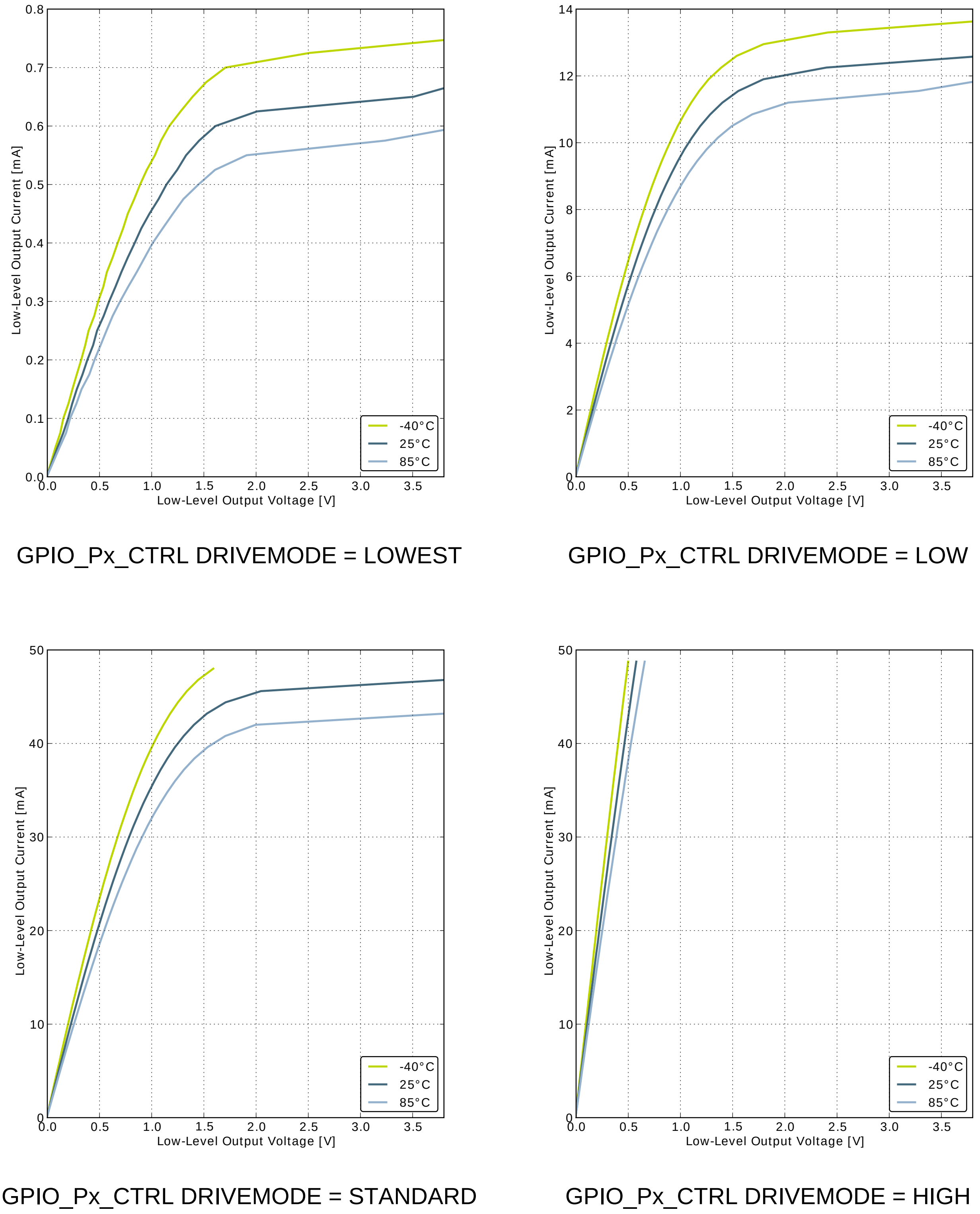
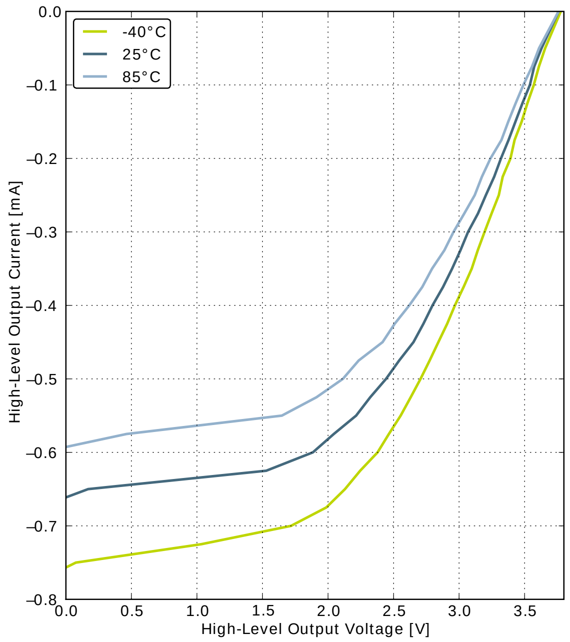
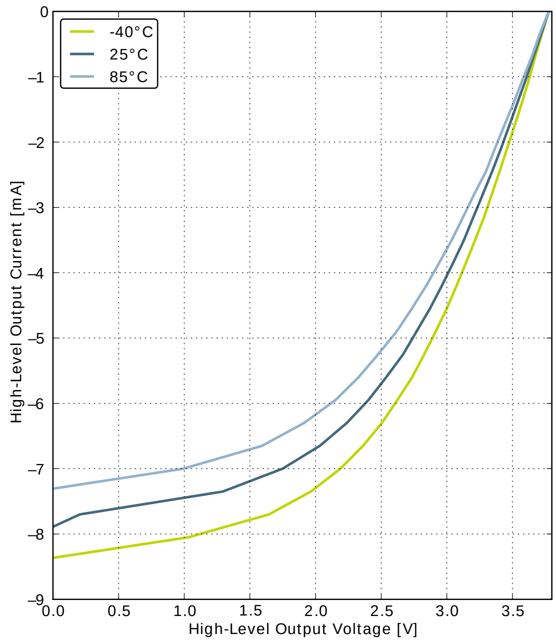


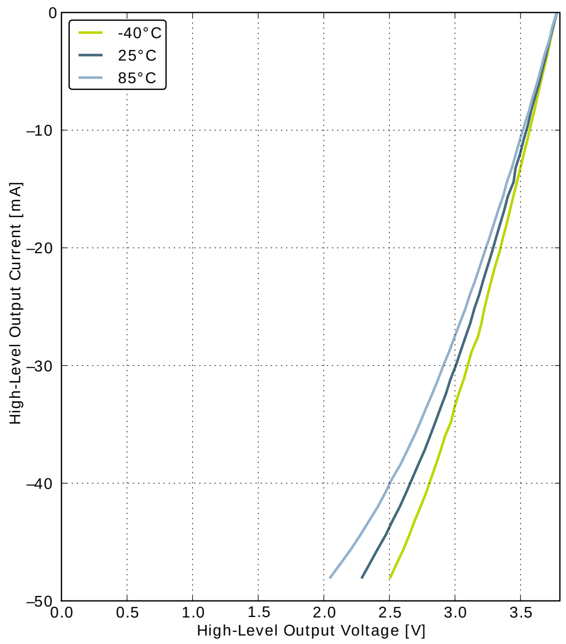
Figure 3.6. Typical High-Level Output Current, 3.8V Supply Voltage



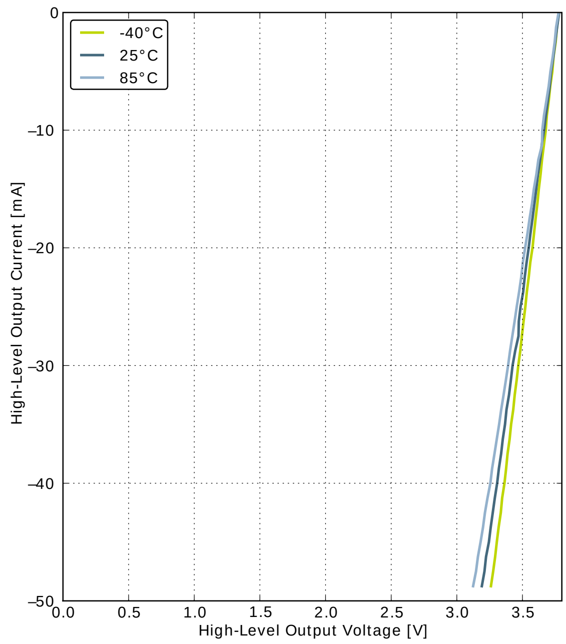
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.9. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		5		25	pF
DC_{LFXO}	Duty cycle		48	50	53.5	%
I_{LFXO}	Current consumption for core and buffer after start-up.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

3.9.2 HFXO

Table 3.10. HFXO

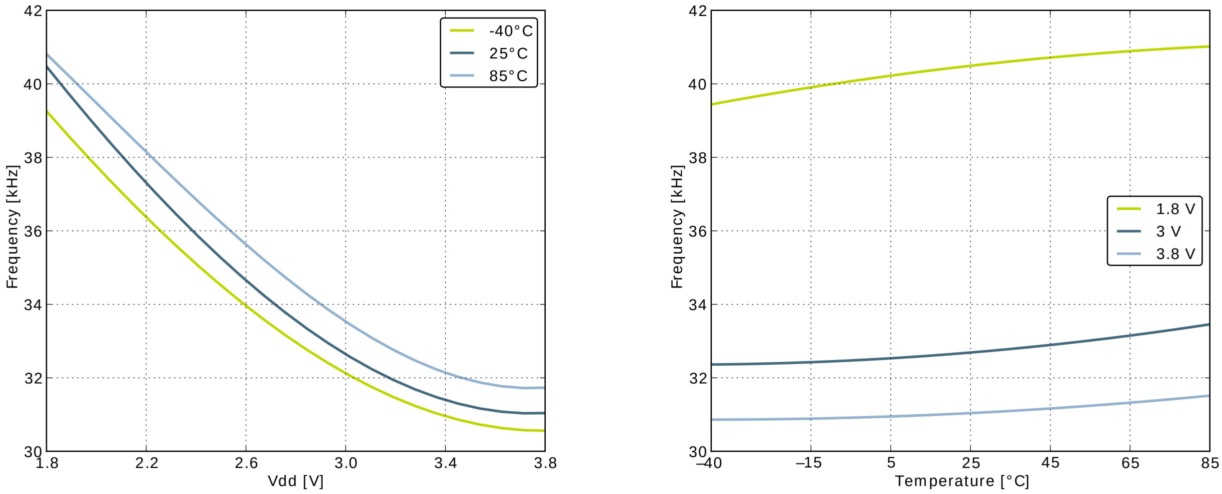
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported nominal crystal Frequency		4		32	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
DC_{HFXO}	Duty cycle		46	50	54	%
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		µs

3.9.3 LFRCO

Table 3.11. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency , V_{DD}= 3.0 V, T_{AMB}=25°C			32		kHz
t_{LFRCO}	Startup time not including software calibration			150		µs
I_{LFRCO}	Current consumption			190		nA
$TUNESTEP_{L-FRCO}$	Frequency step for LSB change in TUNING value			1.5		%

Figure 3.7. Calibrated LFRCO Frequency vs Temperature and Supply Voltage



3.9.4 HFRCO

Table 3.12. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	28 MHz frequency band		28		MHz
		21 MHz frequency band		21		MHz
		14 MHz frequency band		14		MHz
		11 MHz frequency band		11		MHz
		7 MHz frequency band		7		MHz
		1 MHz frequency band		1		MHz
$t_{HFRCO\_settling}$	Settling time after start-up	f_{HFRCO} = 14 MHz		0.6		Cycles
I_{HFRCO}	Current consumption	f_{HFRCO} = 28 MHz		106		µA
		f_{HFRCO} = 21 MHz		93		µA
		f_{HFRCO} = 14 MHz		77		µA
		f_{HFRCO} = 11 MHz		72		µA
		f_{HFRCO} = 7 MHz		63		µA
		f_{HFRCO} = 1 MHz		22		µA
DC_{HFRCO}	Duty cycle	f_{HFRCO} = 14 MHz	48.5	50	51	%
$TUNESTEP_{HFRCO}$	Frequency step for LSB change in TUNING value			0.3		%

Figure 3.8. Calibrated HFRCO 1 MHz Band Frequency vs Temperature and Supply Voltage

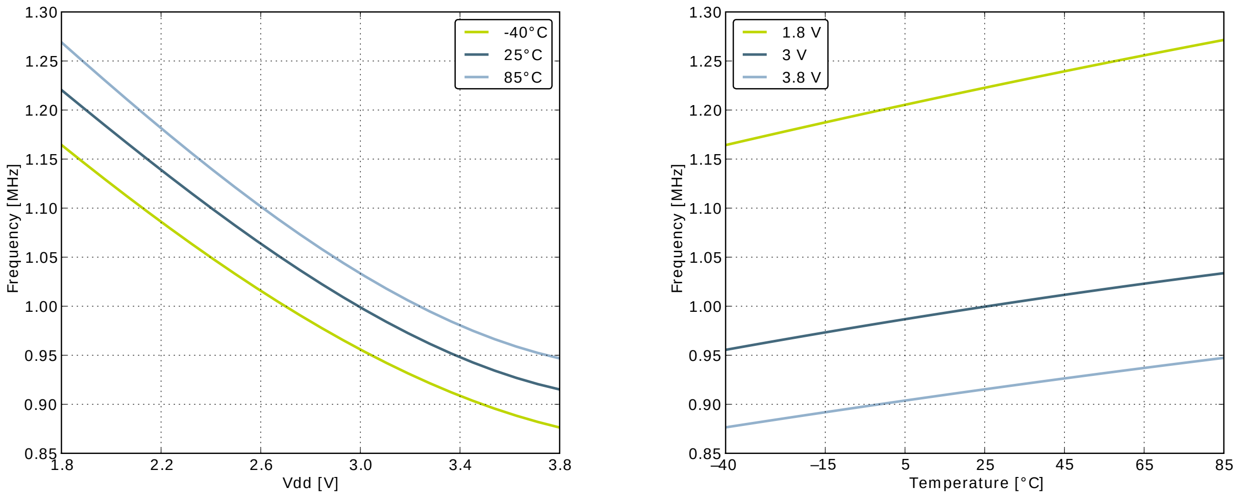


Figure 3.9. Calibrated HFRCO 7 MHz Band Frequency vs Temperature and Supply Voltage

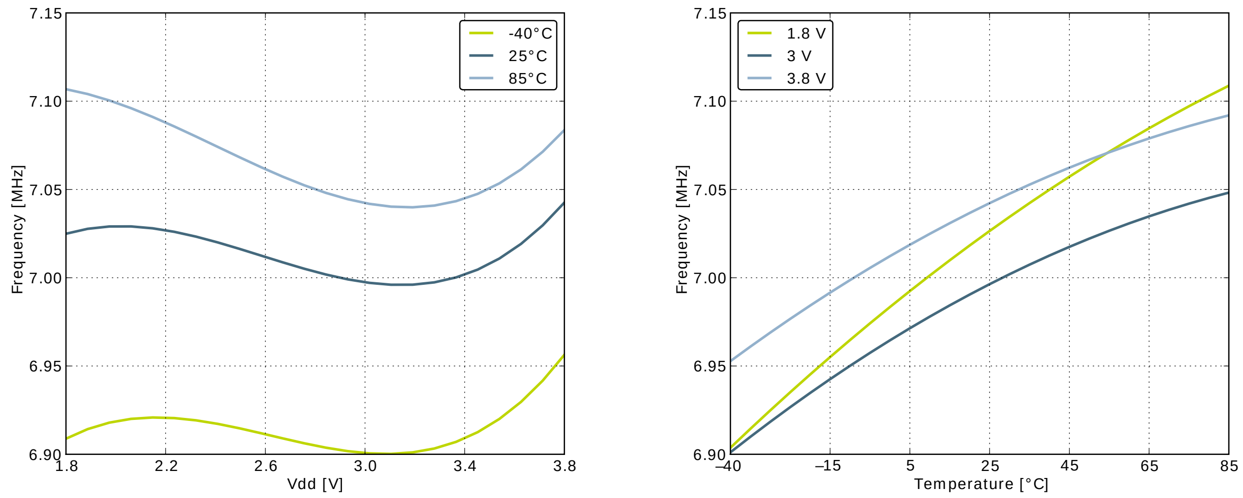


Figure 3.10. Calibrated HFRCO 11 MHz Band Frequency vs Temperature and Supply Voltage

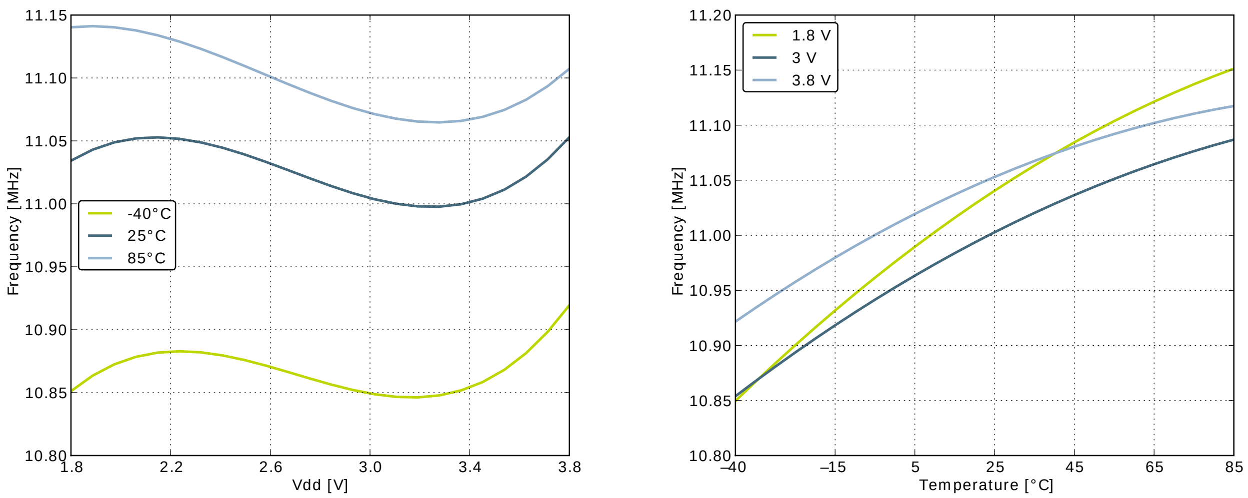


Figure 3.11. Calibrated HFRCO 14 MHz Band Frequency vs Temperature and Supply Voltage

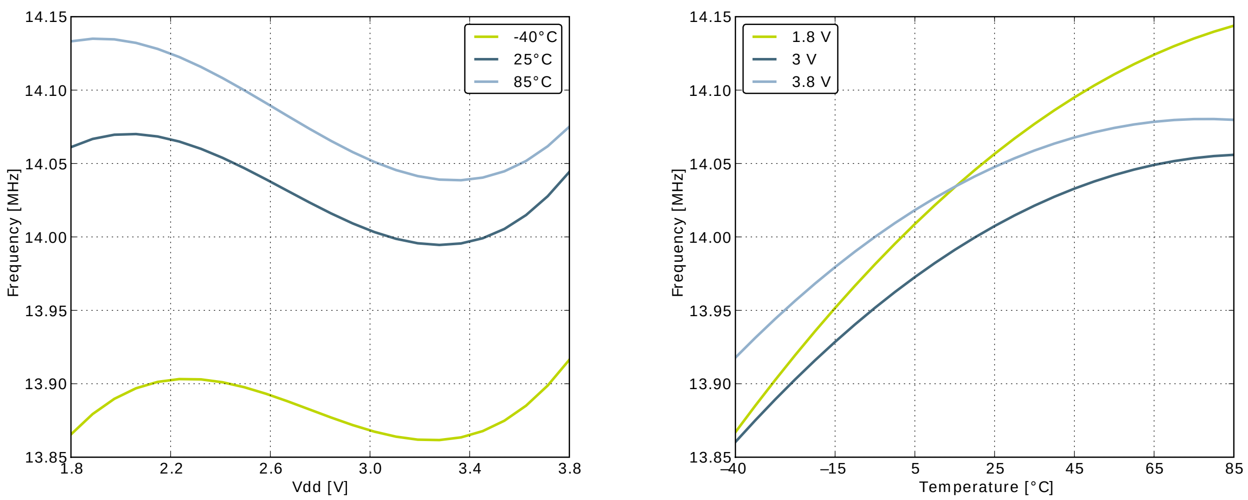


Figure 3.12. Calibrated HFRCO 21 MHz Band Frequency vs Temperature and Supply Voltage

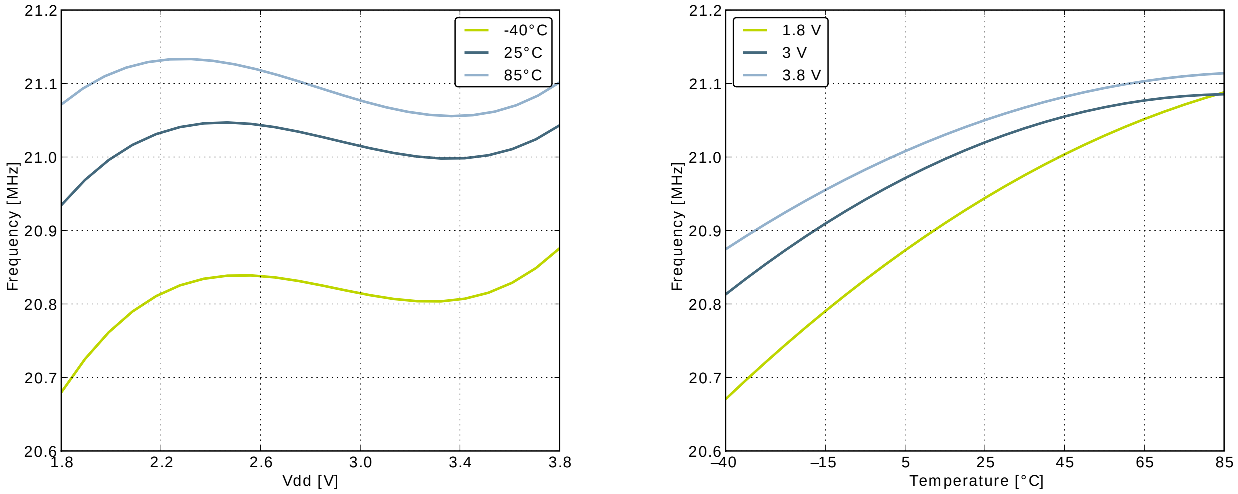
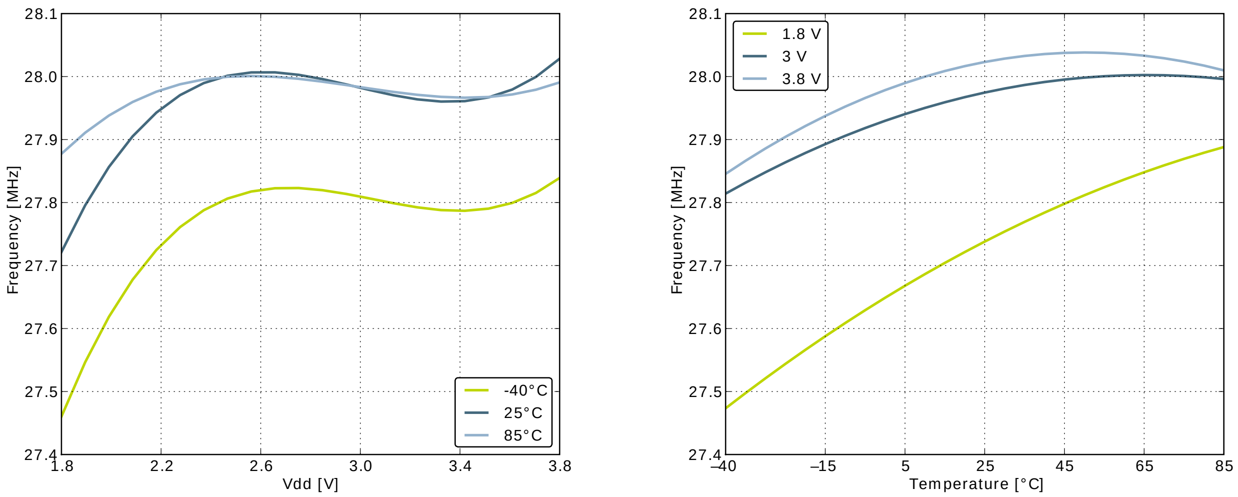


Figure 3.13. Calibrated HFRCO 28 MHz Band Frequency vs Temperature and Supply Voltage



3.9.5 ULFRCO

Table 3.13. ULFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ULFRCO}	Oscillation frequency	25°C, 3V	0.8		1.5	kHz
TC_{ULFRCO}	Temperature coefficient			0.05		%/°C
VC_{ULFRCO}	Supply voltage coefficient			-18.2		%/V

3.10 Analog Digital Converter (ADC)

Table 3.14. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ADCIN}	Input voltage range	Single ended	0		V_{REF}	V
		Differential	$-V_{REF}/2$		$V_{REF}/2$	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{ADCREFIN}$	Input range of external reference voltage, single ended and differential		1.25		V_{DD}	V
$V_{ADCREFIN\_CH7}$	Input range of external negative reference voltage on channel 7	See $V_{ADCREFIN}$	0		V_{DD} - 1.1	V
$V_{ADCREFIN\_CH6}$	Input range of external positive reference voltage on channel 6	See $V_{ADCREFIN}$	0.625		V_{DD}	V
$V_{ADCCMIN}$	Common mode input range		0		V_{DD}	V
I_{ADCIN}	Input current	2pF sampling capacitors		<100		nA
$CMRR_{ADC}$	Analog input common mode rejection ratio			65		dB
I_{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		351		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00		67		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		63		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10		64		µA
I_{ADCREF}	Current consumption of internal voltage reference	Internal voltage reference		65		µA
C_{ADCIN}	Input capacitance			2		pF
R_{ADCIN}	Input ON resistance		1			MOhm
$R_{ADCFILT}$	Input RC filter resistance			10		kOhm
$C_{ADCFILT}$	Input RC filter/decoupling capacitance			250		fF
f_{ADCCLK}	ADC Clock Frequency				13	MHz
$t_{ADCCONV}$	Conversion time	6 bit	7			ADC-CLK Cycles
		10 bit	11			ADC-CLK Cycles
		12 bit	13			ADC-CLK Cycles
t_{ADCACQ}	Acquisition time	Programmable	1		256	ADC-CLK Cycles
$t_{ADCACQVDD3}$	Required acquisition time for VDD/3 reference		2			µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{ADCSTART}$	Startup time of reference generator and ADC core in NORMAL mode			5		µs
	Startup time of reference generator and ADC core in KEEPADCWARM mode			1		µs
SNR_{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		65		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		65		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		67		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		67		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference		69		dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		70		dB
$SNDR_{ADC}$	Signal to Noise-puls-Distortion Ratio (SNDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference		68		dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
$SFDR_{ADC}$	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		76		dBc
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, V_{DD} reference		79		dBc
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		79		dBc
$V_{ADCOFFSET}$	Offset voltage	After calibration, single ended		0.3		mV
		After calibration, differential		0.3		mV
$TGRAD_{ADCTH}$	Thermometer output gradient			-1.16		mV/°C
				-3.85		ADC Codes/°C
DNL_{ADC}	Differential non-linearity (DNL)			±0.7		LSB
INL_{ADC}	Integral non-linearity (INL), End point method			±1.2		LSB
MC_{ADC}	No missing codes		11.999[1]	12		bits

[1]On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.14 (p. 29) and Figure 3.15 (p. 29) , respectively.

Figure 3.14. Integral Non-Linearity (INL)

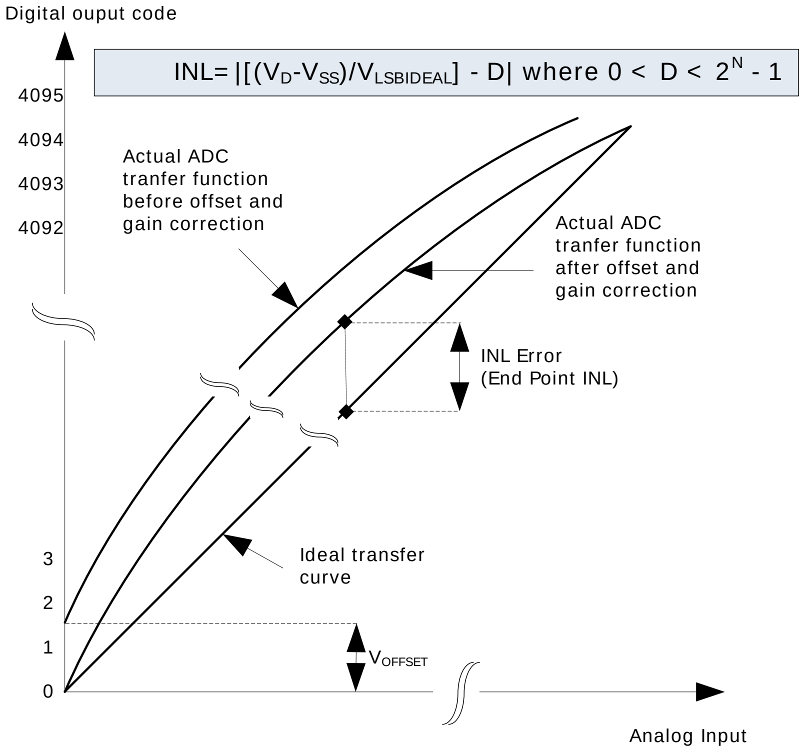
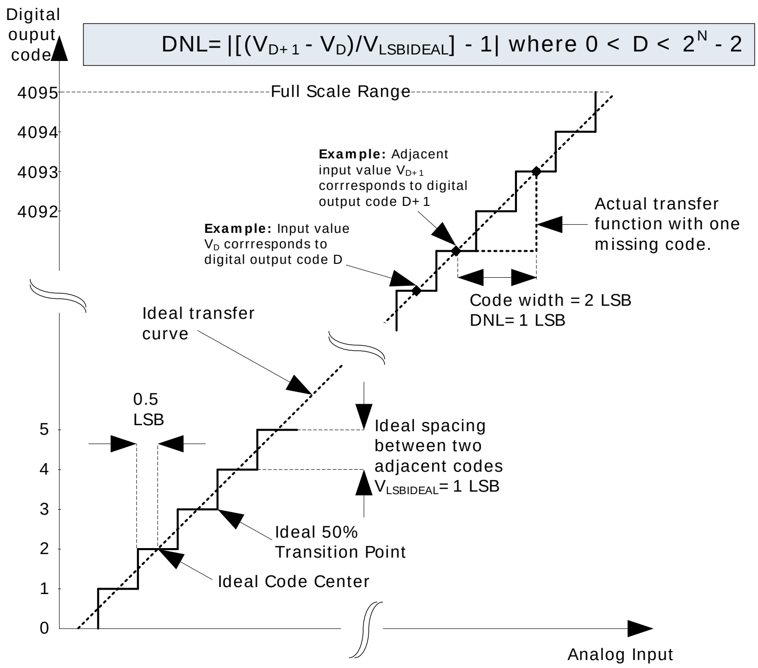
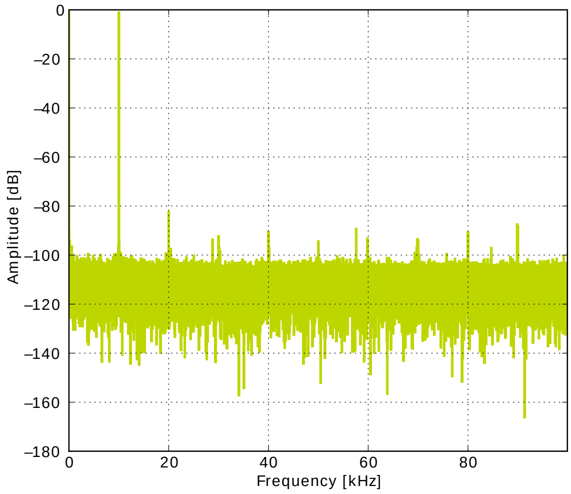


Figure 3.15. Differential Non-Linearity (DNL)

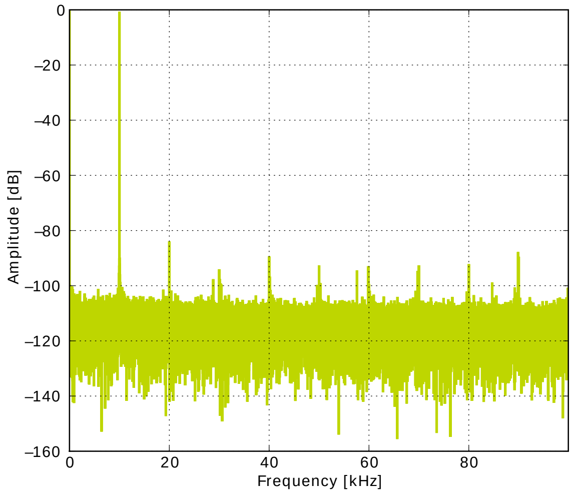


3.10.1 Typical performance

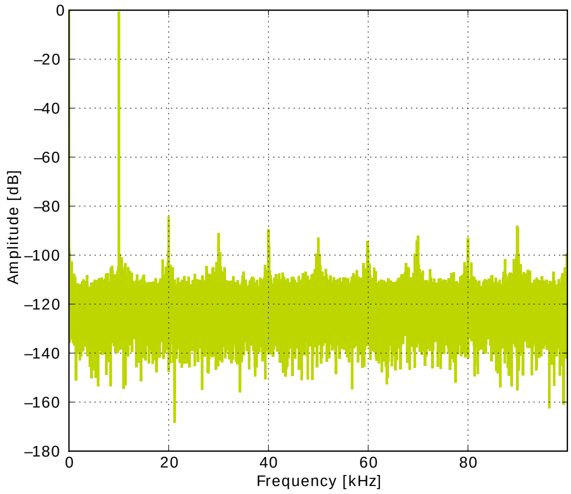
Figure 3.16. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°



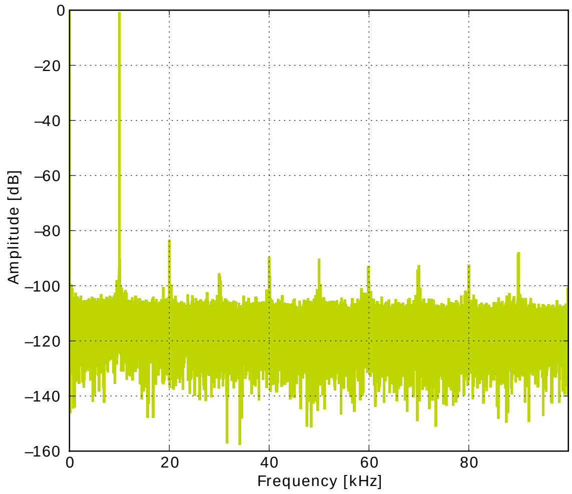
1.25V Reference



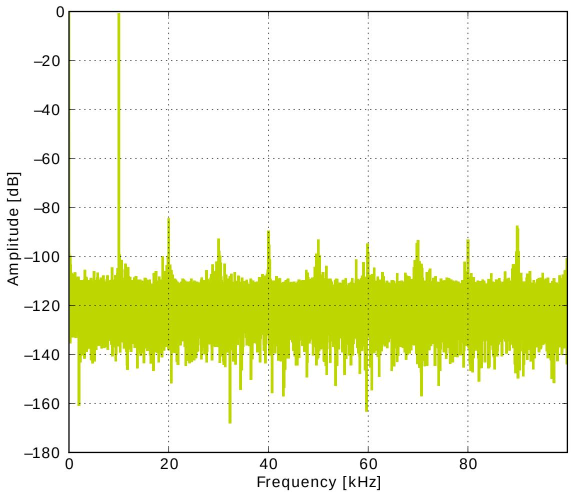
2.5V Reference



2XVDDVSS Reference

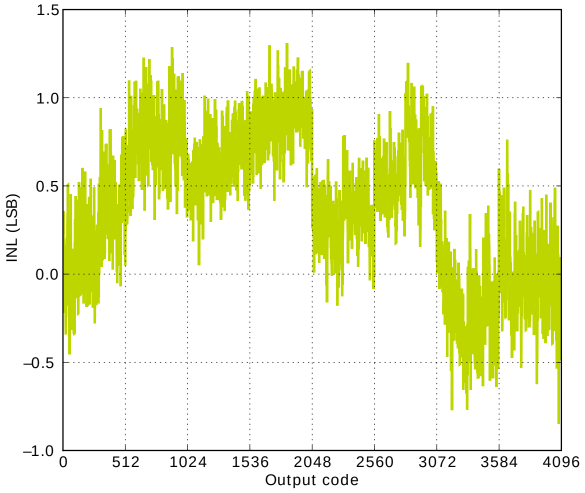


5VDIFF Reference

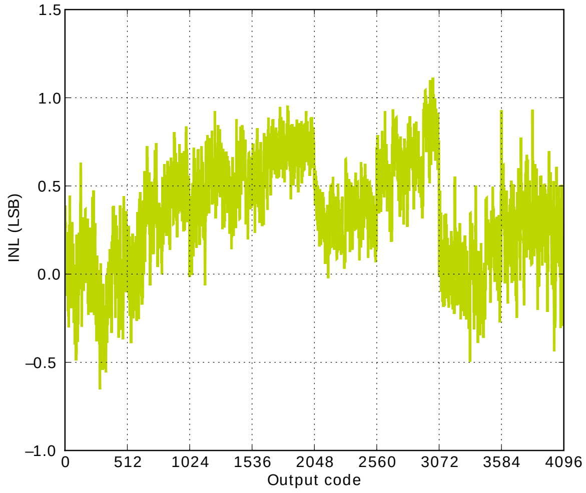


VDD Reference

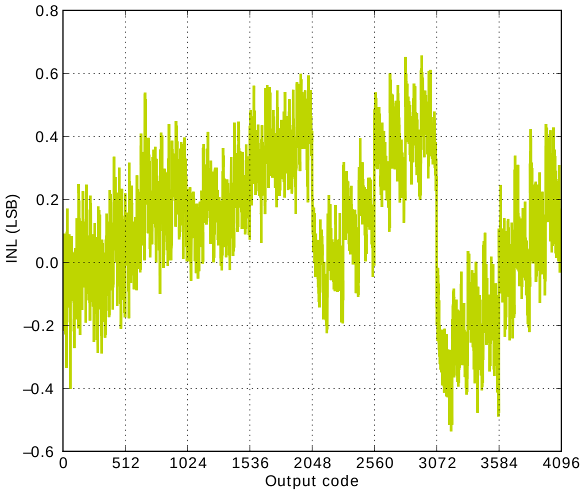
Figure 3.17. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°



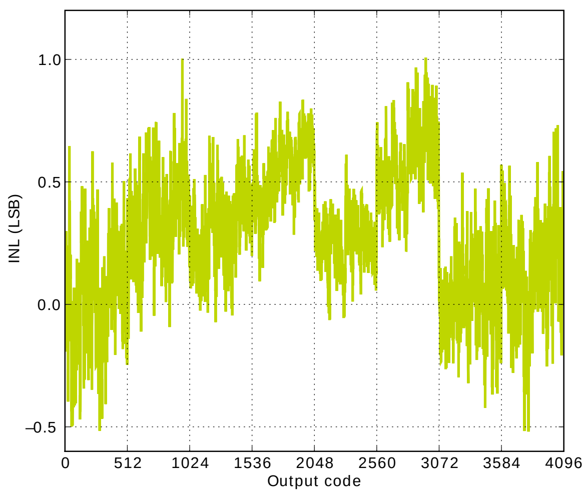
1.25V Reference



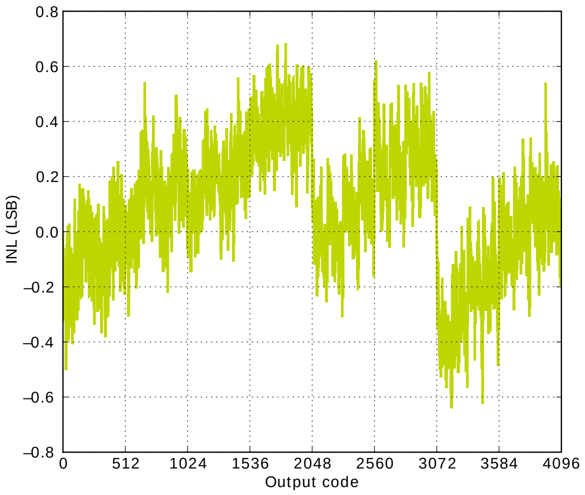
2.5V Reference



2XVDDVSS Reference

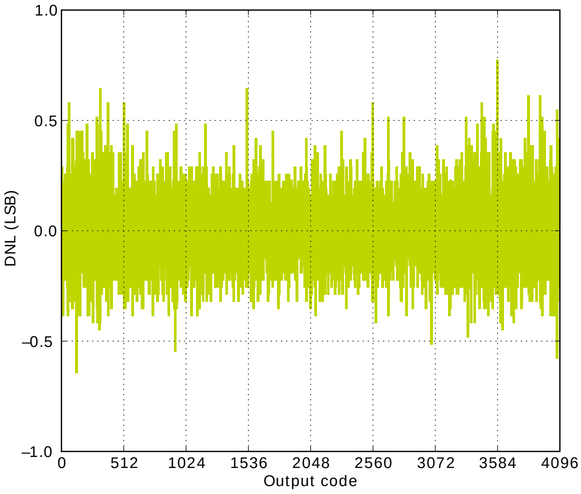


5VDIFF Reference

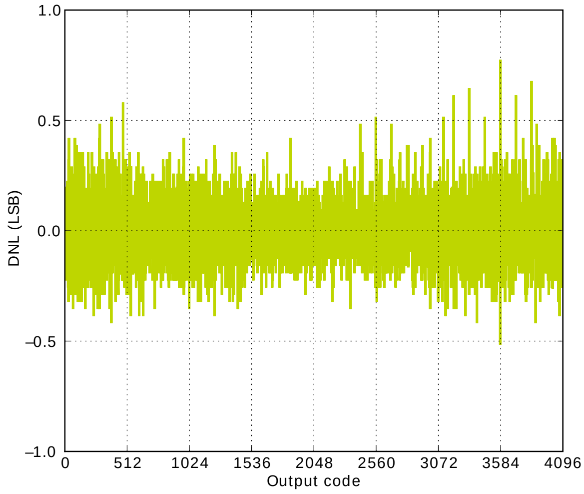


VDD Reference

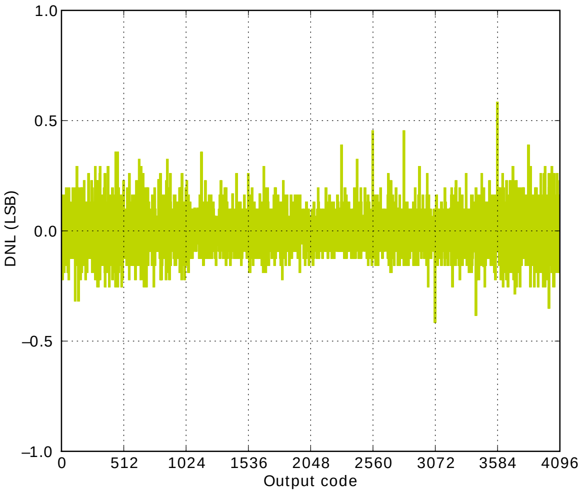
Figure 3.18. ADC Differental Linearity Error vs Code, Vdd = 3V, Temp = 25°



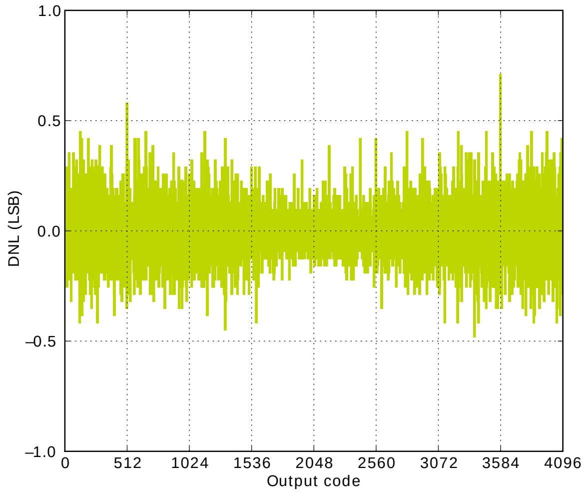
1.25V Reference



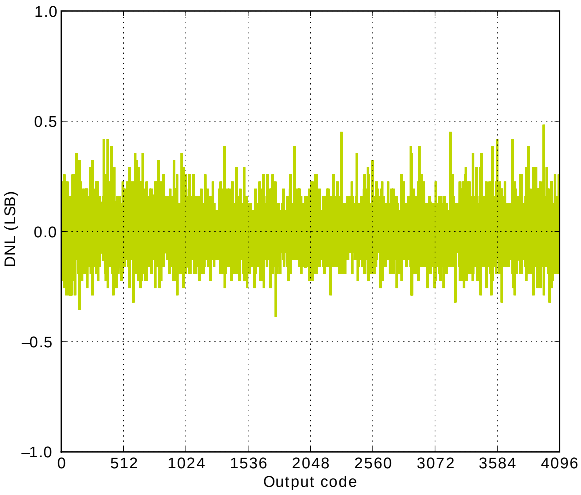
2.5V Reference



2XVDDVSS Reference



5VDIFF Reference



VDD Reference

Figure 3.19. ADC Absolute Offset, Common Mode = Vdd /2

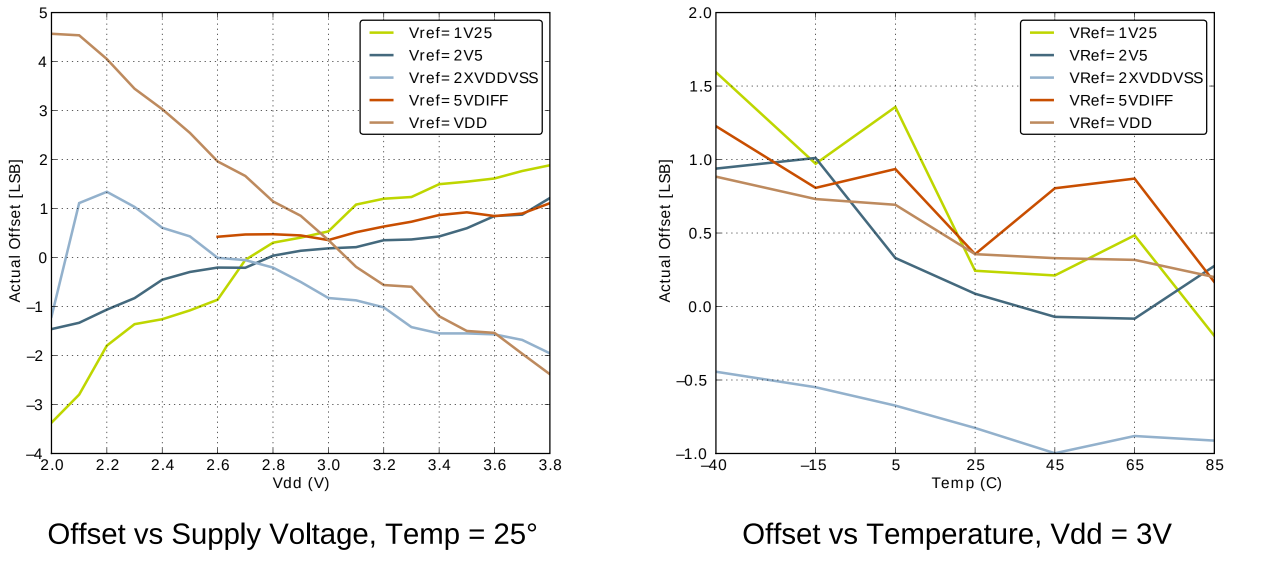


Figure 3.20. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V

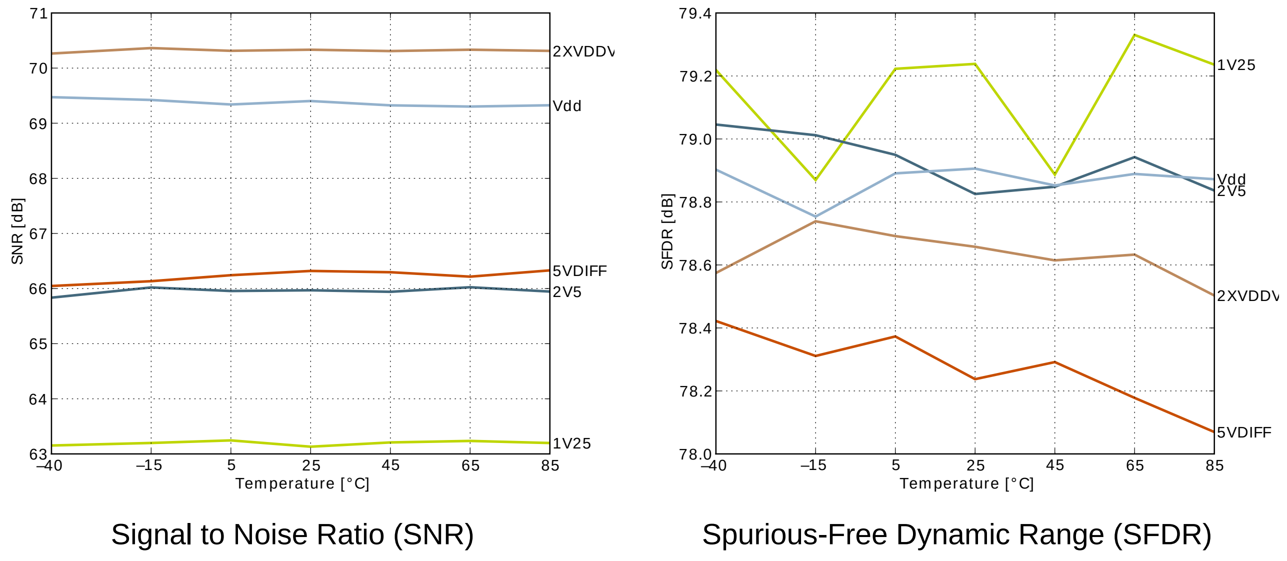
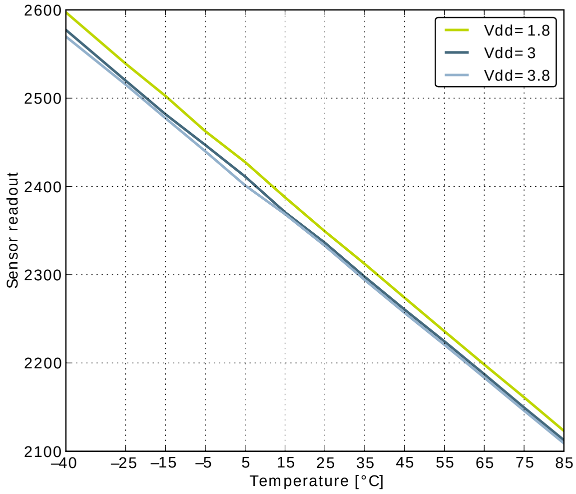


Figure 3.21. ADC Temperature sensor readout



3.11 Analog Comparator (ACMP)

Table 3.15. ACMP

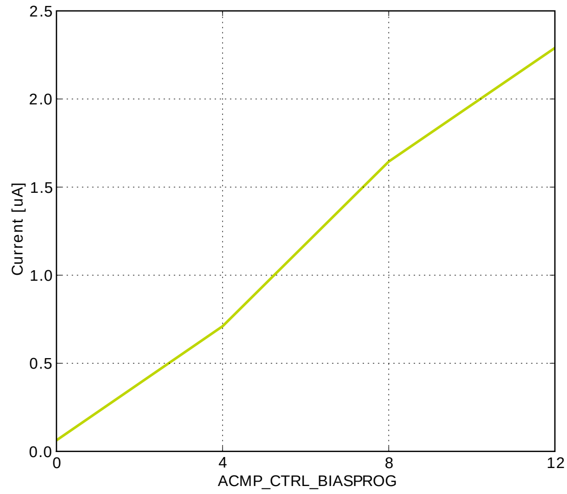
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1		µA
		BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87		µA
		BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195		µA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		µA
		Internal voltage reference		5		µA
$V_{ACMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 35) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

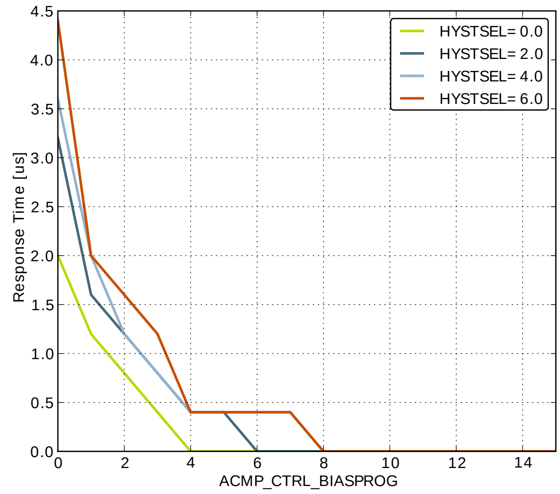
Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

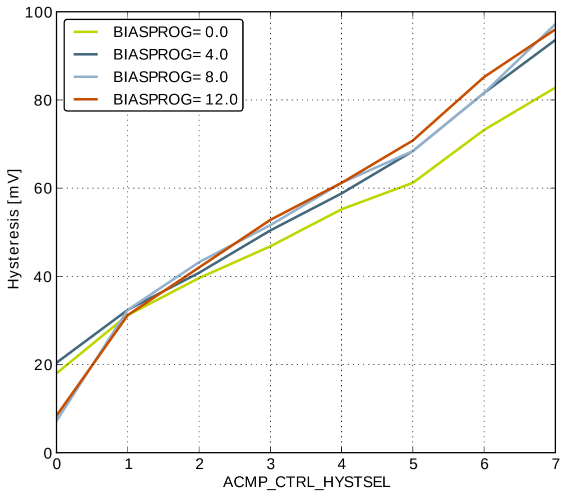
Figure 3.22. Typical ACMP Characteristics



Current consumption



Response time



Hysteresis

3.12 Voltage Comparator (VCMP)

Table 3.16. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCMPIN}	Input voltage range			V_{DD}		V
V_{VCMPCM}	VCMP Common Mode voltage range			V_{DD}		V
I_{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.1		µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		14.7		µA
$t_{VCMPREF}$	Startup time reference generator	NORMAL		10		µs
$V_{VCMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{VCMPHYST}$	VCMP hysteresis			17		mV

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD\ Trigger\ Level}=1.667V+0.034\times TRIGLEVEL \quad (3.2)$$

3.13 Digital Peripherals

Table 3.17. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		7.5		µA/ MHz
I_{I2C}	I2C current	I2C idle current, clock enabled		6.25		µA/ MHz
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		µA/ MHz
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		100		nA
I_{RTC}	RTC current	RTC idle current, clock enabled		100		nA
I_{GPIO}	GPIO current	GPIO idle current, clock enabled		5.31		µA/ MHz
I_{PRS}	PRS current	PRS idle current		2,81		µA/ MHz

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32ZG222.

4.1 Pinout

The *EFM32ZG222* pinout is shown in Figure 4.1 (p. 37) and Table 4.1 (p. 37). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32ZG222 Pinout (top view, not to scale)

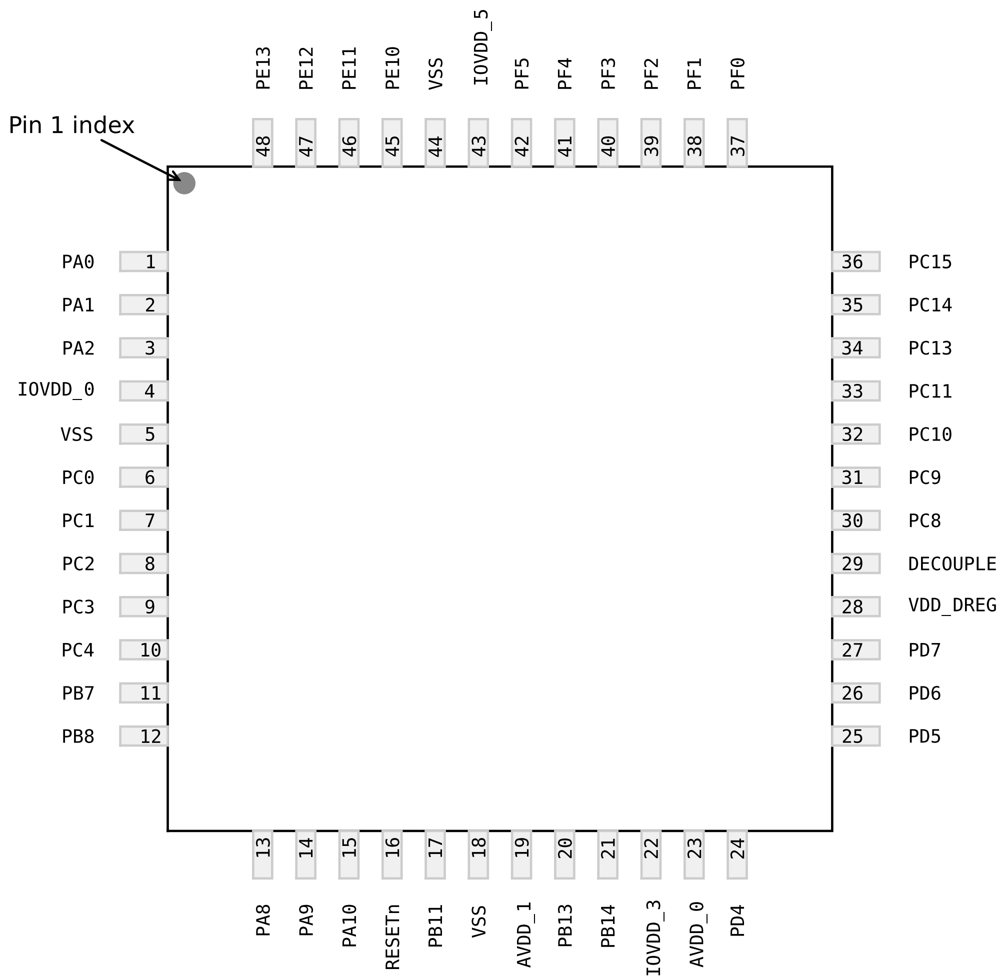


Table 4.1. Device Pinout

QFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0		TIM0_CC0 #0/1/4 TIM1_CC2 #5	US1_CLK #3 LEU0_RX #4 I2C0_SDA #0	CMU_CLK0 #3 PRS_CH0 #0 GPIO_EM4WU0
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0

QFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	IOVDD_0	Digital IO power supply 0.			
5	VSS	Ground			
6	PC0	ACMP0_CH0 #0	TIM0_CC1 #4 PCNT0_S0IN #2	US1_TX #0 I2C0_SDA #4	PRS_CH2 #0
7	PC1	ACMP0_CH1 #0	TIM0_CC2 #4 PCNT0_S1IN #2	US1_RX #0 I2C0_SCL #4	PRS_CH3 #0
8	PC2	ACMP0_CH2 #0			
9	PC3	ACMP0_CH3 #0			
10	PC4	ACMP0_CH4 #0			
11	PB7	LFXTAL_P #0	TIM1_CC0 #3/5	US1_CLK #0	
12	PB8	LFXTAL_N #0	TIM1_CC1 #3/5	US1_CS #0	
13	PA8				
14	PA9				
15	PA10				
16	RESETn	Reset input. Active low, with internal pull-up.			
17	PB11		TIM1_CC2 #3		
18	VSS	Ground			
19	AVDD_1	Analog power supply 1 .			
20	PB13	HFXTAL_P #0	PCNT0_S0IN #5	LEU0_TX #1 I2C0_SDA #7	
21	PB14	HFXTAL_N #0	PCNT0_S1IN #5	LEU0_RX #1 I2C0_SCL #7	
22	IOVDD_3	Digital IO power supply 3.			
23	AVDD_0	Analog power supply 0.			
24	PD4	ADC0_CH4 #0		LEU0_TX #0	
25	PD5	ADC0_CH5 #0		LEU0_RX #0	
26	PD6	ADC0_CH6 #0	TIM1_CC0 #4 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	ACMP0_O #2
27	PD7	ADC0_CH7 #0	TIM1_CC1 #4 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2
28	VDD_DREG	Power supply for on-chip voltage regulator.			
29	DECOUPLE	Decouple output for on-chip voltage regulator, nominally at 1.8 V. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
30	PC8				
31	PC9				GPIO_EM4WU2
32	PC10				
33	PC11				
34	PC13		TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0		
35	PC14		TIM0_CC0 #6 TIM1_CC1 #0 PCNT0_S1IN #0/4	US1_CS #3	

QFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
36	PC15		TIM1_CC2 #0		DBG_SWO #1
37	PF0		TIM0_CC0 #5 PCNT0_S0IN #4	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
38	PF1		TIM0_CC1 #5	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
39	PF2		TIM0_CC2 #5/6	US1_RX #3 LEU0_TX #4	ACMP0_O #1 DBG_SWO #0 GPIO_EM4WU4
40	PF3				PRS_CH0 #1
41	PF4				PRS_CH1 #1
42	PF5				PRS_CH2 #1
43	IOVDD_5	Digital IO power supply 5.			
44	VSS	Ground			
45	PE10		TIM1_CC0 #1		
46	PE11		TIM1_CC1 #1		
47	PE12		TIM0_CC1 #6 TIM1_CC2 #1	US1_TX #3 I2C0_SDA #6	CMU_CLK1 #2/3
48	PE13			I2C0_SCL #6	ACMP0_O #0 GPIO_EM4WU5

4.2 Alternate functionality pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 39). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION								
Functionality	0	1	2	3	4	5	6	7	Description
ACMP0_CH0	PC0								Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1								Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2								Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3								Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4								Analog comparator ACMP0, channel 4.
ACMP0_O	PE13	PF2	PD6						Analog comparator ACMP0, digital output.
ADC0_CH4	PD4								Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5								Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6								Analog to digital converter ADC0, input channel number 6.

Alternate	LOCATION								
Functional-ity	0	1	2	3	4	5	6	7	Description
ADC0_CH7	PD7								Analog to digital converter ADC0, input channel number 7.
CMU_CLK0	PA2		PD7	PA0					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1		PE12	PE12					Clock Management Unit, clock output number 1.
DBG_SWCLK	PF0	PF0	PF0	PF0					Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1					Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15							Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
GPIO_EM4WU0	PA0								Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9								Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1								Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2								Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13								Pin can be used to wake the system up from EM4
HFXTAL_N	PB14								High Frequency Crystal (4 - 32 MHz) negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13								High Frequency Crystal (4 - 32 MHz) positive pin.
I2C0_SCL	PA1	PD7			PC1	PF1	PE13	PB14	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			PC0	PF0	PE12	PB13	I2C0 Serial Data input / output.
LEU0_RX	PD5	PB14		PF1	PA0				LEUART0 Receive input.
LEU0_TX	PD4	PB13		PF0	PF2				LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8								Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7								Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0	PD6	PF0	PB13			Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7	PC14	PB14			Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0	PF3							Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4							Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5							Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1								Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0			PA0	PF0	PC14		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1			PC0	PF1	PE12		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2			PC1	PF2	PF2		Timer 0 Capture Compare input / output channel 2.
TIM1_CC0	PC13	PE10		PB7	PD6	PB7			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7	PB8			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11	PC13	PA0			Timer 1 Capture Compare input / output channel 2.
US1_CLK	PB7		PF0	PA0					USART1 clock input / output.
US1_CS	PB8		PF1	PC14					USART1 chip select input / output.
US1_RX	PC1		PD6	PF2					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).

Alternate	LOCATION								
Functional-ity	0	1	2	3	4	5	6	7	Description
US1_TX	PC0		PD7	PE12					USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

4.3 GPIO pinout overview

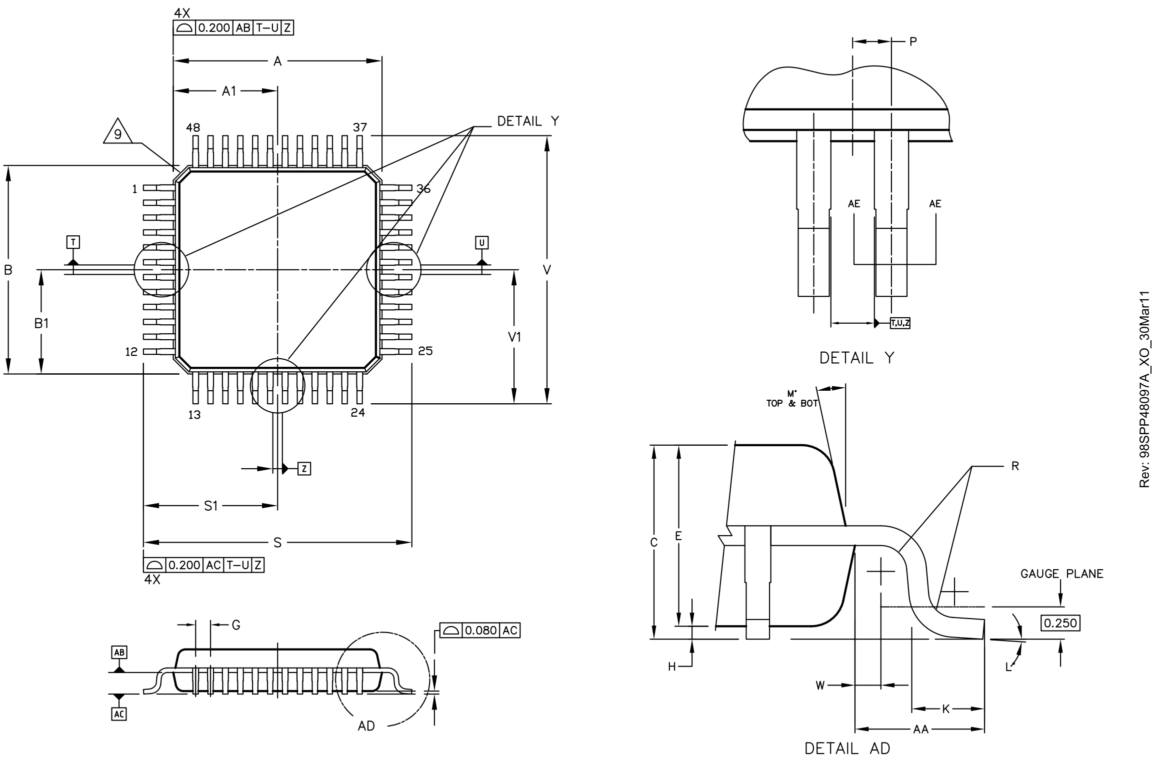
The specific GPIO pins available in *EFM32ZG222* is shown in Table 4.3 (p. 41). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port in indicated by a number from 15 down to 0.

Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	PA10	PA9	PA8	-	-	-	-	-	PA2	PA1	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	PC13	-	PC11	PC10	PC9	PC8	-	-	-	PC4	PC3	PC2	PC1	PC0
Port D	-	-	-	-	-	-	-	-	PD7	PD6	PD5	PD4	-	-	-	-
Port E	-	-	PE13	PE12	PE11	PE10	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	PF5	PF4	PF3	PF2	PF1	PF0

4.4 LQFP48 Package

Figure 4.2. LQFP48



1. Dimensions and tolerance per ASME Y14.5M-1994
2. Control dimension: Millimeter.
3. Datum plane AB is located at bottom of lead and is coincident with the lead where the lead exists from the plastic body at the bottom of the parting line.
4. Datums T, U and Z to be determined at datum plane AB.
5. Dimensions S and V to be determined at seating plane AC.
6. Dimensions A and B do not include mold protrusion. Allowable protrution is 0.250 per side. Dimensions A and B do include mold mismatch and are determined at datum AB.
7. Dimension D does not include dambar protrution. Dambar protrution shall not cause the D dimension to exceed 0.350.
8. Minimum solder plate thickness shall be 0.0076.
9. Exact shape of each corner is optional.

Table 4.4. QFP48 (Dimensions in mm)

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	-	7.000 BSC	-	M	-	12DEG REF	-
A1	-	3.500 BSC	-	N	0.090	-	0.160
B	-	7.000 BSC	-	P	-	0.250 BSC	-
B1	-	3.500 BSC	-	R	0.150	-	0.250
C	1.000	-	1.200	S	-	9.000 BSC	-
D	0.170	-	0.270	S1	-	4.500 BSC	-
E	0.950	-	1.050	V	-	9.000 BSC	-
F	0.170	-	0.230	V1	-	4.500 BSC	-
G	-	0.500 BSC	-	W	-	0.200 BSC	-
H	0.050	-	0.150	AA	-	1.000 BSC	-
J	0.090	-	0.200				
K	0.500	-	0.700				
L	0DEG	-	7DEG				

The LQFP48 Package is 7 by 7 mm in size and has a 0.5 mm pin pitch.

The LQFP48 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

5 PCB Layout and Soldering

5.1 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

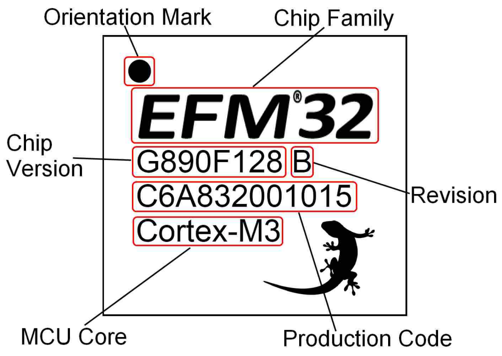
The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions.

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 44). If the revision says "ES" (Engineering Sample), the revision must be read out electronically as specified in the reference manual.

6.3 Errata

No known errata for the EFM32ZG222.

7 Revision History

7.1 Revision 0.30

July 16th, 2011

Updated the Electrical Characteristics section.

7.2 Revision 0.20

June 8th, 2011

Corrected all current values in Electrical Characteristics section.

Updated Cortex M0 related items in the memory map.

Corrected pinout to 37.

7.3 Revision 0.10

June 7th, 2011

Initial preliminary release.

A Disclaimer and Trademarks

A.1 Disclaimer

A.2 Trademark Information

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