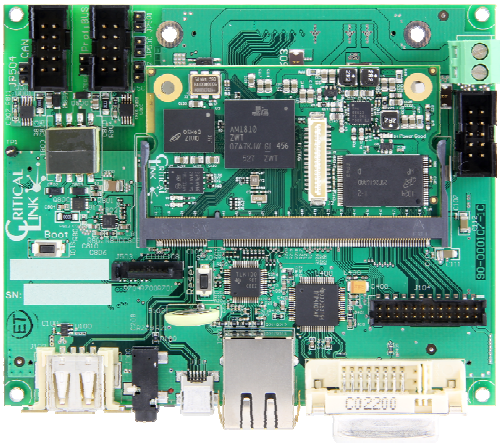
FEATURES

- PROFIBUS Interface
  - Certified by PI International
  - Real-Time Linux Drivers
  - Electrically Isolated Interface
  - Up to 6Mbaud operation
- MityARM-1810 SOM Module
  - Also compatible with MityARM-1810F, MityDSP-L138, and MityDSP-L138F
- Software Included:
  - Real-Time Linux Kernel
  - uBoot
  - User Boot Loader
  - PROFIBUS PRU Image (binary)
  - Slave PROFIBUS Stack (evaluation version)
- Digital Interfaces:
  - RS-232 Serial Interface
  - USB Host Interface
  - USB OTG Interface
  - 10/100 MBit Ethernet Interface
  - Electrically Isolated CAN Bus Interface
  - Electrically Isolated PROFIBUS/RS-485 Interface
  - DVI Video Interface
  - SD/MMC Card Socket
  - Audio Output
- Expansion
  - 3 IO Expansion Slots
  - Integrated +3V/+5V/±12V Power Supply



APPLICATIONS

- MityARM-1810 Evaluation
- PROFIBUS Development
- Process Automation
- Factory Automation
- Industrial Automation
- Embedded Instrumentation
- Rapid Prototyping

DESCRIPTION

The PROFIBUS DEVELOPMENT KIT provides all the hardware and software support for system designers and developers to evaluate the AM1810 Microprocessor for PROFIBUS as well as the Critical Link MityARM-1810 and/or MityARM-1810F. The PROFIBUS DEVELOPMENT KIT comes complete with a MityARM-1810 module, but is fully compatible with MityARM-1810F, MityDSP-L138, and MityDSP-L138F modules as well.

In addition, the PROFIBUS DEVELOPMENT KIT includes on board RS-232, 10/100 MBit Ethernet, Universal Serial Bus (USB) Host and USB-On The-Go (OTG) communication interfaces. Electrically Isolated CAN and PROFIBUS/RS-485 interfaces with 1000V galvanic isolation barrier. Integrated Digital Video Interface (DVI) controller for external display connection with DDC support. Interface to QVGA\WQVGA display via 5 pair LVDS link with additional SPI interface for resistive touch controller (requires an FPGA based module to be installed), Multi Media Card (MMC) interface, 3 I/O Expansion connectors for custom add-on card and integrated power supply with +3V/+5V/±12V outputs from single 12VDC input.

A block diagram of the PROFIBUS DEVELOPMENT KIT is illustrated in Figure 1. All available processor GPIO ports and FPGA I/O lines (if FPGA module is installed) are either used directly by the PROFIBUS DEVELOPMENT KIT or are routed to the Expansion IO connectors. Control of the on-board interface hardware and connected Expansion IO cards require proper configuration of the MityARM / MityDSP ARM, DSP, and FPGA. While not required, it is strongly recommended that the MityARM software and firmware development kit and supplied API be used to manage these interfaces.

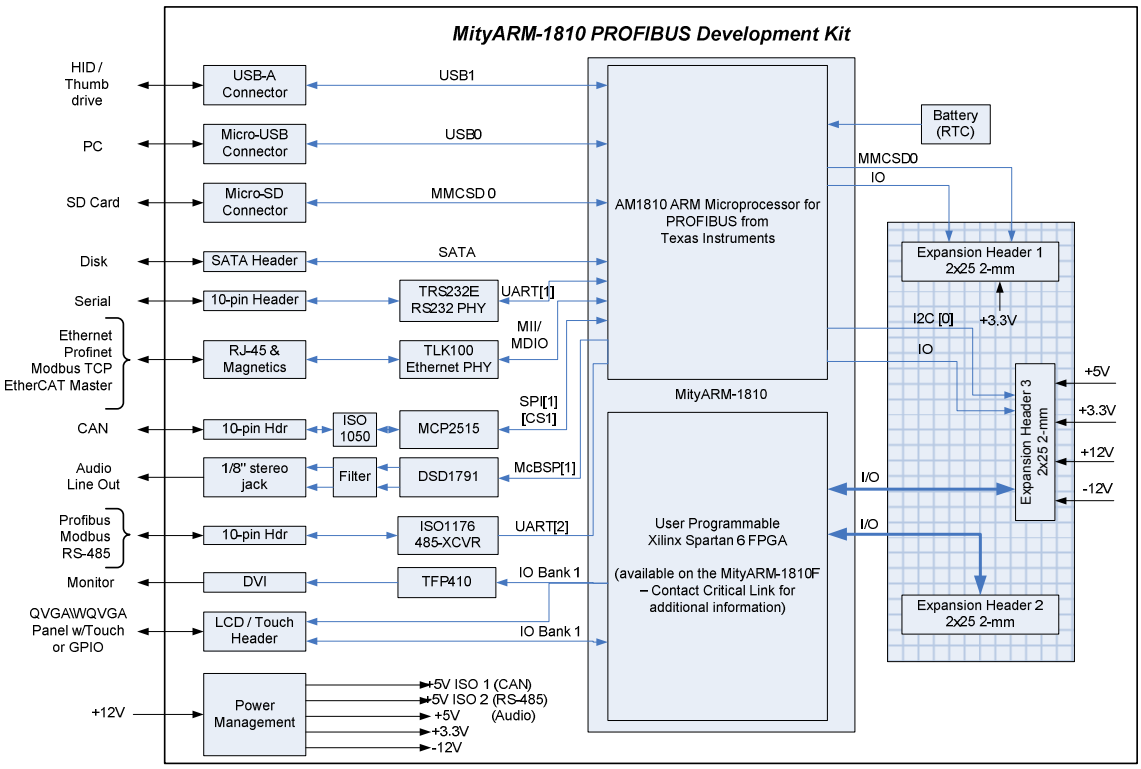


Figure 1: MityARM-1810 PROFIBUS Development Kit Block Diagram

PROFIBUS Interface Description

Texas Instruments Inc. (TI) has integrated PROFIBUS functionality into its AM1810 Sitara ARM microprocessor (MPU). The solution utilizes one of the AM1810 onboard

UARTS and connects directly to the RS-485 transceiver on the PROFIBUS DEVELOPMENT KIT base board and therefore eliminates the need of an external ASIC or FPGA to support the PROFIBUS interface. Customers using the MityARM-1810 in their industrial application can save cost and reduce design complexity as well as PCB space. Furthermore, the industrial application benefits from the low-power architecture of the Sitara ARM MPU and the MityARM-1810 platform from TI and Critical Link.

The AM1810 Sitara ARM MPU PROFIBUS Slave solution has been certified by PROFIBUS International (PI).

The PROFIBUS real-time frame handler (Fieldbus Data Link or FDL) is encapsulated in the Programmable Real-Time Unit Subsystem (PRUSS), which is part of the AM1810 Sitara ARM MPU on-chip peripherals. The PRUSS uses one Universal Asynchronous Receiver/Transmitter (UART) and a timer to generate PROFIBUS-compliant frames. The industrial application and the PROFIBUS DP-Protocol (Layer 7) are operated on the ARM. The solution is completed with an RS-485 transceiver suitable for harsh environments, such as TI's ISO1176 which is found on the PROFIBUS DEVELOPMENT KIT base board to the MityARM-1810.

The PROFIBUS subsystem uses the PRUs that implement real-time frame handling; PROFIBUS message transmission, frame validation and communication with the ARM processor. The PROFIBUS subsystem interfaces with one of the UARTs in the AM1810 Sitara ARM MPU, which is designated for PROFIBUS communication at up to 6Mbaud data rate. The PRU uses interrupts to interact with the ARM where the PROFIBUS stack (Layer 7, DP Protocol) and the industrial application is run. All process data handling like cyclic, acyclic and service access point (SAP) between the PROFIBUS stack on ARM and the PRU is through the internal memory.

Additional details about the AM1810 Sitara ARM MPU, available peripherals and their features are provided in the data sheet at the TI website (www.ti.com/am1810).

RS-232 Interface Description

The on-board RS-232 level driver provides standard serial interface at data rates up to 115,200 baud. The serial interface is routed to the primary MityARM / MityDSP serial bootloading port in order to allow remote code download and FLASH upgrades on an attached MityARM / MityDSP from this connector.

USB Interface Description

The on-board USB interface utilizes dedicated HOST and OTG controllers inside OMAP processor. Linux and drivers are available.

Ethernet Interface Description
The on-board Ethernet interface features a network PHY capable of running at 10/100Mbit including link auto-negotiation and MII/MDIO capability. An industry standard RJ-45 connector is provided for external connection. This Ethernet interface may be used to perform remote code download and FLASH upgrades on an attached MityARM or MityDSP module.

QVGA/WQVGA Interface Description
The PROFIBUS DEVELOPMENT KIT provides a flat-ribbon cable low profile interface for five Low Voltage Differential Signaling (LVDS) pairs. The interface design is intended to support high speed off board interconnects. In addition to custom user interfacing, the pairs may be used to interface to a Quarter VGA LCD screen using the MityARM / MityDSP hardware and software development kit LCD interface libraries and an appropriate daughterboard interface. Off-the-shelf display solutions for QVGA\WQVGA interfaces are provided by Critical Link.

The interface can also be customized to support 17 IO lines at +3.3V CMOS/LVTTL signaling levels based on FPGA configuration.

This interface is available only with an FPGA based MityARM or MityDSP module installed.

DVI Interface Description
The PROFIBUS DEVELOPMENT KIT provides a standard DVI interface for external monitor connection. Based on CPU utilization, recommended resolution should be limited to VGA (640x480) with 5-6-5 color pallet.

CAN Interface Description
The on-board CAN provides a CAN V2.0B compliant interface. This interface is managed by a Microchip MCP2515 CAN controller connected to MityARM / MityDSP via the SPI1 interface.

The galvanic isolation is provided by a dedicated TI ISO1050 transceiver. The ISO1050 is powered by an isolated power supply with 1000V* isolation from the primary supply.

Jumper JP504 can provide dedicated bus termination of 120Ohm. To enable termination, place shorting jumper across JP504.

The Electrical interface is provided via J501, 10-pin shrouded header.

Linux Driver and API examples are available to support CAN functionality.

PROFIBUS / RS-485 Interface Description

The on-board PROFIBUS/RS-485 provides standard serial interface at data rates up to 115,200 baud. The serial interface is routed to the UART2 serial port of MityARM / MityDSP.

The galvanic isolation is provided by a dedicated TI ISO1176 transceive. The ISO1176 is powered by an isolated power supply with 1000V* isolation from the primary supply.

Jumpers JP500-503 can provide dedicated bus termination. If the interface is to be configured to support PROFIBUS, JP500-502 should be installed and JP503 should be removed, in the RS-485 configuration JP500-502 should be removed and JP503 installed.

The Electrical interface provided via J504, 10-pin shrouded header

Linux Driver and API examples are available to support PROFIBUS/RS-485 functionality.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage	13.2 V
Storage Temperature Range	0 to 80C
Shock, Z-Axis	±10 g
Shock, X/Y-Axis	±10 g

OPERATING CONDITIONS

Ambient Temperature Range	0 to 55C
Humidity	0 to 95% Non-condensing
Vibration, Z-Axis	TBS
Vibration, X/Y-Axis	TBS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
Power Dissipation					
V_S	Supply Voltage.		12±5%		V
I_S	Supply Current		0.45[1]		A
MDK-8 Digital I/O					
$F_{clk,din}$	Clock Frequency, Digital Inputs		25	25	MHz
$T_{update,din}$	Update Period, Digital Inputs		1680	1680	ns
$F_{clk,dout}$	Clock Frequency, Digital Output LVDS clk entering deserializer		50	20 / 68	MHz (Min/Max)
$T_{update,dout}$	Update Period, Digital Outputs		20	14.7 / 50	ns (Min/Max)
Notes:	1. Power Supply load is dependent on Daughter Card configuration and utilization.				

Notes: 1. Expansion card is not attached, 100% DSP/FPGA utilization, RS-232 and Ethernet are enabled and active.

ELECTRICAL INTERFACE DESCRIPTION

Input Power

The PROFIBUS DEVELOPMENT KIT power interface, J600, requires a single +12Volt power supply.

Table 1: Input Power Interface Pin Description

Signal	J600 Position
+12V	1
GND	2

Auxiliary / LVDS Interface

The Auxiliary / LVDS interface connector provides up to 5 pairs of LVDS signals connected to the Spartan 6 device on a connected MityARM / MityDSP (modules with FPGA only). The interface use a standard 2mm 24 position male header. Table 3 defines the LVDS connector pinout when an FPGA enabled module is installed, Table 2 defines the pinout for Auxiliary interfaces from the module when a non-FPGA module is installed. In this case the signals are routed directly from the AM1810 or OMAP-L138 to this connector.

A cable using AMP® TBD connector (or equivalent) should be used. Use of the LVDS pairs as outputs will require addition of termination resistors (100 Ohm) on externally designed circuit assemblies. Use of the LVDS pairs as inputs will require population of 0603 sized termination resistors on the PROFIBUS DEVELOPMENT KIT on the provided solder pads. Refer to the detailed schematic and assembly drawing for further information.

Table 2: J104 Aux / LVDS Interface Pin Description – MityARM-1810 Installed

Pin	Signal	Type	Standard	Notes
1	+5 V	Power	-	500 mA Max.
2	+5 V	Power	-	500 mA Max.
3	GND	Power	-	
4	GND	Power	-	
5	VP_CLKOUT3	I/O	3.3V LVCMOS	Software configurable OMAP IO
6	LCD_MCLK	I/O	3.3V LVCMOS	Software configurable OMAP IO
7	RESET_OUT	I/O	3.3V LVCMOS	Software configurable OMAP IO
8	VP_CLKIN3	I/O	3.3V LVCMOS	Software configurable OMAP IO
9	EMA_CS4	I/O	3.3V LVCMOS	Software configurable OMAP IO
10	EMA_CS5	I/O	3.3V LVCMOS	Software configurable OMAP IO
11	EMA_RAS	I/O	3.3V LVCMOS	Software configurable OMAP IO
12	EMA_CS2	I/O	3.3V LVCMOS	Software configurable OMAP IO
13	GND	Power	-	
14	GND	Power	-	
15	EMA_WE	I/O	3.3V LVCMOS	Software configurable OMAP IO
16	EMA_CAS	I/O	3.3V LVCMOS	Software configurable OMAP IO
17	GND	Power	-	
18	EMA_D11	I/O	3.3V LVCMOS	Software configurable OMAP IO
19	EMA_D12	I/O	3.3V LVCMOS	Software configurable OMAP IO
20	EMA_D13	I/O	3.3V LVCMOS	Software configurable OMAP IO
21	EMA_D14	I/O	3.3V LVCMOS	Software configurable OMAP IO
22	EMA_A12	I/O	3.3V LVCMOS	Software configurable OMAP IO
23	EMA_D15	I/O	3.3V LVCMOS	Software configurable OMAP IO
24	EMA_A13	I/O	3.3V LVCMOS	Software configurable OMAP IO

Note that these signals are pin-muxed in the CPU and may be available for a variety of functions.

Table 3: J104 Aux / LVDS Interface Pin Description – MityARM-1810F (with FPGA) Installed

Pin	Signal	Type	Standard	Notes
1	+5 V	-	-	500 mA Max.
2	+5 V	-	-	500 mA Max.
3	GND	-	-	
4	GND	-	-	
5	DISP_A0_P	I/O	LVDS	Display/LVDS Data channel 0
6	DISP_A0_N	I/O	LVDS	Display/LVDS Data channel 0
7	DISP_A1_P	I/O	LVDS	Display/LVDS Data channel 1
8	DISP_A1_N	I/O	LVDS	Display/LVDS Data channel 1
9	DISP_A2_P	I/O	LVDS	Display/LVDS Data channel 2
10	DISP_A2_N	I/O	LVDS	Display/LVDS Data channel 2
11	DISP_A3_P	I/O	LVDS	Display/LVDS Data channel 3
12	DISP_A3_N	I/O	LVDS	Display/LVDS Data channel 3
13	GND	-	-	
14	GND	-	-	
15	DISP_CLKIN_P	I/O	LVDS	Display/LVDS Clock (or Data)
16	DISP_CLKIN_N	I/O	LVDS	Display/LVDS Clock (or Data)
17	GND	-	-	
18	SPARE IO	I/O	CMOS	Display Aux. I/O
19	DISP_I2	I	CMOS	Display Touch-screen Input 2
20	DISP_I1	I	CMOS	Display Touch-screen Input 1
21	DISP_I0	I	CMOS	Display Touch-screen Input 0
22	DISP_O2	O	CMOS	Display Touch-screen Output 2
23	DISP_O1	O	CMOS	Display Touch-screen Output 1
24	DISP_O0	O	CMOS	Display Touch-screen Output 0

Alternatively all IO can be configured as 3.3V CMOS and LVTTL IO

Expansion IO Interface

The PROFIBUS DEVELOPMENT KIT provides three expansion IO connectors. Each connector includes one 50 position dual row receptacle. Mating connectors for these receptacles is a 2x25 2mm male header.

Table 4, Table 5, and Table 7provide signal descriptions for each pin when a MityARM-1810 is installed.

Table 4, Table 6 and Table 8 provides signals description for each pin when a MityARM-1810F is installed. The MityARM-1810F module is identical to the MityARM-1810 with the exception that it also includes an on-board, user programmable Spartan-6 FPGA.
6 provides the electrical standards for the various nets.

Table 4: J700 Connector Pin Assignments – MityARM-1810 or MityARM-1810F (with or without FPGA)

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	GND	Power		
4	GND	Power		
5	+3.3V	Power		250mA Max (Per pin)
6	+3.3V	Power		250mA Max (Per pin)
7	+3.3V	Power		250mA Max (Per pin)
8	+3.3V	Power		250mA Max (Per pin)
9	RESERVED			
10	RESERVED			
11	RESERVED			
12	RESERVED			
13	RESERVED			
14	RESERVED			
15	RESERVED			
16	RESERVED			
17	RESERVED			
18	RESERVED			
19	OMAP_GP0_7	I/O	3.3V LVCMOS	Software configurable GPIO
20	OMAP_GP0_15	I/O	3.3V LVCMOS	Software configurable GPIO
21	OMAP_GP0_13	I/O	3.3V LVCMOS	Software configurable GPIO
22	OMAP_GP0_6	I/O	3.3V LVCMOS	Software configurable GPIO
23	MMCSD0_CLK		3.3V LVCMOS	MMC Interface Clock
24	MMCSD0_CMD		3.3V LVCMOS	MMC Interface Command\ata
25	MMCSD0_DAT0		3.3V LVCMOS	MMC Interface Data Bit 0
26	MMCSD0_DAT3		3.3V LVCMOS	MMC Interface Data Bit 3
27	MMCSD0_DAT1		3.3V LVCMOS	MMC Interface Data Bit 1
28	MMCSD0_DAT2		3.3V LVCMOS	MMC Interface Data Bit
29	SPI1_SCS0	I/O	3.3V LVCMOS	Software configurable GPIO
30	RESERVED			
31	RESERVED			
32	RESERVED			
33	RESERVED			
34	RESERVED			
35	RESERVED			
36	RESERVED			
37	RESERVED			
38	RESERVED			
39	RESERVED			
40	RESERVED			
41	RESERVED			
42	RESERVED			
43	RESERVED			
44	GND	Power		
45	RESERVED			
46	GND	Power		
47	GND	Power		
48	GND	Power		
49	GND	Power		
50	GND	Power		

Note that these signals are pin-muxed in the CPU and may be available for a variety of functions.

Table 5: J701 Connector Pin Assignments – MityARM-1810 Installed

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	VP_CLKIN1		3.3V LVCMOS	Software configurable OMAP IO
4	UPP_CH1_START		3.3V LVCMOS	Software configurable OMAP IO
5	UPP_CH1_D14 / RMII_TXD0		3.3V LVCMOS	Software configurable OMAP IO
6	UPP_CH1_D15 / RMII_TXD1		3.3V LVCMOS	Software configurable OMAP IO
7	UPP_CH1_D12 / RMII_RXD1		3.3V LVCMOS	Software configurable OMAP IO
8	UPP_CH1_D13 / RMII_TXEN		3.3V LVCMOS	Software configurable OMAP IO
9	UPP_CH1_D10 / RMII_RXER		3.3V LVCMOS	Software configurable OMAP IO
10	UPP_CH1_D11 / RMII_RXD0		3.3V LVCMOS	Software configurable OMAP IO
11	UPP_CH1_D8 / RMII_CRS_DV		3.3V LVCMOS	Software configurable OMAP IO
12	UPP_CH1_D9 / RMII_REF_CLK		3.3V LVCMOS	Software configurable OMAP IO
13	UPP_CH1_D6		3.3V LVCMOS	Software configurable OMAP IO
14	UPP_CH1_D7		3.3V LVCMOS	Software configurable OMAP IO
15	GND	Power		
16	GND	Power		
17	OMAP_GP0_7	I/O	3.3V LVCMOS	Software configurable OMAP IO
18	OMAP_GP0_15	I/O	3.3V LVCMOS	Software configurable OMAP IO
19	OMAP_GP0_6	I/O	3.3V LVCMOS	Software configurable OMAP IO
20	OMAP_GP0_13	I/O	3.3V LVCMOS	Software configurable OMAP IO
21	OMAP_GP0_1	I/O	3.3V LVCMOS	Software configurable OMAP IO
22	OMAP_GP0_4	I/O	3.3V LVCMOS	Software configurable OMAP IO
23	OMAP_GP0_3	I/O	3.3V LVCMOS	Software configurable OMAP IO
24	OMAP_GP0_2	I/O	3.3V LVCMOS	Software configurable OMAP IO
25	OMAP_GP0_0	I/O	3.3V LVCMOS	Software configurable OMAP IO
26	OMAP_GP0_8	I/O	3.3V LVCMOS	Software configurable OMAP IO
27	I2C0_SDA[3]	I/O	3.3V LVCMOS	Software configurable OMAP IO
28	I2C0_SCL[3]	I/O	3.3V LVCMOS	Software configurable OMAP IO
29	GND	Power		
30	GND	Power		
31	GND	Power		
32	GND	Power		
33	-12V[4]	Power		250mA Max (Per pin)
34	-12V[4]	Power		250mA Max (Per pin)
35	-12V[4]	Power		250mA Max (Per pin)
36	-12V[4]	Power		250mA Max (Per pin)
37	+3.3V[4]	Power		250mA Max (Per pin)
38	+3.3V[4]	Power		250mA Max (Per pin)
39	+3.3V[4]	Power		250mA Max (Per pin)
40	+3.3V[4]	Power		250mA Max (Per pin)
41	+5V[4]	Power		250mA Max (Per pin)
42	+5V[4]	Power		250mA Max (Per pin)
43	+5V[4]	Power		250mA Max (Per pin)
44	+5V[4]	Power		250mA Max (Per pin)
45	+12V[4]	Power		250mA Max (Per pin)
46	+12V[4]	Power		250mA Max (Per pin)
47	+12V[4]	Power		250mA Max (Per pin)
48	+12V[4]	Power		250mA Max (Per pin)
49	GND	Power		
50	GND	Power		

Note that these signals are pin-muxed in the CPU and may be available for a variety of functions.

Table 6: J701 Connector Pin Assignments - MityARM-1810F (with FPGA) Installed

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	FPGA_IO_48_N[1,2]			Hardware Configurable FPGA IO
4	FPGA_IO_48_P[1,2]			Hardware Configurable FPGA IO
5	FPGA_IO_46_N[1,2]			Hardware Configurable FPGA IO
6	FPGA_IO_46_P[1,2]			Hardware Configurable FPGA IO
7	FPGA_IO_44_N[1,2]			Hardware Configurable FPGA IO
8	FPGA_IO_44_P[1,2]			Hardware Configurable FPGA IO
9	FPGA_IO_42_N[1,2]			Hardware Configurable FPGA IO
10	FPGA_IO_42_P[1,2]			Hardware Configurable FPGA IO
11	FPGA_IO_40_N[1,2]			Hardware Configurable FPGA IO
12	FPGA_IO_40_P[1,2]			Hardware Configurable FPGA IO
13	FPGA_IO_38_N[1,2]			Hardware Configurable FPGA IO
14	FPGA_IO_38_P[1,2]			Hardware Configurable FPGA IO
15	GND	Power		
16	GND	Power		
17	OMAP_GP0_7	I/O	3.3V LVCMOS	Software configurable GPIO
18	OMAP_GP0_15	I/O	3.3V LVCMOS	Software configurable GPIO
19	OMAP_GP0_6	I/O	3.3V LVCMOS	Software configurable GPIO
20	OMAP_GP0_13	I/O	3.3V LVCMOS	Software configurable GPIO
21	OMAP_GP0_1	I/O	3.3V LVCMOS	Software configurable GPIO
22	OMAP_GP0_4	I/O	3.3V LVCMOS	Software configurable GPIO
23	OMAP_GP0_3	I/O	3.3V LVCMOS	Software configurable GPIO
24	OMAP_GP0_2	I/O	3.3V LVCMOS	Software configurable GPIO
25	OMAP_GP0_0	I/O	3.3V LVCMOS	Software configurable GPIO
26	OMAP_GP0_8	I/O	3.3V LVCMOS	Software configurable GPIO
27	I2C0_SDA[3]	I/O	3.3V LVCMOS	Software configurable GPIO
28	I2C0_SCL[3]	I/O	3.3V LVCMOS	Software configurable GPIO
29	GND	Power		
30	GND	Power		
31	GND	Power		
32	GND	Power		
33	-12V[4]	Power		250mA Max (Per pin)
34	-12V[4]	Power		250mA Max (Per pin)
35	-12V[4]	Power		250mA Max (Per pin)
36	-12V[4]	Power		250mA Max (Per pin)
37	+3.3V[4]	Power		250mA Max (Per pin)
38	+3.3V[4]	Power		250mA Max (Per pin)
39	+3.3V[4]	Power		250mA Max (Per pin)
40	+3.3V[4]	Power		250mA Max (Per pin)
41	+5V[4]	Power		250mA Max (Per pin)
42	+5V[4]	Power		250mA Max (Per pin)
43	+5V[4]	Power		250mA Max (Per pin)
44	+5V[4]	Power		250mA Max (Per pin)
45	+12V[4]	Power		250mA Max (Per pin)
46	+12V[4]	Power		250mA Max (Per pin)
47	+12V[4]	Power		250mA Max (Per pin)
48	+12V[4]	Power		250mA Max (Per pin)
49	GND	Power		
50	GND	Power		

Notes:
[1] 3.3V CMOS or 3.3V LVTTL Standard signal levels.
[2] <signal_name>_N/_P can be configured as a differential pair or single-ended FPGA I/O
[3] The I2C bus controlled by MityARM / MityDSP hardware. Slave address 0x90 reserved for Power Management Controller IC. User should not attempt to write any data to this address as it will result in module damage.
[4] Maximum current per power bus should be limited to 1.0Amp, it is advised to have input fuses on expansion board.

Table 7: J702 Connector Pin Assignments - MityARM-1810 Installed

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	UPP_CH1_D5	I/O	3.3V LVCMOS	Software configurable OMAP IO
4	UPP_CH1_ENABLE	I/O	3.3V LVCMOS	Software configurable OMAP IO
5	UPP_CH1_D3	I/O	3.3V LVCMOS	Software configurable OMAP IO
6	UPP_CH1_D4	I/O	3.3V LVCMOS	Software configurable OMAP IO
7	UPP_CH1_WAIT	I/O	3.3V LVCMOS	Software configurable OMAP IO
8	UPP_CH1_D2	I/O	3.3V LVCMOS	Software configurable OMAP IO
9	UPP_CH1_D0	I/O	3.3V LVCMOS	Software configurable OMAP IO
10	UPP_CH1_D1	I/O	3.3V LVCMOS	Software configurable OMAP IO
11	UPP_CH0_ENABLE	I/O	3.3V LVCMOS	Software configurable OMAP IO
12	UPP_CH1_CLK	I/O	3.3V LVCMOS	Software configurable OMAP IO
13	VP_CLKIN2	I/O	3.3V LVCMOS	Software configurable OMAP IO
14	VP_CLKOUT2	I/O	3.3V LVCMOS	Software configurable OMAP IO
15	UPP_CH0_START	I/O	3.3V LVCMOS	Software configurable OMAP IO
16	UPP_CH0_WAIT	I/O	3.3V LVCMOS	Software configurable OMAP IO
17	VP_CLKIN0	I/O	3.3V LVCMOS	Software configurable OMAP IO
18	UPP_CH0_CLK	I/O	3.3V LVCMOS	Software configurable OMAP IO
19	EMA_OE	I/O	3.3V LVCMOS	Software configurable OMAP IO
20	EMA_CS0	I/O	3.3V LVCMOS	Software configurable OMAP IO
21	EMA_BA1	I/O	3.3V LVCMOS	Software configurable OMAP IO
22	EMA_BA0	I/O	3.3V LVCMOS	Software configurable OMAP IO
23	EMA_A1	I/O	3.3V LVCMOS	Software configurable OMAP IO
24	EMA_A0	I/O	3.3V LVCMOS	Software configurable OMAP IO
25	EMA_A3	I/O	3.3V LVCMOS	Software configurable OMAP IO
26	EMA_A1	I/O	3.3V LVCMOS	Software configurable OMAP IO
27	EMA_A5	I/O	3.3V LVCMOS	Software configurable OMAP IO
28	EMA_A4	I/O	3.3V LVCMOS	Software configurable OMAP IO
29	EMA_A11	I/O	3.3V LVCMOS	Software configurable OMAP IO
30	EMA_A10	I/O	3.3V LVCMOS	Software configurable OMAP IO
31	EMA_A9	I/O	3.3V LVCMOS	Software configurable OMAP IO
32	EMA_A8	I/O	3.3V LVCMOS	Software configurable OMAP IO
33	EMA_A7	I/O	3.3V LVCMOS	Software configurable OMAP IO
34	EMA_A6	I/O	3.3V LVCMOS	Software configurable OMAP IO
35	EMA_D8	I/O	3.3V LVCMOS	Software configurable OMAP IO
36	EMA_D9	I/O	3.3V LVCMOS	Software configurable OMAP IO
37	Reserved	I/O	3.3V LVCMOS	Software configurable OMAP IO
38	Reserved	I/O	3.3V LVCMOS	Software configurable OMAP IO
39	EMA_CLK	I/O	3.3V LVCMOS	Software configurable OMAP IO
40	EMA_SDCKE	I/O	3.3V LVCMOS	Software configurable OMAP IO
41	EMA_WEN_DQM1	I/O	3.3V LVCMOS	Software configurable OMAP IO
42	EMA_WEN_DQM0	I/O	3.3V LVCMOS	Software configurable OMAP IO
43	EMA_D0	I/O	3.3V LVCMOS	Software configurable OMAP IO
44	EMA_D1	I/O	3.3V LVCMOS	Software configurable OMAP IO
45	EMA_D2	I/O	3.3V LVCMOS	Software configurable OMAP IO
46	EMA_D3	I/O	3.3V LVCMOS	Software configurable OMAP IO
47	EMA_D4	I/O	3.3V LVCMOS	Software configurable OMAP IO
48	EMA_D5	I/O	3.3V LVCMOS	Software configurable OMAP IO
49	GND	Power		
50	GND	Power		

Table 8: J702 Connector Pin Assignments - MityARM-1810F (with FPGA) Installed

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	FPGA_IO_36_N[1]	I/O	LVDS, 3.3V LVCMOS/LVTTL	
4	FPGA_IO_36_P[1]	I/O	LVDS, 3.3V LVCMOS/LVTTL	
5	FPGA_IO_34_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
6	FPGA_IO_34_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
7	FPGA_IO_32_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
8	FPGA_IO_32_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
9	FPGA_IO_30_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
10	FPGA_IO_30_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
11	FPGA_IO_28_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
12	FPGA_IO_28_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
13	FPGA_IO_26_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
14	FPGA_IO_26_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
15	FPGA_IO_24_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
16	FPGA_IO_24_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
17	FPGA_IO_2_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
18	FPGA_IO_2_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
19	FPGA_IO_4_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
20	FPGA_IO_4_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
21	FPGA_IO_6_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
22	FPGA_IO_6_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
23	FPGA_IO_8_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
24	FPGA_IO_8_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
25	FPGA_IO_10_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
26	FPGA_IO_10_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
27	FPGA_IO_12_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
28	FPGA_IO_12_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
29	FPGA_IO_14_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
30	FPGA_IO_14_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
31	FPGA_IO_16_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
32	FPGA_IO_16_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
33	FPGA_IO_18_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
34	FPGA_IO_18_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
35	FPGA_IO_20_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
36	FPGA_IO_20_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
37	FPGA_IO_22_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
38	FPGA_IO_22_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
39	FPGA_IO_1_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
40	FPGA_IO_1_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
41	FPGA_IO_3_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
42	FPGA_IO_3_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
43	FPGA_IO_5_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
44	FPGA_IO_5_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
45	FPGA_IO_7_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
46	FPGA_IO_7_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
47	FPGA_IO_9_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
48	FPGA_IO_9_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
49	GND	Power		
50	GND	Power		

Notes:
[1] <signal_name>_N/_P can be configured as a differential pair or single-ended FPGA IO.

Signal Naming Description

Table 9: Daughter Card Signal Description

Signal	Type	Standard	Notes
FPGA_IO_##_N/P	I/O	LVDS/3.3V CMOS/ 3.3V LVTTL	Direct Interface to MityARM / MityDSP Spartan6 FPGA.
OMAP_GP0_##	I/O	3.3V CMOS	Direct Interface to MityARM / MityDSP processor
DO_##	O	3.3V CMOS	Digital Output. Update Rate of 20 nsec. DO_CLK provides sampling clock – outputs should be sampled on rising edge.
DI_##	I	3.3V CMOS	Digital Input. Sampling interval < 2 µs.

CAN Interface

Table 10: J501 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	RESERVED			
2	CANL	I/O		CAN Bus Signal L
3	GND	Power		CAN Bus Isolated Ground
4	RESERVED			
5	RESERVED			
6	RESERVED			
7	CANH	I/O		CAN Bus Signal H
8	RESERVED			
9	+5V	Power		Isolated +5V Output, 20mA Max
10	RESERVED			

Notes: please see Figure 2 for physical pin-out of connector

ProfiBus/RS-485 Interface

Table 11: J504 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	RESERVED			
2	RESERVED			
3	A	I/O		RS-485 Bus - Signal A
4	RESERVED			
5	GND	Power		RS-485 Bus Isolated Ground
6	+5V	Power		Isolated +5V Output, 20mA Max
7	RESERVED			
8	B	I/O		RS-485 Bus - Signal B
9	RESERVED			
10	RESERVED			

Notes: please see Figure 2 for physical pin-out of connector

RS-232 Interface

Table 12: J502 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	RESERVED			
2	RS232_RX	I		RS232-level Input Signal
3	RS232_TX	O		RS232-level Output Signal
4	RESERVED			
5	GND	Power		RS-232 Ground
6	RESERVED			
7	RESERVED			
8	RESERVED			
9	RESERVED			
10	RESERVED			

Notes: please see Figure 2 for physical pin-out of connector

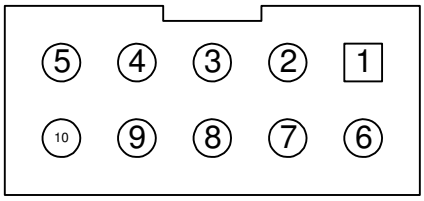


Figure 2: J501, J502, J504 Pin-out (Top View)

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

Board mounting is compatible to ETX standard.

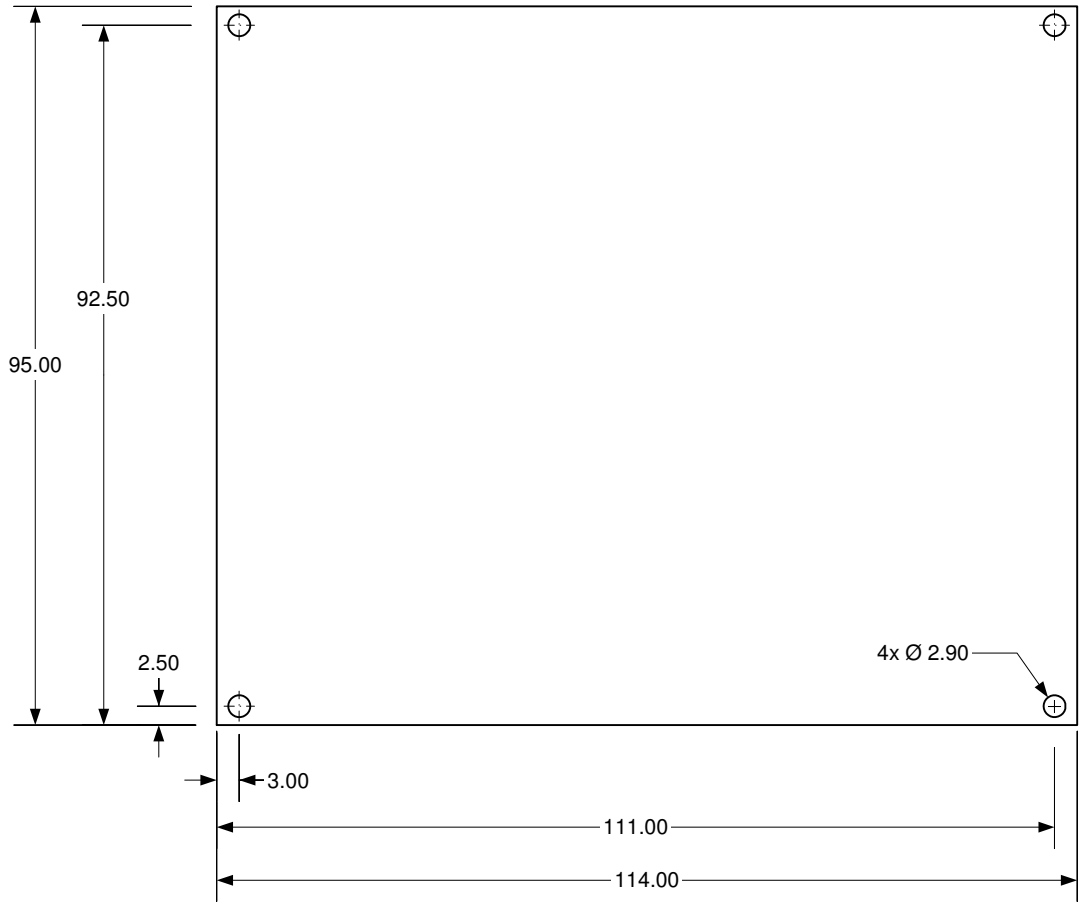


Figure 3: PROFIBUS DEVELOPMENT KIT Outline and Mounting Holes Locations (Top View, mm)

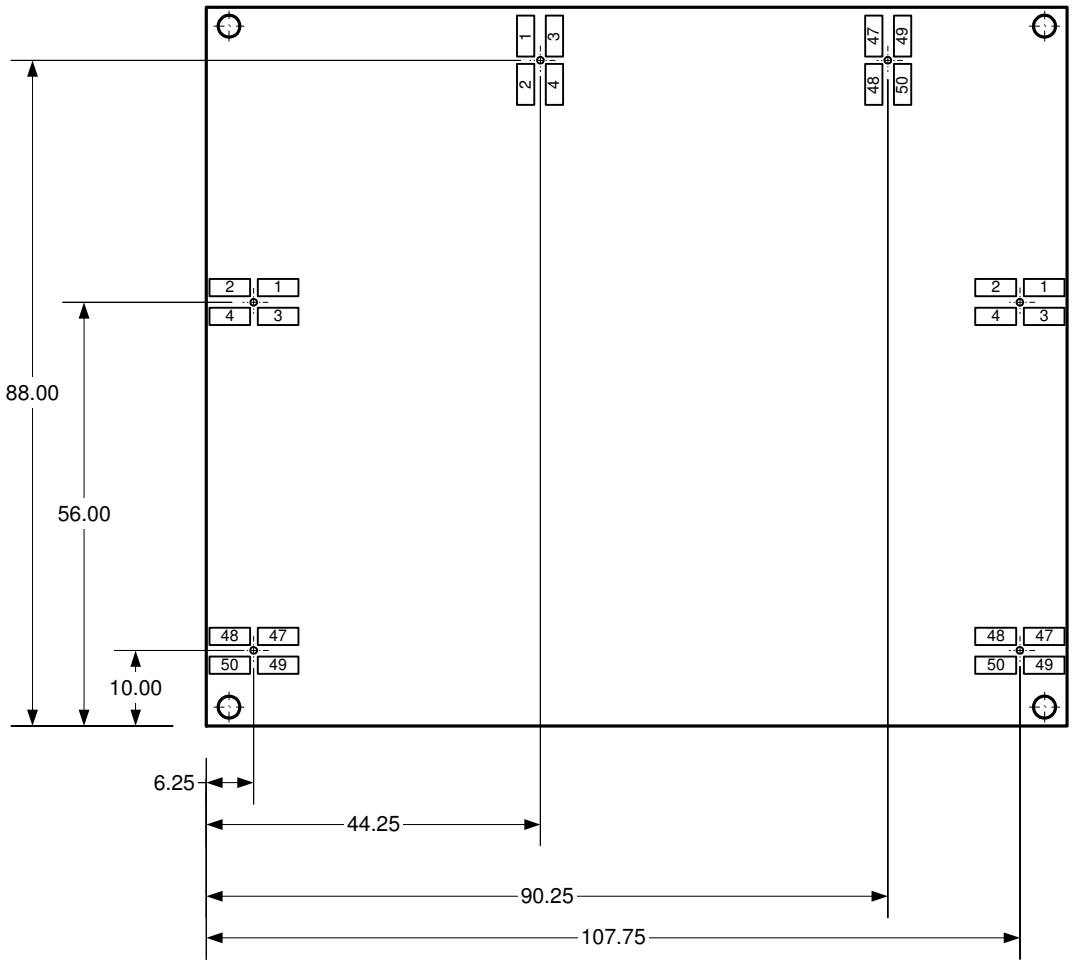


Figure 4: Mounting holes for expansion I/O connectgors based on Molex 79109-1224 connector (Top View, mm)