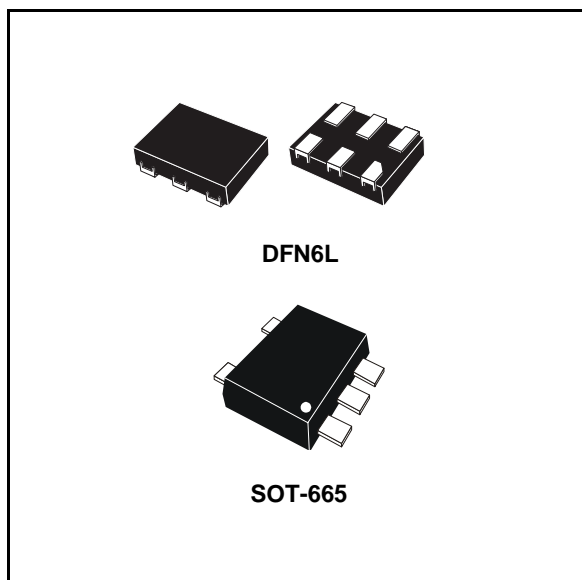


Low power single inverter gate

Features

- High speed: $t_{PD} = 4.3 \text{ ns (max.)}$ at $V_{CC} = 2.3 \text{ V}$
- Power down protection on inputs and outputs
- Balanced propagation delays:
 $t_{PLH} \approx t_{PHL}$
- Operating voltage range:
 $V_{CC} \text{ (opr)} = 1.2 \text{ to } 3.6 \text{ V}$
- Low power dissipation:
 $I_{CC} = 1 \mu\text{A (max.)}$ at $T_A = 85 \text{ }^\circ\text{C}$
- Latch-up performance exceeds 300 mA (JESD 78, Class II)
- ESD performance:
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



Applications

- Mobile phones
- Personal digital assistants (PDAs)

Description

The 74AUP1G04 is a low voltage CMOS single inverter gate fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for 1.2 to 3.6 V operations and low power and low noise applications.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2kV ESD immunity and transient excess voltage.

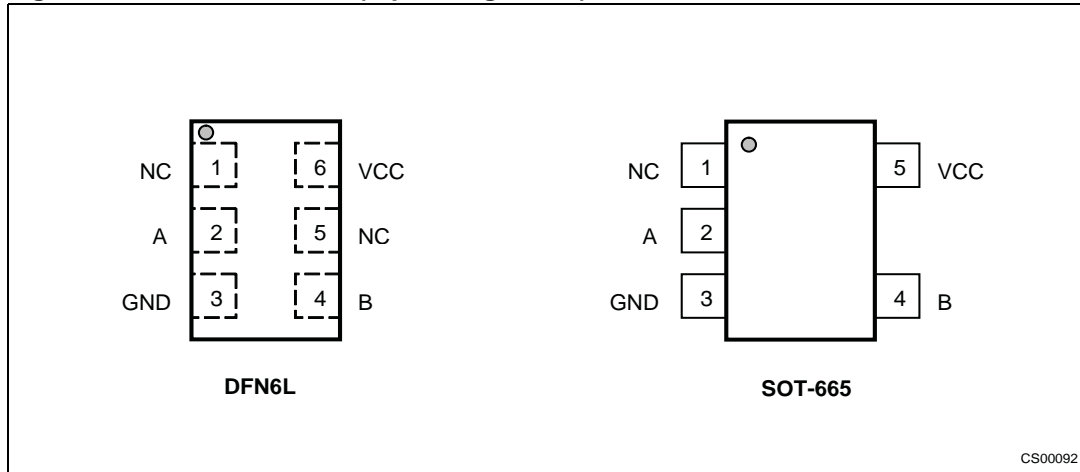
Table 1. Device summary

Order code	Package	Packing
74AUPG04DTR	DFN6L (1.2 x 1 mm)	Tape and reel
74AUPG04GTR	SOT-665 (1.6 x 1.6 mm)	Tape and reel

1 Pin settings

1.1 Pin connection

Figure 1. Pin connection (top through view)



CS00092

1.2 Pin description

Table 2. Pin assignment

DFN pin number	SOT pin number	Symbol	Name and function
1	1	NC	Not connected
2	2	A	Data input
3	3	GND	Ground (0V)
4	4	B	Data output
5	-	NC	Not connected
6	5	V _{CC}	Positive supply voltage

1.3 Truth table

Figure 2. Truth table

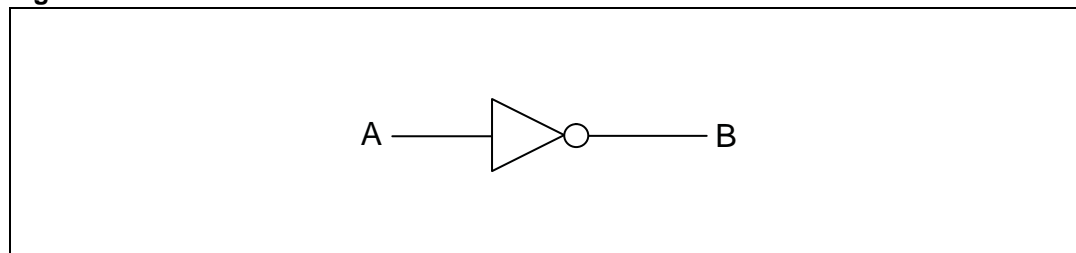
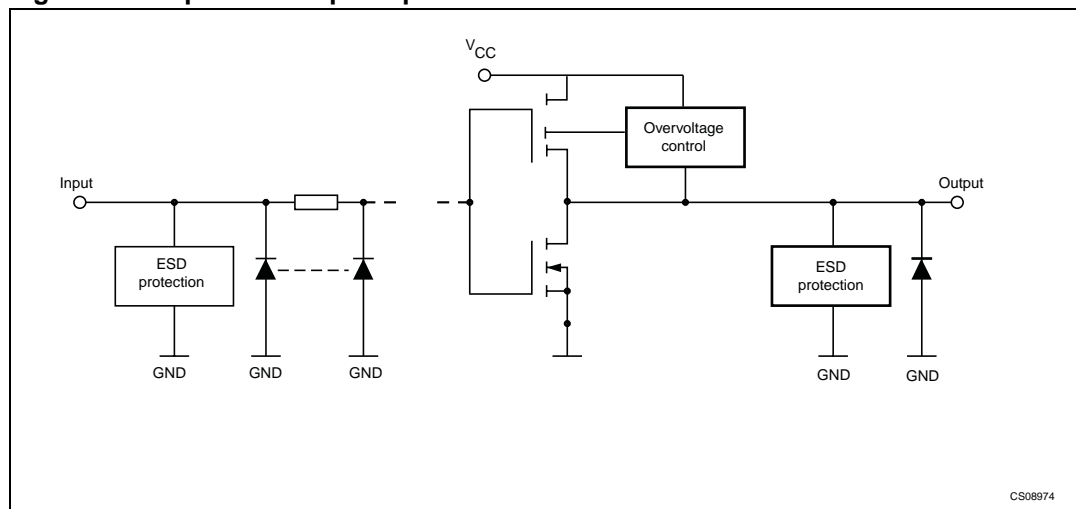


Table 3. Truth table

A	B
L	H
H	L

Figure 3. Input and output equivalent circuit



2 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +4.6	V
V_I	DC input voltage	-0.5 to +4.6	V
V_O	DC output voltage ($V_{CC} = 0$ V)	-0.5 to +4.6	V
V_O	DC output voltage (high or low state)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC input diode current	-20	mA
I_{OK}	DC output diode current	-50	mA
I_O	DC output current	± 50	mA
I_{CC}	DC supply current per supply pin	± 100	mA
I_{GND}	DC ground current per supply pin	± 100	mA
P_D	Power dissipation	200	mW
T_{stg}	Storage temperature	-65 to +150	$^{\circ}C$
T_L	Lead temperature (10 sec)	260	$^{\circ}C$

2.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit	
V_{CC}	Supply voltage	1.2 to 3.6	V	
V_I	Input voltage	0 to V_{CC}	V	
V_O	Output voltage	0 to V_{CC}	V	
T_{op}	Operating temperature	-40 to 85	$^{\circ}C$	
dt/dv	Input rise and fall time	$V_{CC} = 3.0$ to 3.6 V	10	ns/V
		$V_{CC} = 2.3$ to 2.7 V	20	ns/V
		$V_{CC} = 1.2$ to 1.95 V	100	ns/V

3 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	V _{CC} (V)	Test condition	Value		Value		Unit
				25 °C		-40 to 85 °C		
				Min	Max	Min	Max	
V _{IH}	High level input voltage	1.2 to 1.95		0.65 V _{CC}		0.65 V _{CC}		V
		2.0 to 2.7		1.6		1.6		
		2.75 to 3.6		2.0		2.0		
V _{IL}	Low level input voltage	1.2 to 1.95			0.35 V _{CC}		0.35V _{CC}	V
		2.0 to 2.7			0.7		0.7	
		2.75 to 3.6			0.8		0.8	
V _{OH}	High level output voltage	1.2 to 3.6	I _{OH} = -100 µA	V _{CC} - 0.2		V _{CC} - 0.2		V
		3.0	I _{OH} = -10 mA	2.45		2.4		
		2.3	I _{OH} = -6 mA	1.85		1.8		
		1.65	I _{OH} = -4 mA	1.30		1.25		
		1.4	I _{OH} = -2 mA	1.10		1.05		
		1.2	I _{OH} = -1 mA	1.00		0.95		
V _{OL}	Low level output voltage	1.2 to 3.6	I _O = 100 µA		0.15		0.20	V
		3.0	I _O = 10 mA		0.50		0.55	
		2.3	I _O = 6 mA		0.35		0.40	
		1.65	I _O = 4 mA		0.35		0.40	
		1.4	I _O = 2 mA		0.25		0.30	
		1.2	I _O = 1 mA		0.20		0.25	
I _I	Input leakage current	0 to 3.6	V _I = GND to 3.6		±0.1		±0.5	µA
I _{off}	Power off leakage current	0	V _I or V _O = 0 to 3.6 V		±0.1		±1.0	µA
I _{CC}	Quiescent supply current	1.2 to 3.6	V _I = V _{CC} or GND		0.1		1	µA
ΔI _{CC}	I _{CC} increment per input	3.3	V _I = V _{CC} - 0.6V, I _O = 0		80		100	µA

Table 7. AC electrical characteristics

Symbol	Parameter	V _{CC} (V)	Test condition	Value			Unit
				C _L (pF)	25 °C	-40 to 85 °C	
			Typ		Min	Max	
t _{PLH} , t _{PHL}	Propagation delay time	1.1 to 1.3	5	8.0		12.4	ns
		1.4 to 1.6		4.2		6.6	
		1.65 to 1.95		3.2		5.1	
		2.3 to 2.7		2.3		3.1	
		3.0 to 3.6		1.9		2.5	
		1.1 to 1.3	10	8.6		13	
		1.4 to 1.6		4.6		7	
		1.65 to 1.95		3.5		5.3	
		2.3 to 2.7		2.4		3.5	
		3.0 to 3.6		2.0		2.9	
		1.1 to 1.3	15	9.1		13.3	
		1.4 to 1.6		5.6		7.5	
		1.65 to 1.95		3.8		5.7	
		2.3 to 2.7		2.6		3.7	
		3.0 to 3.6		2.2		3.1	
		1.1 to 1.3	30	10.5		16	
		1.4 to 1.6		5.5		9	
		1.65 to 1.95		4.3		6.7	
		2.3 to 2.7		3.1		4.3	
		3.0 to 3.6		2.7		3.8	

Table 8. Capacitive characteristics

Symbol	Parameter	V _{CC} (V)	Test condition	Value			Unit
				T _A = 25 °C			
				Min	Typ	Max	
C _I	Input capacitance	0	V _I = 0 or V _{CC}		3		pF
		3.6	V _I = 0 or V _{CC}		6		
C _O	Output capacitance	3.6	V _I = 0 or V _{CC}		6		pF
C _{PD}	Power dissipation capacitance	3.6	f = 10 MHz		32		pF

4 Test circuit

Figure 4. Test circuit

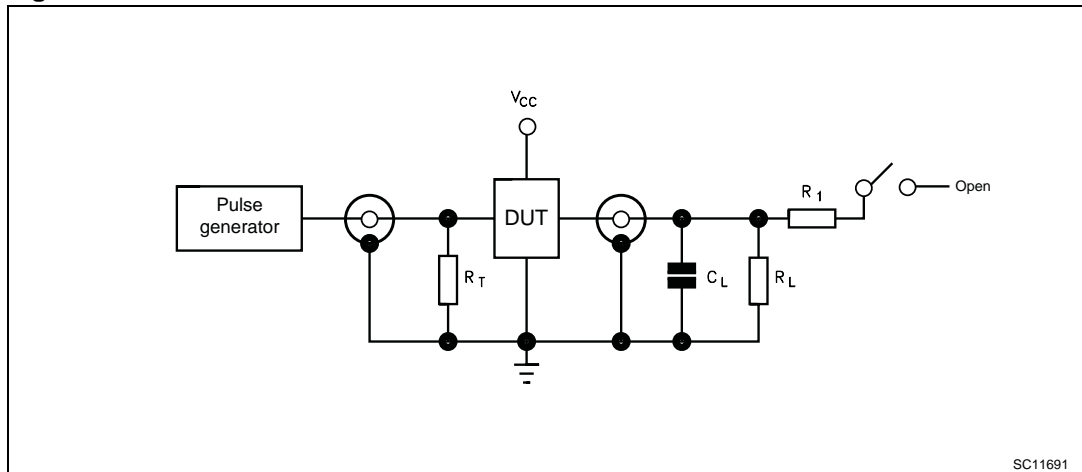


Table 9. Test setting

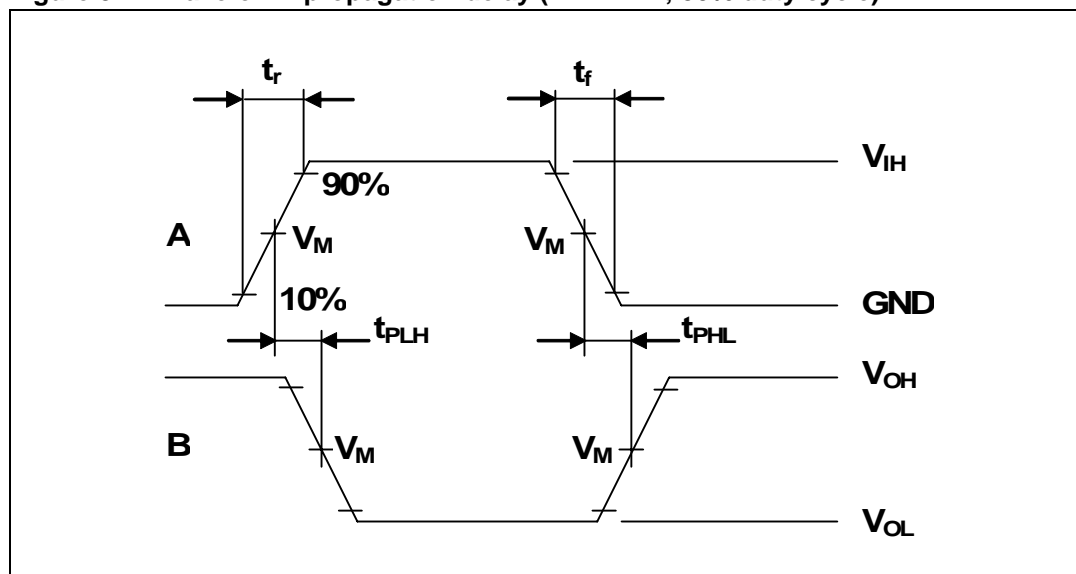
Test	Switch
t_{PLH} , t_{PHL}	Open

Table 10. Symbol and values for test circuit and waveform

Symbol	V_{CC}				
	$1.2 \pm 0.1 \text{ V}$	$1.5 \pm 0.1 \text{ V}$	$1.8 \pm 0.15 \text{ V}$	$2.5 \pm 0.2 \text{ V}$	$3.3 \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
R_L	500 Ω	500 Ω	500 Ω	500 Ω	500 Ω
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	1.5
V_{IH}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
$t_r = t_f$	$\leq 2 \text{ ns}$	$\leq 2 \text{ ns}$	$\leq 2 \text{ ns}$	$\leq 2 \text{ ns}$	$\leq 2 \text{ ns}$

$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 5. Waveform: propagation delay ($f = 1\text{ MHz}$; 50% duty cycle)



5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 6. DFN6L (1.2 x 1 mm) package outline

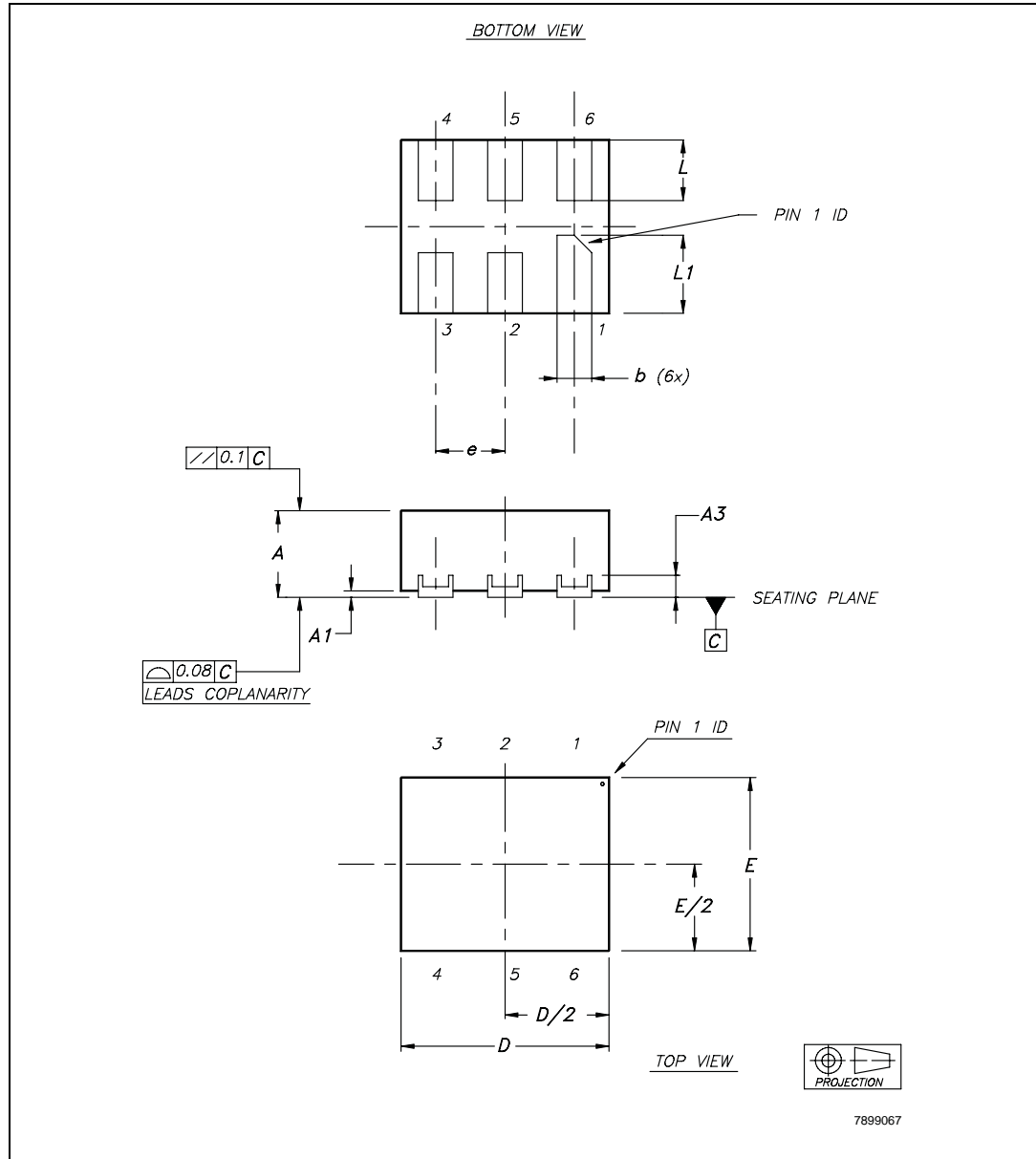


Table 11. DFN6L (1.2 x 1 mm) package mechanical data

Symbol	Millimeters		
	Typ	Min	Max
A	0.50	0.45	0.55
A1	0.02	0	0.05
A3	0.127		
b	0.20	0.15	0.25
D	1.20	1.15	1.25
E	1	0.95	1.05
e	0.40		
L	0.35	0.30	0.40
L1	0.45	0.40	0.50

Figure 7. DFN6L (1.2 x 1 mm) package footprint

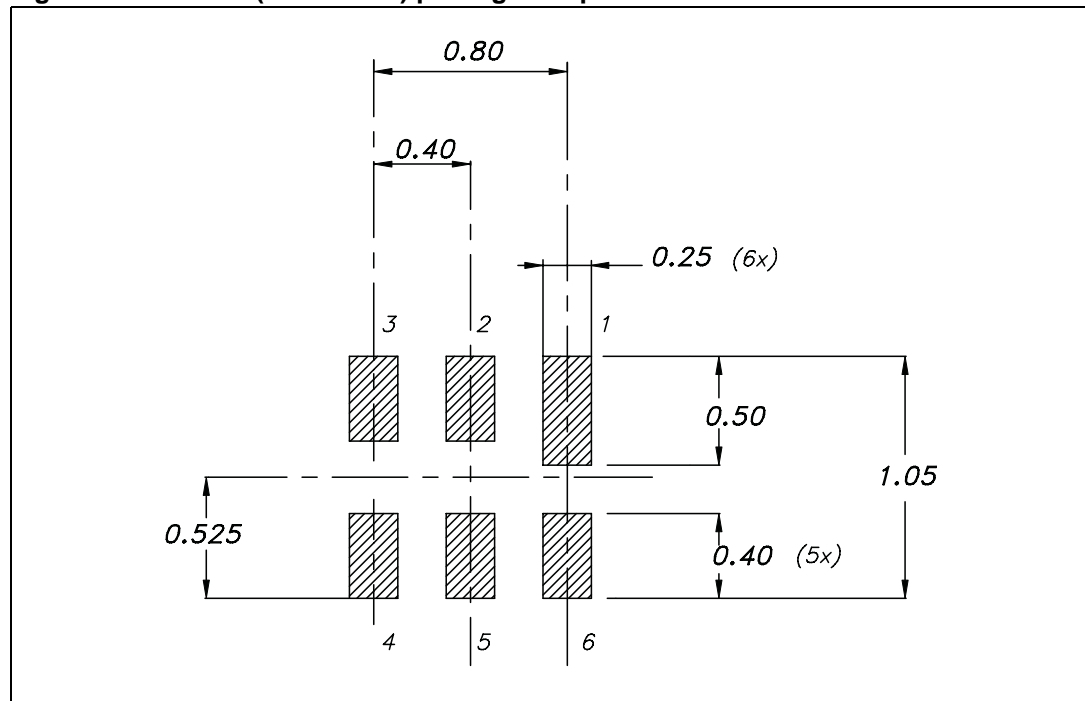


Figure 8. SOT-665 (1.6 x 1.6 mm) package outline

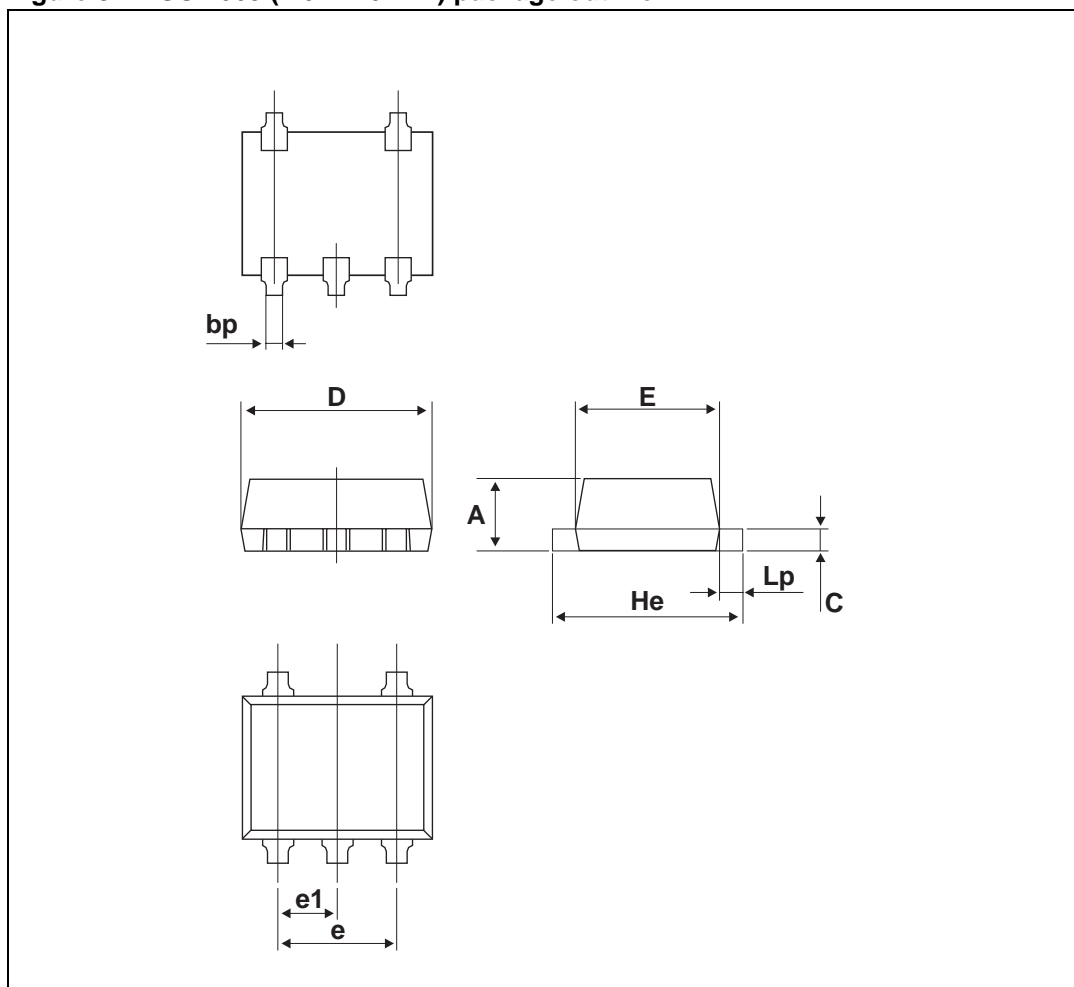


Table 12. SOT665 (1.6 x 1.6 mm) mechanical data

Symbol	Millimeters		
	Typ	Min	Max
A		0.50	0.60
bp		0.17	0.27
c		0.08	0.18
D		1.5	1.7
E		1.1	1.3
e	1		
e1	0.5		
He		1.5	1.7
Lp		0.1	0.3

Figure 9. SOT-665 (1.6 x 1.6 mm) package footprint

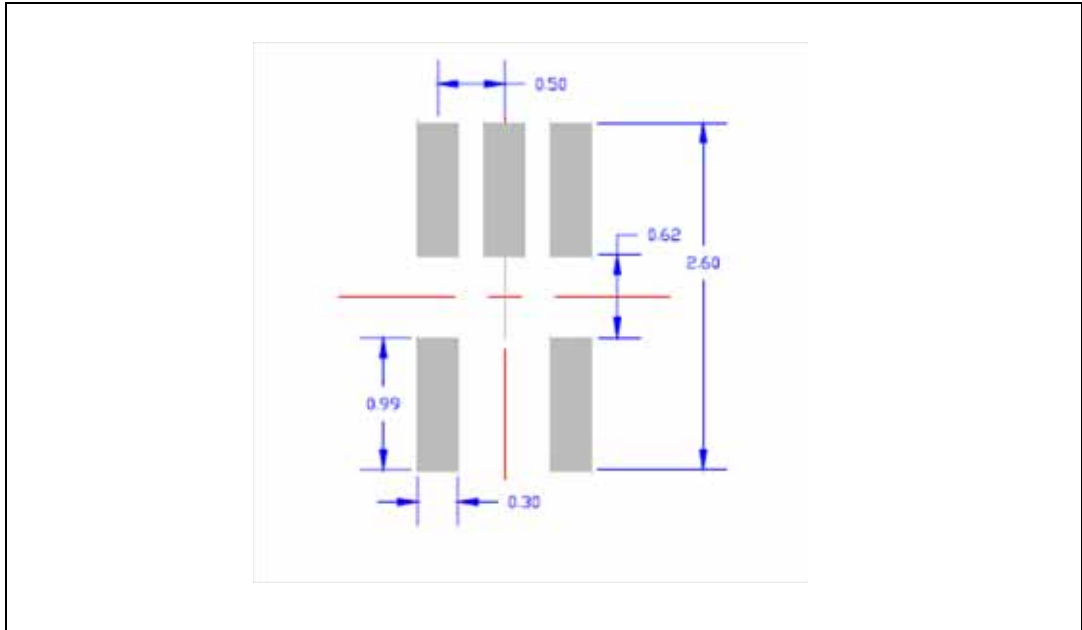


Figure 10. DFN6L (1.2 x 1 mm) carrier tape information

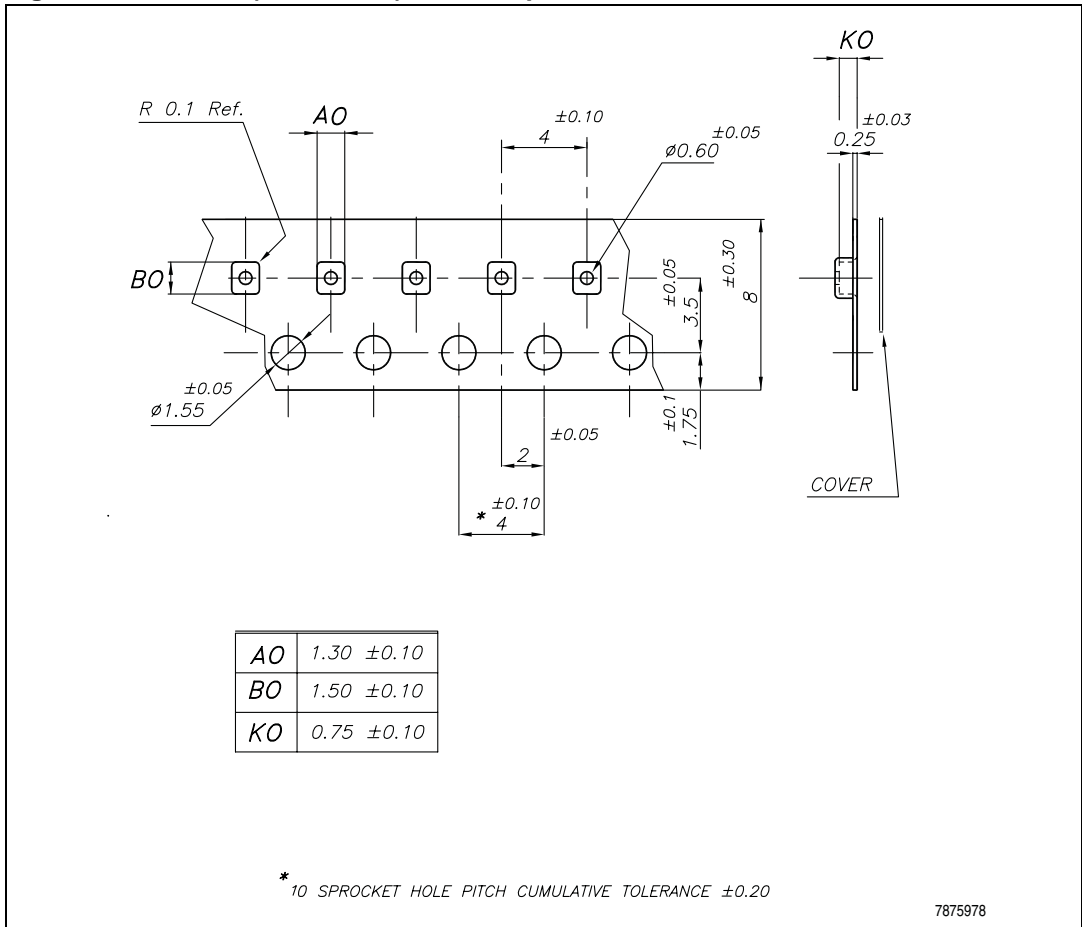


Figure 11. DFN6L (1.2 x 1 mm) reel information drawing (back view)

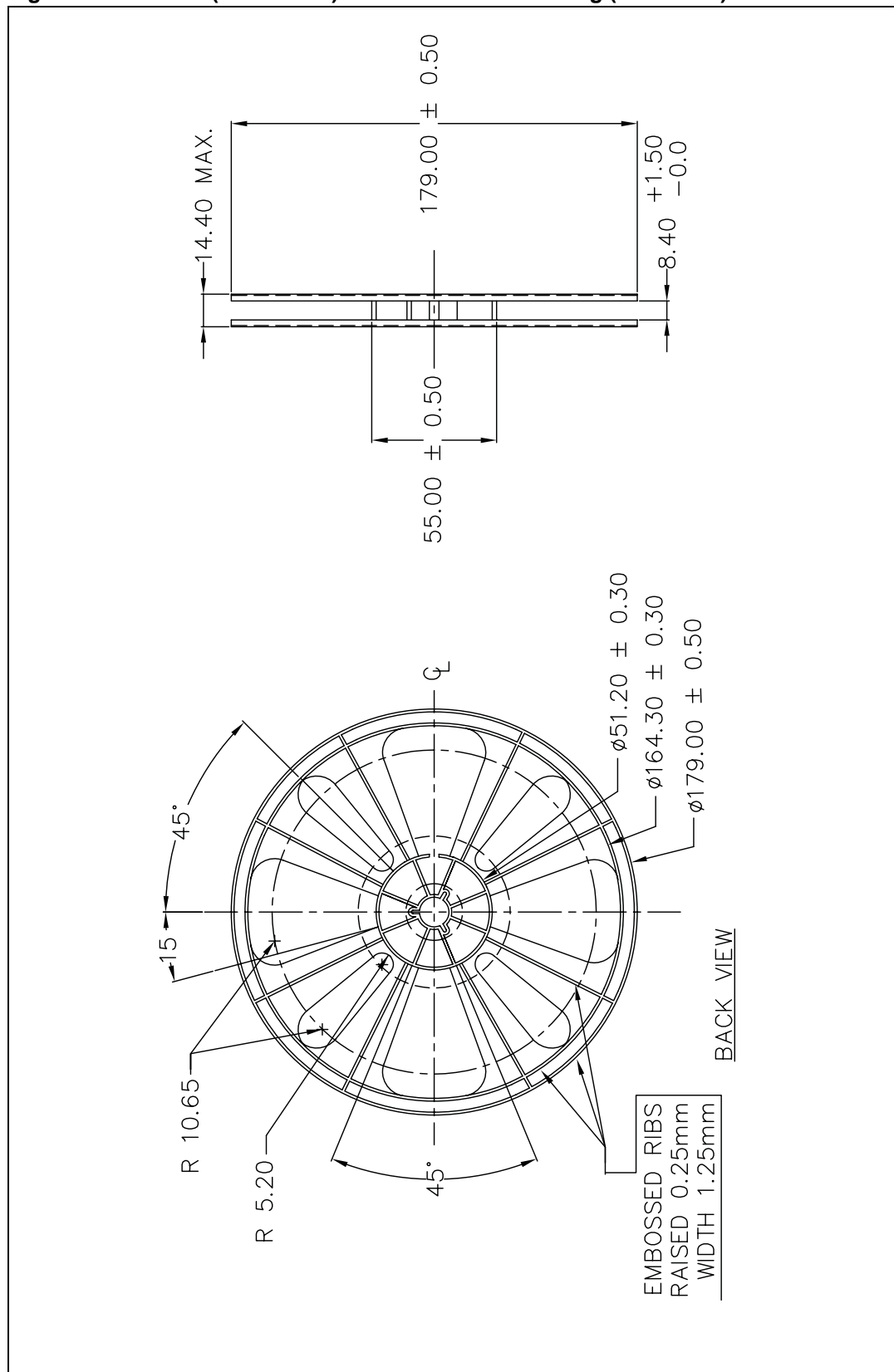


Figure 12. DFN6L (1.2 x 1 mm) reel information drawing (front view)

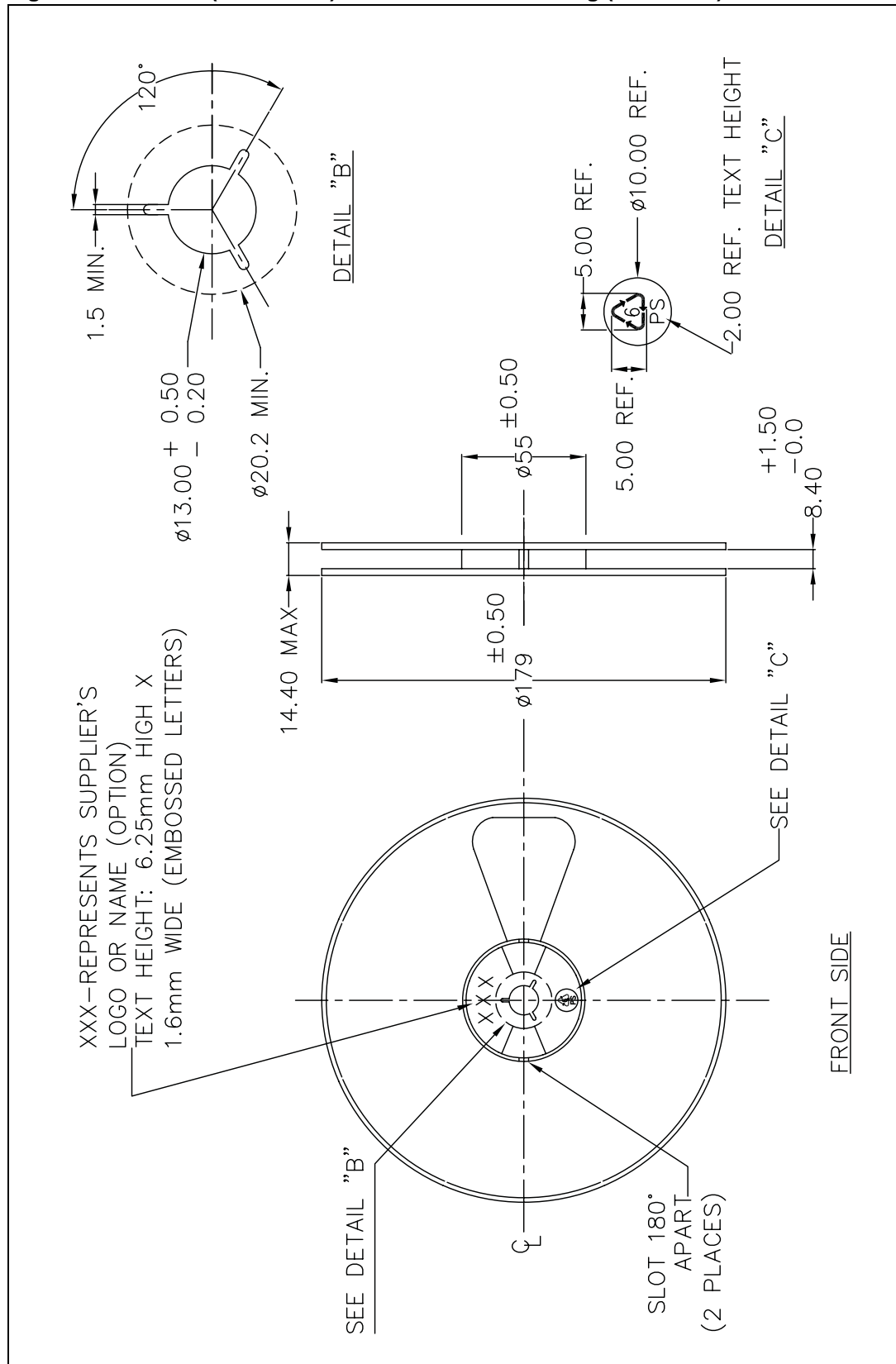


Figure 13. SOT-665 (1.6 x 1.6 mm) carrier tape information

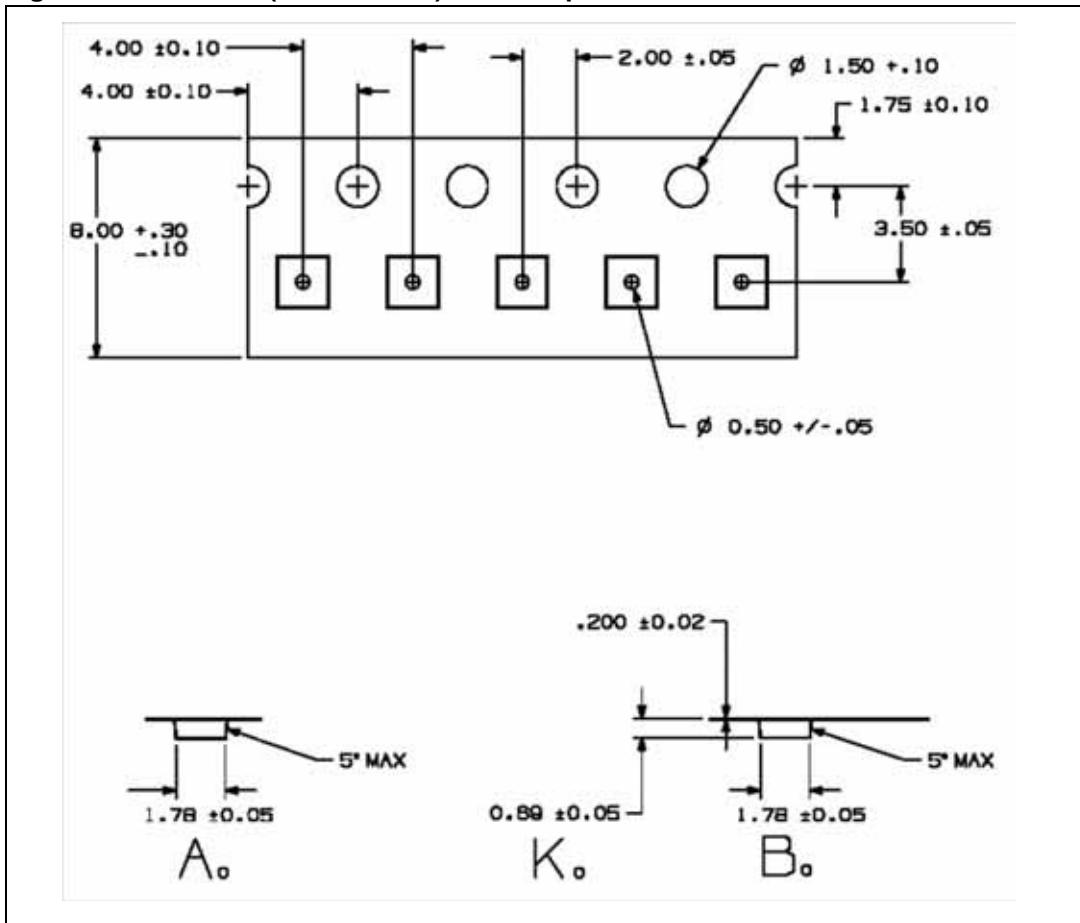


Figure 14. SOT-665 (1.6 x 1.6 mm) reel information

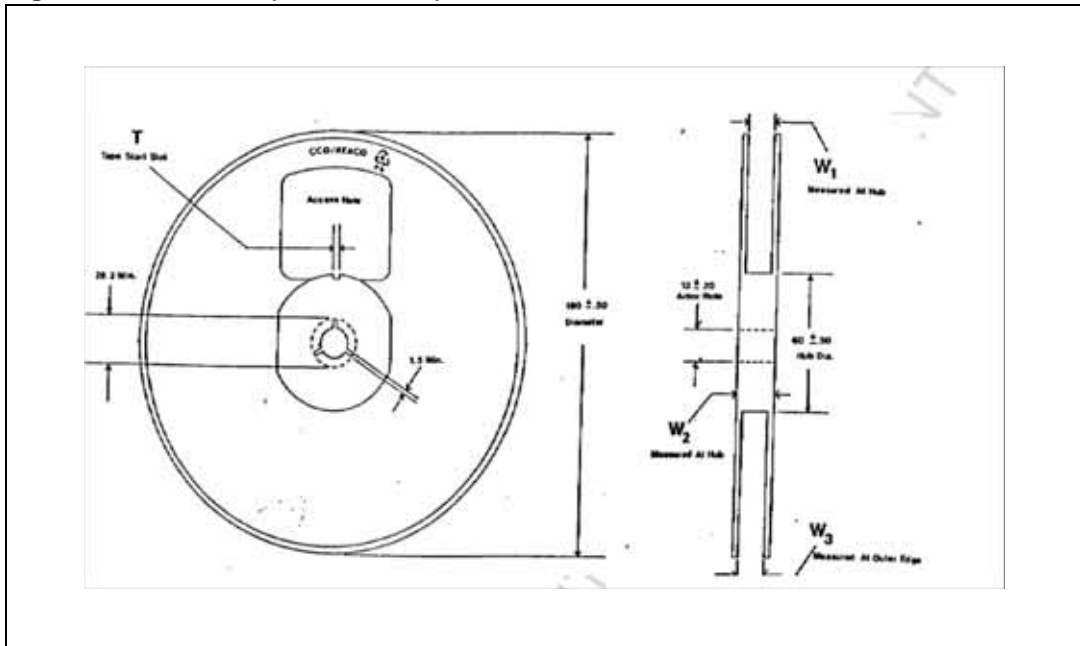


Table 13. SOT-665 (1.6 x 1.6 mm) reel description

Value ⁽¹⁾	R1	R2	R3	eint (at hub)	e1	W1	W2	W3
Min	12.8	175	59.5	8.4	1.5	8.4		7.9
Typ	13	180	60	8.4		8.4		9.4
Max	13.2	185	60.5	10		10	14.4	10.9

1. Millimeters.

6 Revision history

Table 14. Document revision history

Date	Revision	Changes
28-Mar-2008	1	Initial release.

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