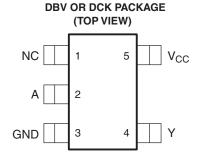
SCES674-MARCH 2007

FEATURES

- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of –55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.6 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

JESD 78, Class II

- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

This single Schmitt-trigger inverter is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G14 device contains one inverter and performs the Boolean function $Y = \overline{A}$. The device functions as an independent inverter, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T_n}) and negative-going (V_{T_n}) signals.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
SOT (SOT-23) – DBV		Reel of 3000	SN74LVC1G14MDBVREP	SBLM
-55 C to 125 C	-55°C to 125°C SOP – DCK		SN74LVC1G14MDCKREP	CAL

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE

INPUT A	OUTPUT Y
Н	L
L	Н



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	V _{CC} Supply voltage range				V
VI	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-imp	pedance or power-off state ⁽²⁾	-0.5	6.5	V
Vo	Vo Voltage range applied to any output in the high or low state (2)(3)				V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
0	Package thermal impedance ⁽⁴⁾			389	°C/W
θ_{JA}	DBV				C/VV
T_{stg}	T _{stg} Storage temperature range				°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

The value of V_{CC} is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-2.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
1/	Cumply veltage	Operating	1.65	5.5	V
V_{CC}	Supply voltage	Data retention only	1.5		V
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-8	
I_{OH}	OH High-level output current	V 2.V		-16	
		V _{CC} = 3 V		-24	
		V _{CC} = 4.5 V		-32	
		V _{CC} = 1.65 V		4	
		V _{CC} = 2.3 V		8	
I_{OL}	Low-level output current	V 2 V		16	mA
		V _{CC} = 3 V		24	
		V _{CC} = 4.5 V		32	
T _A	Operating free-air temperature		-55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾ MAX	UNIT	
		1.65 V	0.79	1.16		
V_{T+}		2.3 V	1.11	1.56		
Positive-going input threshold		3 V	1.5	1.87	V	
voltage		4.5 V	2.16	2.74		
		5.5 V	2.61	3.33		
		1.65 V	0.39	0.62		
V_{T-}		2.3 V	0.58	0.87		
Negative-going input threshold		3 V	0.84	1.14	V	
voltage		4.5 V	1.41	1.79		
		5.5 V	1.87	2.29		
		1.65 V	0.37	0.62		
ΔV_T		2.3 V	0.48	0.77		
Hysteresis (V _{T+} - V _{T-})		3 V	0.56	0.87	V	
		4.5 V	0.71	1.04		
		5.5 V	0.71	1.11		
	$I_{OL} = -100 \mu A$	1.65 V to 4.5 V	V _{CC} - 0.1			
	$I_{OL} = -4 \text{ mA}$	1.65 V	1.2			
V	$I_{OL} = -8 \text{ mA}$	2.3 V	1.9		V	
V_{OH}	$I_{OL} = -16 \text{ mA}$	3 V	2.4		V	
	$I_{OL} = -24 \text{ mA}$	3 V	2.3			
	$I_{OL} = -32 \text{ mA}$	4.5 V	3.8			
	$I_{OL} = 100 \mu\text{A}$	1.65 V to 4.5 V		0.1		
	$I_{OL} = 4 \text{ mA}$	1.65 V		0.45		
V	$I_{OL} = 8 \text{ mA}$	2.3 V		0.3	V	
V_{OL}	I _{OL} = 16 mA	3 V		0.4	V	
	I _{OL} = 24 mA	3 V		0.55		
	I _{OL} = 32 mA	4.5 V		0.55	İ	
I _I A input	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V		±5	μΑ	
I _{off}	V_I or $V_O = 5.5 \text{ V}$	0		±10	μΑ	
I _{CC}	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V		19	μΑ	
ΔI_{CC}	One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND	3 V to 5.5 V		500	μΑ	
C _i	$V_I = V_{CC}$ or GND	3.3 V		4.5	pF	

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	PARAMETER FROM (INPUT)		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
	(INFOT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Υ	2.8	9.9	1.6	5.5	1.5	4.6	0.9	4.4	ns

SN74LVC1G14-EP SINGLE SCHMITT-TRIGGER INVERTER

SCES674-MARCH 2007



Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
	(INPOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Υ	3.8	16	2	7.5	1.8	6.0	1.2	5	ns

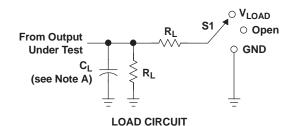
Operating Characteristics

 $T_A = 25^{\circ \circ}C$

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V V _{CC} = 5 V		UNIT	
TAKAMETEK	1231 CONDITIONS	TYP	TYP	TYP	TYP	ONII	
C _{pd} Power dissipation capacitance	f = 10 MHz	20	21	22	25	pF	

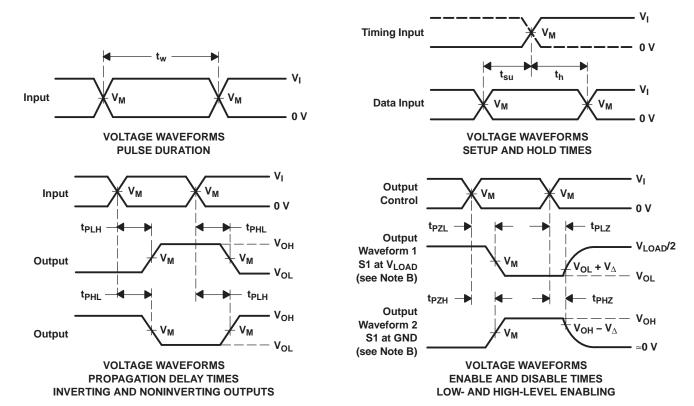


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V_{LOAD}
t _{PHZ} /t _{PZH}	GND

.,	IN	PUTS	.,	.,	•	_	.,
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	V_{Δ}
1.8 V ± 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.15 V
2.5 V \pm 0.2 V	V_{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 M Ω	0.3 V
5 V \pm 0.5 V	v_{cc}	≤2.5 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.3 V

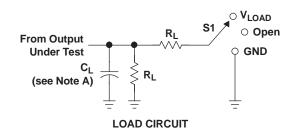


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_0 = 50 Ω .
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

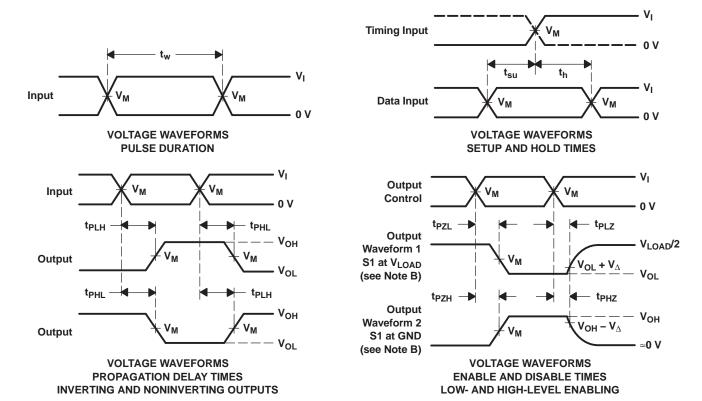


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

V	INF	PUTS	.,	V	_	Б	V
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	V_{Δ}
1.8 V ± 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V \pm 0.5 V	V _{CC}	≤2.5 ns	V _{CC} /2	2×V _{CC}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_0 = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

www.ti.com 28-May-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins F	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
1P1G14MDBVREPG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G14MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/07626-01XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G14-EP:

Catalog: SN74LVC1G14

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

www.ti.com 8-Mar-2011

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G14MDBVREP	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

www.ti.com 8-Mar-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G14MDBVREP	SOT-23	DBV	5	3000	202.0	201.0	28.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.



DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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