SN74LS19A, SN74LS24A SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

JANUARY 1981 - REVISED MARCH 1988

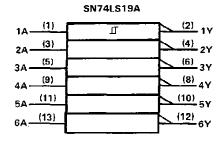
- Functionally and Mechanically Identical to 'LS13, 'LS14, and 'LS132, Respectively
- Improved Line-Receiving Characteristics
- P-N-P Inputs Reduce System Loading
- Excellent Noise Immunity with Typical Hysteresis of 0.8 V

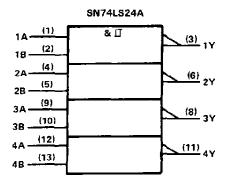
description

Each circuit functions as a NAND gate or inverter, but because of the Schmitt action, it has different input threshold levels for positivegoing $\{V_{T+}\}$ and for negative-going $\{V_{T-}\}$ signals. The hysteresis or backlash, which is the difference between the two threshold levels $\{V_{T+} - V_{T-}\}$, is typically 800 millivolts.

These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

logic symbols†





[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LS19A . . . D. J, OR N PACKAGE (TOP VIEW)

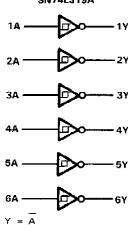
	_		_
1A 🗌	1	U 14	□vcc
1Y 🗌	2	13	□6A
2A 🗌	3	12	<u>∏</u> 6Y
2Y 🗀	4	11]5A
3A 🗌	5	10	_5Y
3Y 🖺	6	9	□4A
GND 🗌	7	8	□4 Y

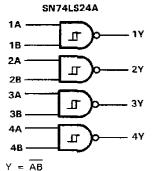
SN74LS24A . . . D, J, OR N PACKAGE (TOP VIEW)

1A 1	14	V C (
1B 2	13	4B
1Y 3	12	4A
2A 4	11	4Y
2B 5	10	3B
	11 10 9 8	ļ,

logic diagrams (positive logic)

SN74LS19A

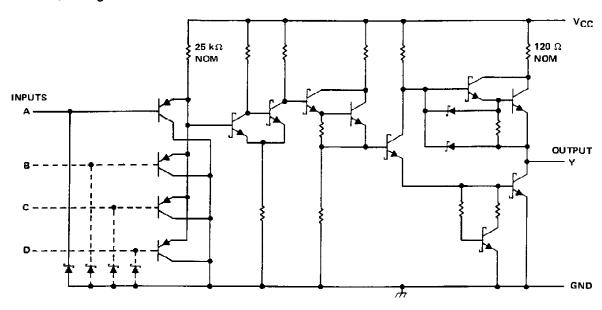




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schematic (each gate)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range 0°C to 7	70°C
Storage temperature range65°C to 15	50°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, VCC	4.75	5	5.25	V
High-level output current, IOH			-400	μΑ
Low-level output current, IOL			8	mA
Operating free-air temperature, TA	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDIT	MIN	TYP‡	MAX	UNIT	
V _{T +}	V _{CC} = 5 V			1.65	1.9	2.15	V
٧٢_	V _{CC} = 5 V			0.75	1.0	1.25	٧
Hysteresis (VT+ - VT-)	V _{CC} = 5 V			0.4	0.9		V
VIK	VCC = MIN.	ij = -18 mA			-1.5		V
VoH	V _{CC} → MIN,	V _I ÷ V _{T-min}	I _{OH} = -0.4 mA	2.7	3.4		V
V	Vcc = MIN,	V. – V–	$I_{OL} = 4 \text{ mA}$		0.25	0.4	V
VOL	A.C.C. = 341114'	$V_{\parallel} = V_{T+max}$	I _{OL} = 8 mA		0.35	0.5	ľ
¹ Τ+	Vcc = 5 V.	V _I = V _{T+}			-2	- 20	$\mu \Delta$
I _T _	V _{CC} = 5 V,	V _I = V _T =			-5	- 30	μΑ
I ₁	$V_{CC} = MAX$	V _I = 7 V			0.1		mΑ
IН	$V_{CC} = MAX$	V _I = 2.7 V				20	μА
IIL	V _{CC} = MAX.	V _I = 0.4 V				- 50	μΑ
los§	$V_{CC} = MAX$	$V_1 = V_0 = 0 V$		- 20		- 100	mΑ
1	V _{CC} = MAX,	V6 0 V	'LS19A		9.9	18	4
_Г ССН	VCC = MAX,	ν ₁ = υ ν	'LS24A		6.6	12	mA
1)/ MAY)(, _ 4 E)/	'LS19A		17	30	0
CCL	$V_{CC} = MAX, V_{I}$	ν = 4.5 V	'LS24A		11	20	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC - 5 V, TA - 25 °C (see Figure 1)

DADAMETED	FROM	то	TEST CONDITIONS	SI	174LS1	9A	SN	174L\$2	4A	UNIT
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	ONII
tPLH	Any	Y	$R_1 = 2 k\Omega$, $C_1 = 15 pF$		13	20		13	20	ns
tpHI	Any	Υ	$R_L = 2 k\Omega$, $C_L = 15 pF$		18	30		25	40	ns

tplH = Propagation delay time, low-to-high-level output

tpHL = Propagation delay time, high-to-low-level output

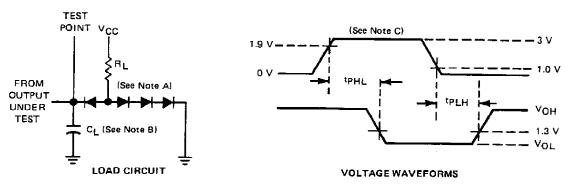


 $^{^4}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. All diodes are IN3064 or equivalent.

- B. C_L includes probe and circuit capacitance.
- C. The generator characteristics are: PRR = 1 MHz, t_r = 15 ns, t_p = 6 ns, Z_0 = 50 Ω .

FIGURE 1

PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LS19ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS19ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS19ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS19AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS19ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS19ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS19ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS19ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS24AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74LS24AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS19ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS19ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS19ADR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LS19ANSR	SO	NS	14	2000	346.0	346.0	33.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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