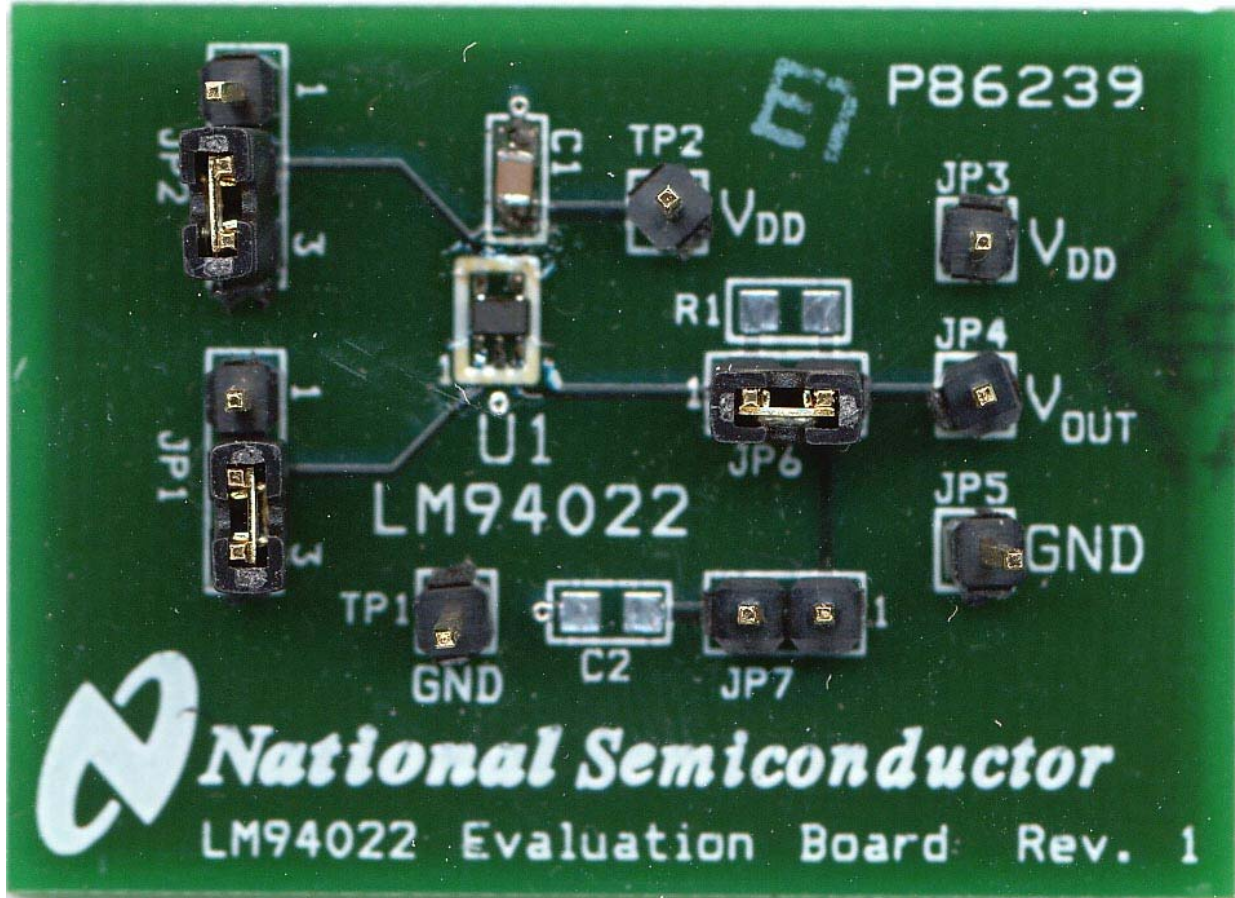


LM94022 Evaluation Board User's Guide



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Table of Contents

Table of Contents	2
References	3
1.0 Introduction	4
1.1 Block Diagram	4
2.0 Quick Start	5
2.1 Quick Start Diagram	5
3.0 Functional Description	6
3.1 LM95022 Evaluation Board Connection Table	6
4.0 Electrical and Mechanical Specifications	7
4.1 Electrical Specifications	7
4.2 Electrical Schematic	7
4.3 Evaluation Board Layout	8
4.4 Bill of Materials	9
4.5 Mechanical Specifications	9

LM94022 Evaluation Board User's Guide

References

1. "LM94022 1.5V, SC70, Multi-Gain Analog Temperature Sensor with Class-AB Output" datasheet.

The latest copy of the LM94022 datasheet can be obtained by going to the National Semiconductor website www.national.com, by searching on "LM94022", and then downloading the LM94022.pdf file.

1.0 Introduction

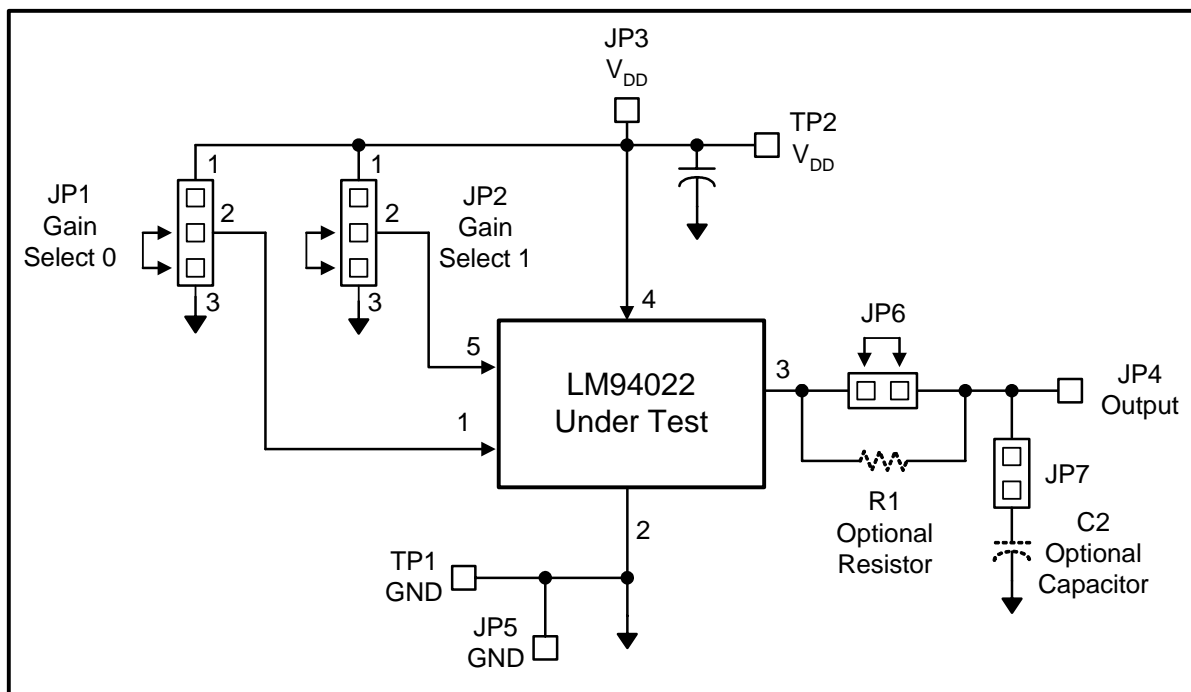
The LM94022 Evaluation Board offers the user a convenient way to experiment with the operation of the LM94022 Multi-Gain Temperature Sensor.

There are jumpers that allow the selection of the temperature-to-output voltage gain. The default condition for the Gain Select 0 jumper (JP1) is for the shunt to be across pins 2 and 3. The default condition for the Gain Select 1 jumper (JP2) is also for the shunt to be across pins 2 and 3.

By default, jumper JP6 is installed, connecting the LM94022 output to pin JP4. The evaluation board can be configured with an output capacitor by installing C2 and shorting jumper JP7. Resistor R1 can be installed and JP6 removed to insert it in series with the output. See the datasheet for recommended values for R1 and C2.

The block diagram below shows the jumpers in the default condition.

1.1 Block Diagram



2.0 Quick Start

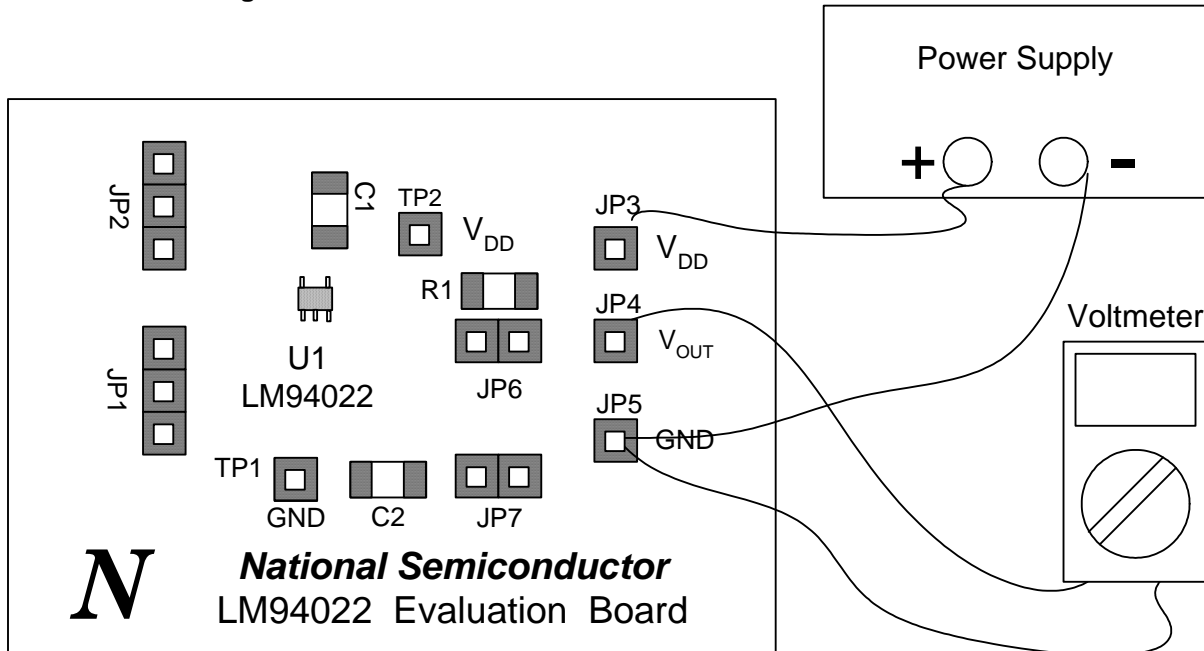
The diagram below shows how the LM94022 is connected in a typical bench test configuration.

Before applying power directly to the LM94022 Evaluation Board, make sure that the voltage is between +1.5 VDC and +5.5 VDC. Also make sure that JP1 and JP2 are

jumpered for the desired gain. Make sure that JP6 is jumpered for a direct connection to the output.

Apply power to the LM94022 evaluation board. Measure the output voltage connected between to output pin (JP4) and ground.

2.1 Quick Start Diagram



!

3.0 Functional Description

Selecting the LM94022's various output gains is described in detail in the LM94022 datasheet.

The inversely proportional output voltage vs temperature characteristic has different slopes depending on the gain select. See the datasheet for details.

3.1 LM94022 Evaluation Board Connection Table

Connector Label	Connector Name	Pin Number	Description
JP1	Gain Select 0	1 - 2	If pins 1 and 2 are jumpered then Gain Select 0 is connected to V_{DD} .
		2 - 3	If Pins 2 and 3 are jumpered then Gain Select 0 is connected to GND. Default: pins 2 and 3 are jumpered.
JP2	Gain Select 1	1 - 2	If pins 1 and 2 are jumpered then Gain Select 1 is connected to V_{DD} .
		2 - 3	If Pins 2 and 3 are jumpered then Gain Select 1 is connected to GND. Default: pins 2 and 3 are jumpered.
JP3	V_{DD} Input		Supply +1.5 to 5.5 VDC to this pin.
JP4	V_{OUT} Output		This is the output pin. See the schematic and description within this document.
JP5	GND Input		This is Power Supply return for V_{DD} Input (JP3).
JP6	Series Output	1 - 2	Jumper is installed across pins 1 and 2 by default. Otherwise resistor R1 is in series with the output.
JP7	Parallel Output	1 - 2	Jumper is not installed across pins 1 and 2 by default. Otherwise capacitor C2 shunts the output.
TP1	Test Point 1		This is the GND test point
TP2	Test Point 2		This is the V_{DD} test point.

4.0 Electrical and Mechanical Specifications

4.1 Electrical Specifications

Power Requirements	
The Board uses the +1.5 VDC to +5.5 VDC and GND lines from an external low-noise power supply.	+1.5 VDC to +5.5 VDC

4.2 Electrical Schematic

JP1 and JP2 default configuration:
Pins 2 and 3 shorted.

Note: Pin 2 of JP1 and JP2 must
be shorted high or low. Do not
leave floating.

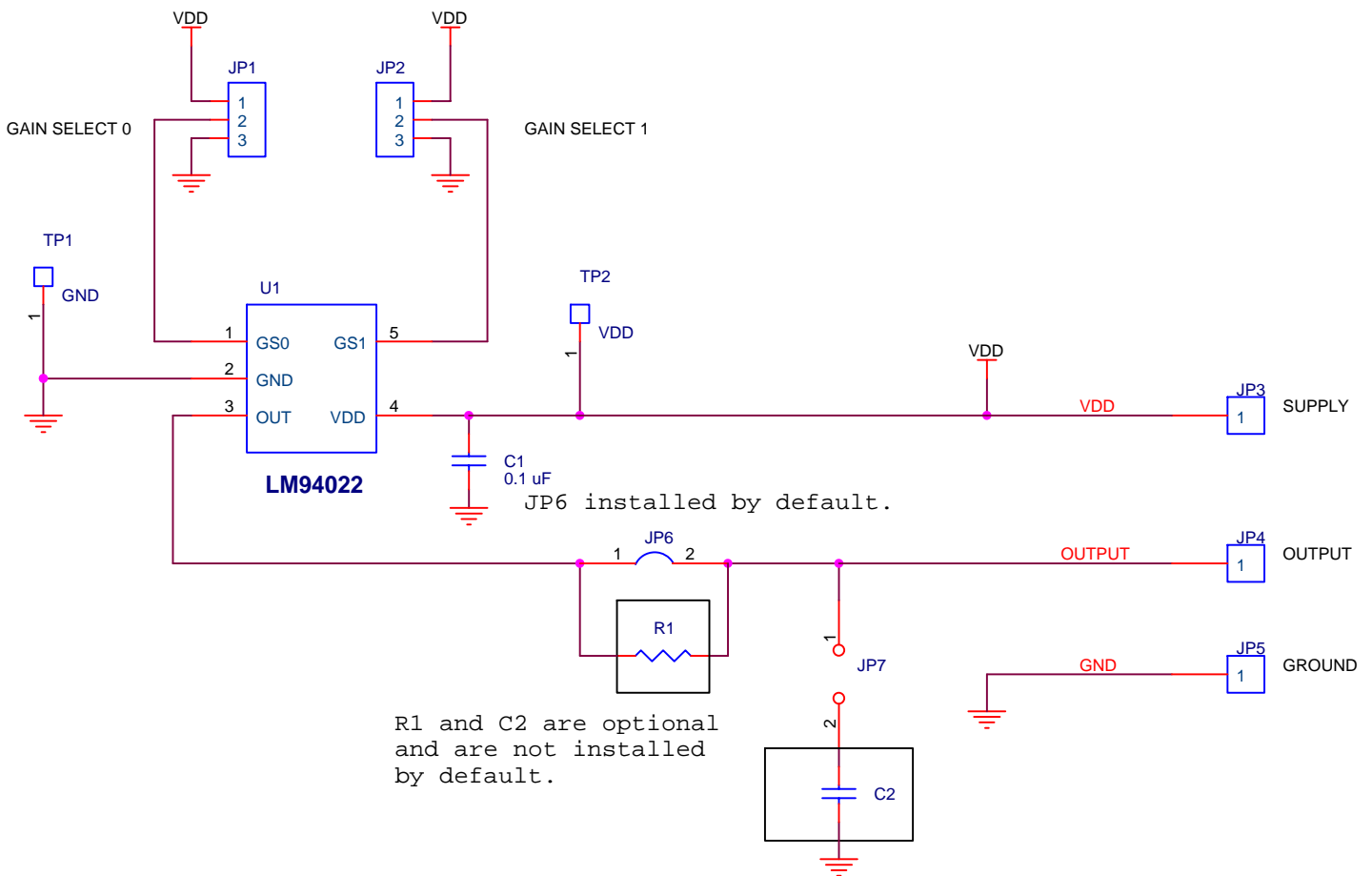


Figure 4.2 Schematic Diagram of the LM94022 Evaluation Board

4.3 Evaluation Board Layout

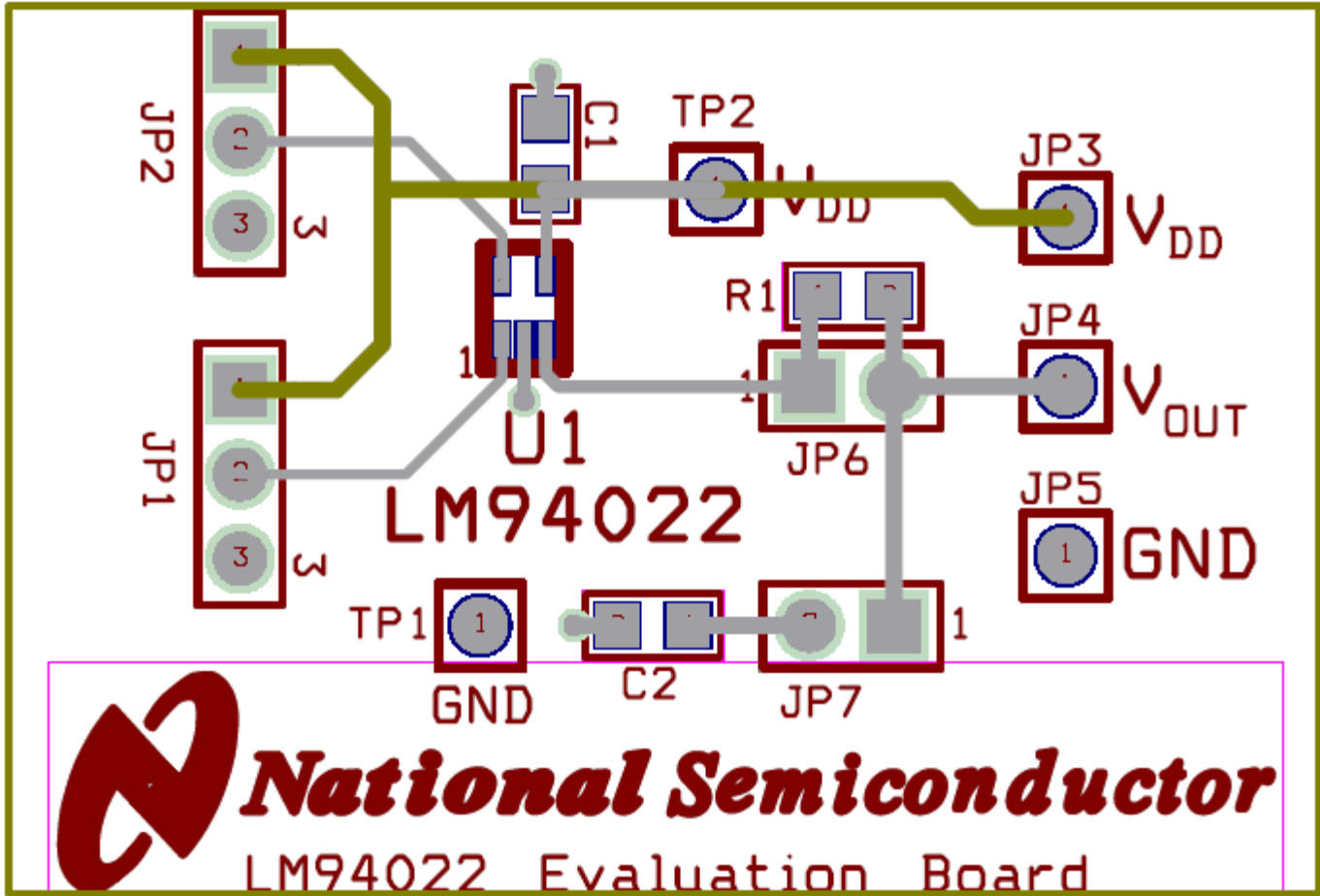


Figure 4.3 Layout diagram of the LM94022 Evaluation Board

4.4 Bill of Materials for LM94022 Evaluation Board

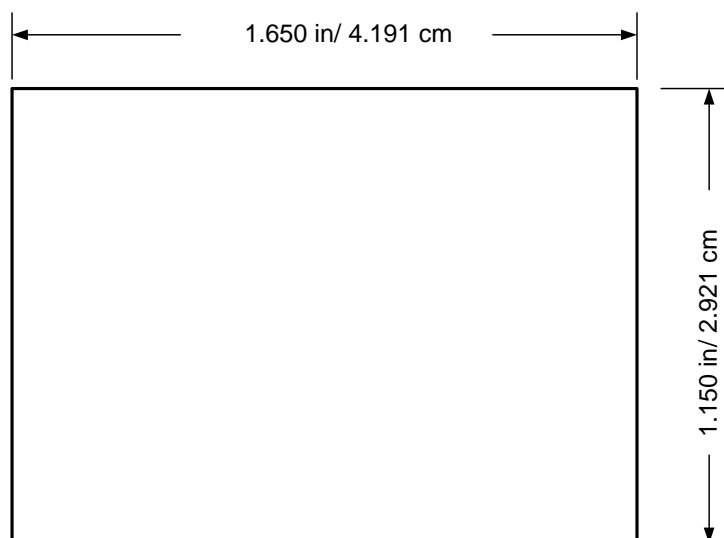
Item	Quantity	Reference	Part
1	1	C1	Capacitor, Ceramic, 0.1uF
2	1	C2	Capacitor (not stuffed)
3	2	JP1, JP2	Header, 1X3, 0.1 in centers
4	3	JP3, JP4, JP5	Header, 1X1, 0.1 in centers
5	2	JP6, JP7	Header, 1X2, 0.1 in centers
6	3		Shunts, 1X2, 0.1 in centers,
7	1	R1	Resistor, (not stuffed)
8	2	TP1-TP2	Test Points (1X1 Headers)
9	1	U1	LM94022CIMF Device Under Test (DUT)
10	1	--	Circuit Board, Fabricated, LM94022 Evaluation Board, Rev. 1

4.5 Mechanical Specifications

4.5.1 Operating Mechanical and Environmental Specifications

	Minimum	Typical	Maximum
Temperature	0°C	25°C	70°C

4.5.2 Evaluation Board Basic Dimensions



4.5.3 Electrostatic Discharge (ESD) Precautions

The user shall use ESD precautions as specified in National Semiconductor ESD document (SC)CSI-3-038 available through www.national.com.

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