



PGA204 PGA205

Programmable Gain INSTRUMENTATION AMPLIFIER

FEATURES

- DIGITALLY PROGRAMMABLE GAIN:
 PGA204: G=1, 10, 100, 1000V/V
 PGA205: G=1, 2, 4, 8V/V
- LOW OFFSET VOLTAGE: 50µV max
- LOW OFFSET VOLTAGE DRIFT: 0.25µV/°C
- LOW INPUT BIAS CURRENT: 2nA max
- LOW QUIESCENT CURRENT: 5.2mA typ
- NO LOGIC SUPPLY REQUIRED
- 16-PIN PLASTIC DIP, SOL-16 PACKAGES

APPLICATIONS

- DATA ACQUISITION SYSTEM
- GENERAL PURPOSE ANALOG BOARDS
- MEDICAL INSTRUMENTATION

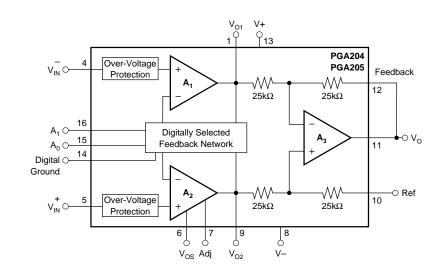
DESCRIPTION

The PGA204 and PGA205 are low cost, general purpose programmable-gain instrumentation amplifiers offering excellent accuracy. Gains are digitally selected: PGA204—1, 10, 100, 1000, and PGA205—1, 2, 4, 8V/V. The precision and versatility, and low cost of the PGA204 and PGA205 make them ideal for a wide range of applications.

Gain is selected by two TTL or CMOS-compatible address lines, A_0 and A_1 . Internal input protection can withstand up to $\pm 40V$ on the analog inputs without damage.

The PGA204 and PGA205 are laser trimmed for very low offset voltage (50 μ V), drift (0.25 μ V/°C) and high common-mode rejection (115dB at G=1000). They operate with power supplies as low as ±4.5V, allowing use in battery operated systems. Quiescent current is 5mA.

The PGA204 and PGA205 are available in 16-pin plastic DIP, and SOL-16 surface-mount packages, specified for the -40° C to $+85^{\circ}$ C temperature range.



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SPECIFICATIONS

ELECTRICAL

At $T^{}_{A}$ = +25°C, $V^{}_{S}$ = $\pm 15 V,$ and $R^{}_{L}$ = $2 k \Omega$ unless otherwise noted.

PGA204 G=1, 10, 100, 1000V/V

		PGA204BP, BU			P			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT Offset Voltage, RTI vs Temperature vs Power Supply Long-Term Stability Impedance, Differential Common-Mode Input Common-Mode Range	$T_A=+25^{\circ}C$ $T_A=T_{MIN}$ to T_{MAX} $V_S=\pm4.5V$ to $\pm18V$ $V_O=0V$ (see text)	±10.5	$\begin{array}{c} \pm 10+20/G\\ \pm 0.1+0.5/G\\ 0.5+2/G\\ \pm 0.2+0.5/G\\ 10^{10} 6\\ 10^{10} 6\\ \pm 12.7\end{array}$	±50+100/G ±0.25+5/G 3+10/G	*	±25+30/G ±0.25+5/G * * *	±125+500/G ±1+10/G *	μV μV/°C μV/ν μV/mo Ω pF Ω pF V
Safe Input Voltage Common-Mode Rejection	V _{CM} =±10V, ΔR _S =1kΩ			±40			*	V
	G=1 G=10 G=100 G=1000	80 96 110 115	99 114 123 123		75 90 106 106	90 106 110 110		dB dB dB dB
BIAS CURRENT vs Temperature Offset Current vs Temperature			± 0.5 ± 8 ± 0.5 ± 8	±2 ±2		* * *	±5 *	nA pA/°C nA pA/°C
NOISE, Voltage, RTI ⁽¹⁾ : f=10Hz f=10Hz f=1kHz f=1kHz f_B=0.1Hz to 10Hz Noise Current f=10Hz f=1kHz	G≥100, $R_S=0\Omega$ G≥100, $R_S=0\Omega$ G≥100, $R_S=0\Omega$ G≥100, $R_S=0\Omega$		16 13 13 0.4 0.4 0.2			* * * *		nV/√Hz nV/√Hz nV/√Hz μVp-p pA/√Hz pA/√Hz
f _B =0.1Hz to 10Hz			18			*		рАр-р
GAIN, Error Gain vs Temperature Nonlinearity	$\begin{array}{c} G=1\\ G=10\\ G=100\\ G=100\\ G=1\ to\ 1000\\ G=1\\ G=10\\ G=10\\ G=100\\ G=1000\\ G=1000\end{array}$		$\begin{array}{c} \pm 0.005 \\ \pm 0.01 \\ \pm 0.01 \\ \pm 0.02 \\ \pm 2.5 \\ \pm 0.0004 \\ \pm 0.0004 \\ \pm 0.0004 \\ \pm 0.0008 \end{array}$	$\begin{array}{c} \pm 0.024 \\ \pm 0.024 \\ \pm 0.024 \\ \pm 0.05 \\ \pm 10 \\ \pm 0.001 \\ \pm 0.002 \\ \pm 0.002 \\ \pm 0.01 \end{array}$		* * * * * * *	$\begin{array}{c} \pm 0.05 \\ \pm 0.05 \\ \pm 0.05 \\ \pm 0.1 \\ * \\ \pm 0.002 \\ \pm 0.004 \\ \pm 0.004 \\ \pm 0.02 \end{array}$	% % % ppm/°C % of FSR % of FSR % of FSR % of FSR
OUTPUT								
Voltage, Positive ⁽²⁾ Negative ⁽²⁾ Load Capacitance Stability Short Circuit Current	I_{O} =5mA, T_{MIN} to T_{MAX} I_{O} =–5mA, T_{MIN} to T_{MAX}	(V+)–1.5 (V–)+1.5	(V+)-1.3 (V-)+1.3 1000 +23/-17		*	* * *		V V pF mA
FREQUENCY RESPONSE								
Bandwidth, –3dB Slew Rate Settling Time ⁽³⁾ , 0.1% 0.01% Overload Recovery	$\begin{array}{c} G=1\\ G=10\\ G=100\\ G=1000\\ V_0=\pm 10V,\ G=10\\ G=1\\ G=10\\ G=100\\ G=1000\\ G=1\\ G=10\\ G=100\\ G=1000\\ G=1000\\ G=000\\ 50\% \ Overdrive \end{array}$	0.3	1 80 10 1 0.7 22 23 100 1000 23 28 140 1300 70			* * * * * * * * * * * *		MHz kHz kHz μs μs μs μs μs μs μs μs μs μs
DIGITAL LOGIC Digital Ground Voltage, V _{DG}		V–		(V+)−4	*		*	v
Digital Clour Voltage Digital Low Voltage Digital Input Current Digital High Voltage		V- V- V _{DG} +2	1	(V+)-4 V _{DG} +0.8V V+	*	*	*	ν V μΑ V
POWER SUPPLY, Voltage Current	\/−0\/	±4.5	±15 +5.2/-4.2	±18	*	*	* ±7.5	V mA
Current TEMPERATURE RANGE Specification Operating θ_{JA}	V _{IN} =0V	-40 -40	80	±6.5 +85 +125	*	*	±7.5 * *	mA °C °C °C/W

* Specification same as PGA204BP.

NOTES: (1) Input-referred noise voltage varies with gain. See typical curves. (2) Output voltage swing is tested for ±10V min on ±11.4V power supplies. (3) Includes time to switch to a new gain.



SPECIFICATIONS

ELECTRICAL

At $T_{A} = +25^{\circ}C$, $V_{S} = \pm 15V$, and $R_{I} = 2k\Omega$ unless otherwise noted.

PGA205 G=1, 2, 4, 8V/V

		Р	F					
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT Offset Voltage, RTI vs Temperature vs Power Supply Long-Term Stability Impedance, Differential	T_A =+25°C T_A =T _{MIN} to T _{MAX} V_S =±4.5V to ±18V		±10+20/G ±0.1+0.5/G 0.5+2/G ±0.2+0.5/G 10 ¹⁰ 6	±50+100/G ±0.25+5/G 3+10/G		±25+30/G ±0.25+5/G * *	±125+500/G ±1+10/G *	μV μV/°C μV/ν μV/mo Ω pF
Common-Mode Input Common-Mode Range Safe Input Voltage Common-Mode Rejection	V_{O} =0V (see text) V_{CM} =±10V, ΔR_{S} =1k Ω	±10.5	10 ¹⁰ 6 ±12.7	±40	*	*	*	Ω pF V V
	G=1 G=2 G=4 G=8	80 85 90 95	94 100 106 112		75 80 85 89	88 94 100 106		dB dB dB dB
BIAS CURRENT			±0.5	±2		*	±5	nA
vs Temperature Offset Current vs Temperature			±8 ±0.5 ±8	±2		* * *	*	pA/°C nA pA/°C
Noise Voltage, RTI ⁽¹⁾ : f=10Hz f=10Hz f=100Hz f=1kHz f=0.1Hz to 10Hz Noise Current	G=8, R _S =0Ω G=8, R _S =0Ω G=8, R _S =0Ω G=8, R _S =0Ω		19 15 15 0.5			* * *		nV/√Hz nV/√Hz nV/√Hz μVp-p
f=10Hz f=1kHz f _B =0.1Hz to 10Hz			0.4 0.2 18			* * *		pA/√Hz pA/√Hz pAp-p
GAIN, Error	G=1 G=2 G=4 G=8		±0.005 ±0.01 ±0.01 ±0.01	± 0.024 ± 0.024 ± 0.024 ± 0.024		* * *	± 0.05 ± 0.05 ± 0.05 ± 0.05	% % % %
Gain vs Temperature Nonlinearity	G=1 to 8 G=1 G=2 G=4 G=8		$\begin{array}{c} \pm 2.5 \\ \pm 0.00024 \\ \pm 0.00024 \\ \pm 0.00024 \\ \pm 0.00024 \end{array}$	± 10 ± 0.001 ± 0.002 ± 0.002 ± 0.002		* * * *	* ±0.002 ±0.004 ±0.004 ±0.004	ppm/°C % of FSF % of FSF % of FSF % of FSF
OUTPUT Voltage, Positive ⁽²⁾ Negative ⁽²⁾ Load Capacitance Stability Short Circuit Current	$I_{O}{=}5mA,~T_{MIN}$ to T_{MAX} $I_{O}{=}{-}5mA,~T_{MIN}$ to T_{MAX}	(V+)–1.5 (V–)+1.5	(V+)-1.3 (V-)+1.3 1000 +23/-17		*	* * *		V V pF mA
FREQUENCY RESPONSE			+23/-17					IIIA
Slew Rate Settling Time ⁽³⁾ , 0.1%	$\begin{array}{c} G=1\\ G=2\\ G=4\\ G=8\\ V_{O}=\pm 10V,\ G=8\\ G=1\\ G=2\\ G=4\\ G=8\\ G=1\\ G=2\\ \end{array}$	0.3	1 400 200 100 0.7 22 22 23 23 23 23 23 23		×	* * * * * * * * * * * *		MHz kHz kHz μs μs μs μs μs
Overload Recovery	G=2 G=4 G=8 50% overdrive		23 25 28 70			* * *		μs μs μs μs
DIGITAL LOGIC INPUTS Digital Ground Voltage, V _{DG} Digital Low Voltage Digital Low Current		V- V-	1	(V+)–4 V _{DG} +0.8V	*	*	*	V V μA
Digital High Voltage POWER SUPPLY, Voltage		V _{DG} +2 ±4.5	±15	V+ ±18	*	*	*	V V
Current	V _{IN} =0V		+5.2/-4.2	±6.5		*	±7.5	mA
TEMPERATURE RANGE Specification Operating θ _{JA}		-40 -40	80	+85 +125	*	*	*	°C ℃ W\C

* Specification same as PGA204BP. NOTES: (1) Input-referred noise voltage varies with gain. See typical curves. (2) Output voltage swing is tested for ±10V min on ±11.4V power supplies. (3) Includes time to switch to a new gain.



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
PGA204AP	16-Pin Plastic DIP	180
PGA204BP	16-Pin Plastic DIP	180
PGA204AU	SOL-16 Surface Mount	211
PGA204BU	SOL-16 Surface Mount	211
PGA205AP	16-Pin Plaseic DIP	180
PGA205BP	16-Pin Plastic DIP	180
PGA205AU	SOL-16 Surface Mount	211
PGA205BU	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

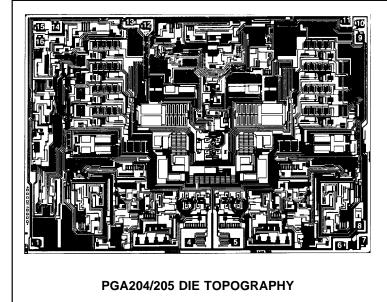
MODEL	GAINS	PACKAGE	TEMPERATURE RANGE
PGA204AP	1, 10, 100, 1000V/V	16-Pin Plastic DIP	–40 to +85°C
PGA204BP	1, 10, 100, 1000V/V	16-Pin Plastic DIP	–40 to +85°C
PGA204AU	1, 10, 100, 1000V/V	SOL-16 Surface-Mount	–40 to +85°C
PGA204BU	1, 10, 100, 1000V/V	SOL-16 Surface-Mount	−40 to +85°C
PGA205AP	1, 2, 4, 8V/V	16-Pin Plastic DIP	-40 to +85°C
PGA205BP	1, 2, 4, 8V/V	16-Pin Plastic DIP	-40 to +85°C
PGA205AU	1, 2, 4, 8V/V	SOL-16 Surface-Mount	-40 to +85°C
PGA205BU	1, 2, 4, 8V/V	SOL-16 Surface-Mount	-40 to +85°C

ABSOLUTE MAXIMUM RATINGS

upply Voltage±18V nalog Input Voltage Range±40V	
nalog Input Voltage Range±40V	
ogic Input Voltage Range $\pm V_S$	
utput Short-Circuit (to ground)	
perating Temperature40°C to +125°C	
torage Temperature40°C to +125°C	
unction Temperature +150°C	
ead Temperature (soldering -10s) +300°C	



DICE INFORMATION



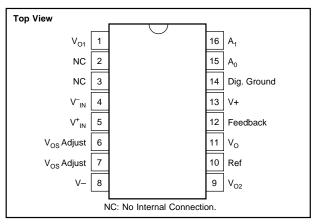
PAD	FUNCTION	PAD	FUNCTION
1	V _{O1}	9	V _{O2}
2	_	10	Ref
3	-	11	Vo
4	V-IN	12	Feedback
5	V+INI	13	V+
6	V _{OS} Adj V _{OS} Adj V–	14	Dig. Ground
7	V _{OS} Adj	15	- A ₀
8	V-	16	A ₁

Substrate Bias: Internally connected to V- power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	186 x 130 ±5	4.72 x 3.30 ±0.13
Die Thickness Min. Pad Size	20 ±3 4 x 4	0.51 ±0.08 0.1 x 0.1
Backing		Gold

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

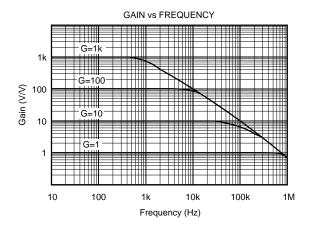
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

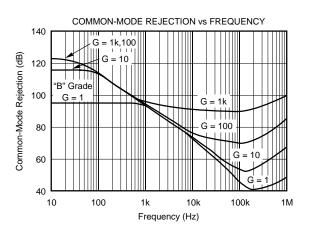
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

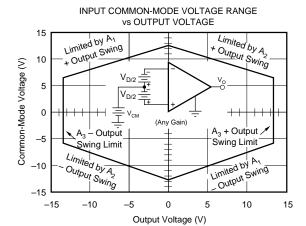


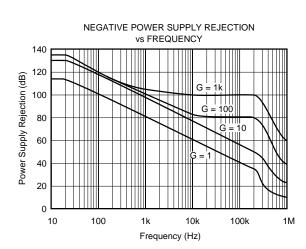
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

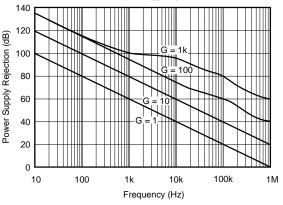


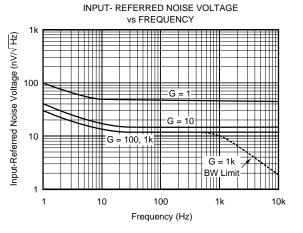






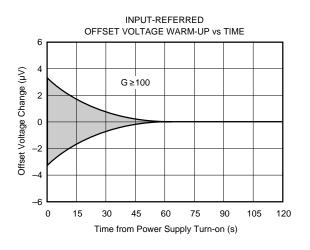
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY

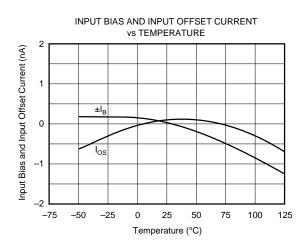


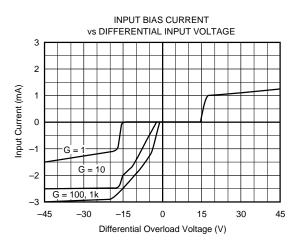


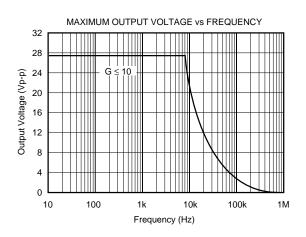


At T_A = +25°C, and V_S = \pm 15V, unless otherwise noted.

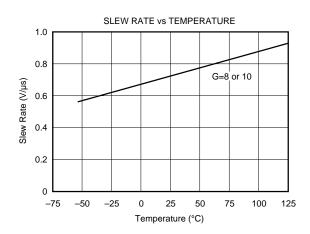








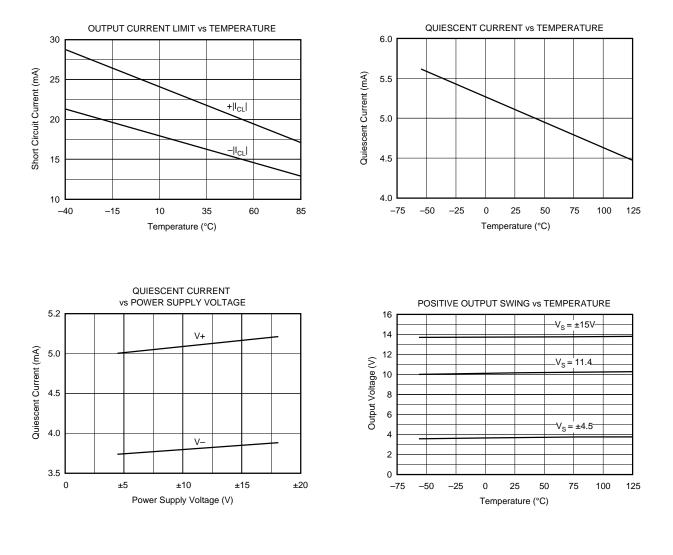
INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE 3 Both Inputs 2 $||_{b1}| + ||_{b2}|$ Input Bias Current (mA) One Input 1 Over-Voltage Protection 0 Over-Voltage Normal Protection Operation -1 One Input -2 Both Inputs -3 -30 -15 15 30 45 -45 0 Common-Mode Voltage (V)

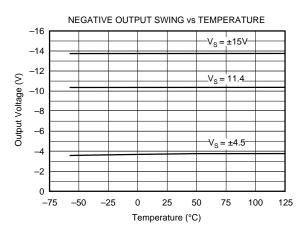




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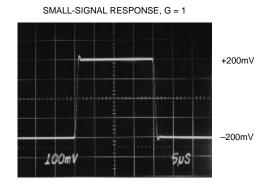
At $\rm T_{A}$ = +25°C, and $\rm V_{S}$ = ±15V, unless otherwise noted.

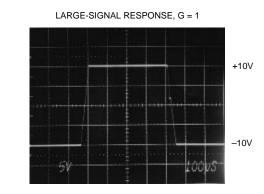




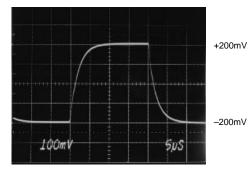
BURR-BROWN® PGA204/205

At T_{A} = +25°C, and V_{S} = $\pm 15V,$ unless otherwise noted.

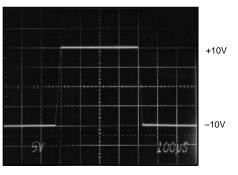


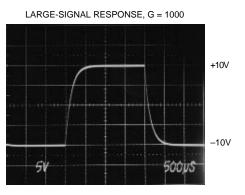


SMALL-SIGNAL RESPONSE, G = 10





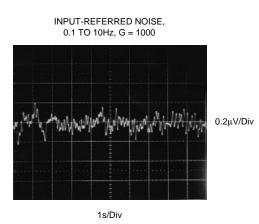




SMALL-SIGNAL RESPONSE, G = 1000 +200mV -200mV -200mV



At $T_A = +25^{\circ}C$, and $V_S = \pm 15V$, unless otherwise noted.

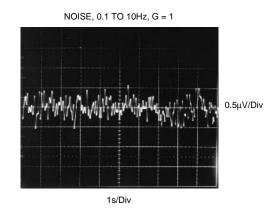


APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the PGA204/205. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G=1).

The PGA204/205 has an output feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. The output Feedback connection can



be used to sense the output voltage directly at the load for best accuracy.

DIGITAL INPUTS

The digital inputs A_0 and A_1 select the gain according to the logic table in Figure 1. Logic "1" is defined as a voltage greater than 2V above digital ground potential (pin 14). Digital ground can be connected to any potential from the V– power supply to 4V less than V+. Digital ground is normally connected to ground. The digital inputs interface directly CMOS and TTL logic components.

Approximately 1µA flows out of the digital input pins when a logic "0" is applied. Logic input current is nearly zero with a logic "1" input. A constant current of approximately

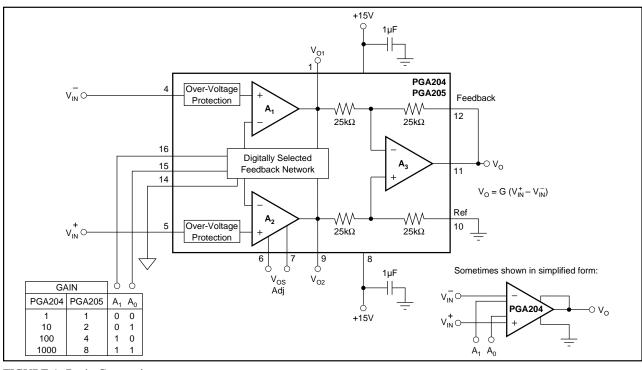


FIGURE 1. Basic Connections.



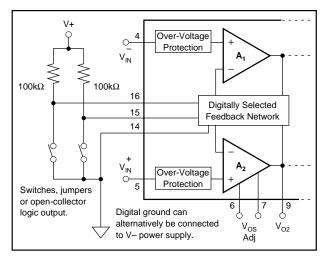


FIGURE 2. Switch or Jumper-Selected Digital Inputs.

1.3mA flows in the digital ground pin. It is good practice to return digital ground through a separate connection path so that analog ground is not affected by the digital ground current.

The digital inputs, A_0 and A_1 , are not latched; a change in logic inputs immediately selects a new gain. Switching time of the logic is approximately 1µs. The time to respond to gain change is effectively the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see settling time specifications).

Many applications use an external logic latch to access gain control data from a high speed data bus (see Figure 7). Using an external latch isolates the high speed digital bus from sensitive analog circuitry. Locate the latch circuitry as far as practical from analog circuitry. Some applications select gain of the PGA204/205 with switches or jumpers. Figure 2 shows pull-up resistors connected to assure a noise-free logic "1" when the switch, jumper or open-collector logic is open or off. Fixed-gain applications can connect the logic inputs directly to V+ or V– (or other valid logic level); no resistor is required.

OFFSET VOLTAGE

Voltage offset of the PGA204/205 consists of two components—input stage offset and output stage offset. Both components are specified in the specification table in equation form:

$$V_{\rm OS} = V_{\rm OSI} + V_{\rm OSO} / G \tag{1}$$

where:

V_{OS} total is the combined offset, referred to the input.

 V_{OSI} is the offset voltage of the input stage, A_1 and A_2 .

 V_{OSO} is the offset voltage of the output difference amplifier, A_3 .

 V_{OSI} and V_{OSO} do not change with gain. The composite offset voltage V_{OS} changes with gain because of the gain term in equation 1. Input stage offset dominates in high gain (G≥100); both sources of offset may contribute at low gain (G=1 to 10).

OFFSET TRIMMING

Both the input and output stages are laser trimmed for very low offset voltage and drift. Many applications require no external offset adjustment.

Figure 3 shows an optional input offset voltage trim circuit. This circuit should be used to adjust only the input stage offset voltage of the PGA204/205. Do this by programming

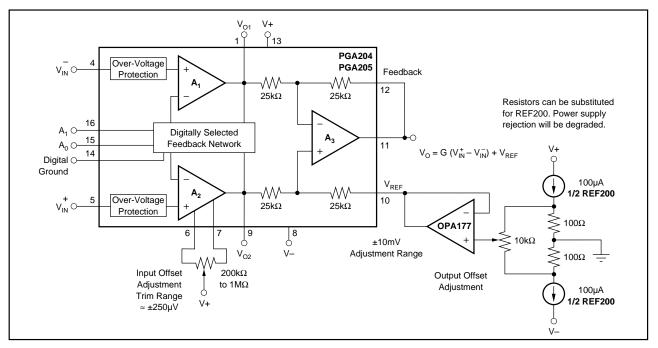


FIGURE 3. Optional Offset Voltage Trim Circuit.



it to its highest gain and trimming the output voltage to zero with the inputs grounded. Drift performance usually improves slightly when the input offset is nulled with this procedure.

Do not use the input offset adjustment to trim system offset or offset produced by a sensor. Nulling offset that is not produced by the input amplifiers will increase temperature drift by approximately $3.3\mu V/^{\circ}C$ per 1mV of offset adjustment.

Many applications that need input stage offset adjustment do not need output stage offset adjustment. Figure 3 also shows a circuit for adjusting output offset voltage. First, adjust the input offset voltage as discussed above. Then program the device for G=1 and adjust the output to zero. Because of the interaction of these two adjustments at G=8, the PGA205 may require iterative adjustment.

The output offset adjustment can be used to trim sensor or system offsets without affecting drift. The voltage applied to the Ref terminal is summed with the output signal. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering the trim voltage with an op amp as shown.

NOISE PERFORMANCE

The PGA204/205 provides very low noise in most applications. Low frequency noise is approximately 0.4μ Vp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of "low noise" chopper-stabilized amplifiers.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the PGA204/205 is extremely high approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than $\pm 1nA$ (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the PGA204/205 is to operate properly. Figure 4 shows provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the PGA204/205 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 4). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due bias current and better common-mode rejection.

Many sources or sensors inherently provide a path for input bias current (e.g. the bridge sensor shown in Figure 4). These applications do not require additional resistor(s) for proper operation.

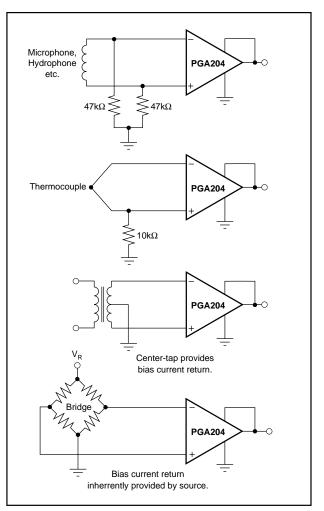


FIGURE 4. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the PGA204/205 is approximately $\pm 12.7V$ (or 2.3V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A₁ and A₂. The common-mode range is related to the output voltage of the complete amplifier—see performance curve "Input Common-Mode Range vs Output Voltage".

A combination of common-mode and differential input voltage can cause the output of A_1 or A_2 to saturate. Figure 5 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier, A_3 . For applications where input common-mode range must be maximized, limit the output voltage swing by selecting a lower gain of the PGA204/205 (see performance curve "Input Common-Mode Voltage Range vs Output Voltage"). If necessary, add gain after the PGA204/205 to increase the voltage swing.



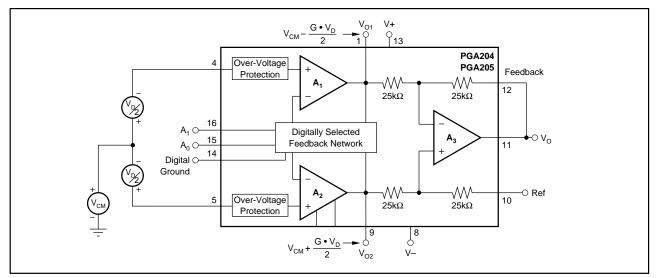


FIGURE 5. Voltage Swing of A_1 and A_2 .

Input-overload often produces an output voltage that appears normal. For example, consider an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the PGA204/205 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the PGA204/205 are individually protected for voltages up to ± 40 V. For example, a condition of -40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

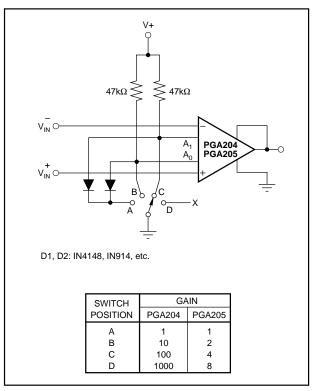


FIGURE 6. Switch-Selected PGIA.

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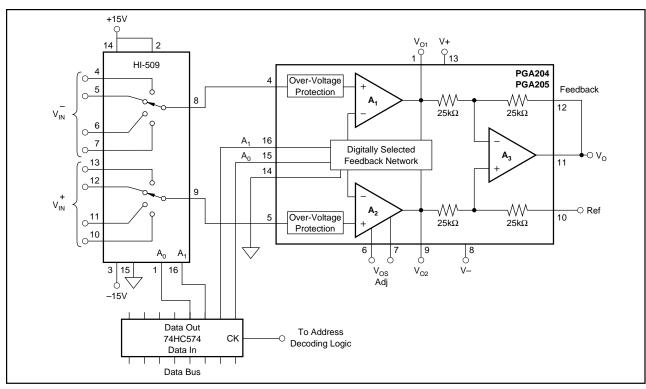


FIGURE 7. Multiplexed-Input Programmable Gain IA.

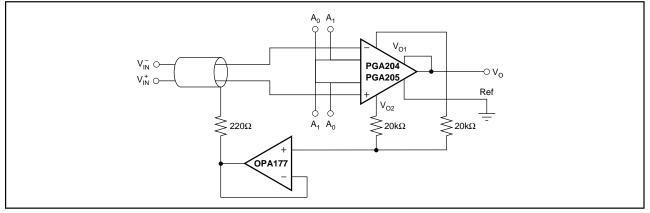
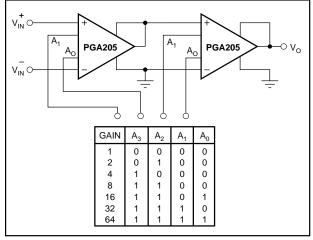
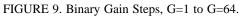


FIGURE 8. Shield Drive Circuit.





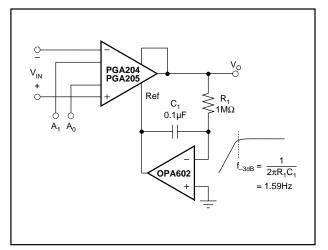


FIGURE 10. AC-Coupled PGIA.



μħ. **TEXAS** TRUMENTS www.ti.com

16-Feb-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
PGA204AP	ACTIVE	PDIP	Ν	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
PGA204APG4	ACTIVE	PDIP	Ν	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
PGA204AU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA204AU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA204AU/1KE4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA204AUE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA204AUG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA204BP	ACTIVE	PDIP	Ν	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
PGA204BPG4	ACTIVE	PDIP	Ν	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
PGA204BU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA204BU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA204BU/1KE4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA204BUE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA205AP	ACTIVE	PDIP	Ν	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
PGA205APG4	ACTIVE	PDIP	Ν	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
PGA205AU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA205AU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA205AU/1KG4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA205AUG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA205BP	ACTIVE	PDIP	Ν	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
PGA205BPG4	ACTIVE	PDIP	Ν	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
PGA205BU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
PGA205BUG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
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 LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.



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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TEXAS INSTRUMENTS





TAPE AND REEL INFORMATION

TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

All dimensions are nomin	al											
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA204AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PGA204BU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PGA205AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

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PACKAGE MATERIALS INFORMATION

6-Jun-2012



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA204AU/1K	SOIC	DW	16	1000	346.0	346.0	33.0
PGA204BU/1K	SOIC	DW	16	1000	346.0	346.0	33.0
PGA205AU/1K	SOIC	DW	16	1000	346.0	346.0	33.0

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