



14-Bit, Parallel Input Multiplying Digital-to-Analog Converter

FEATURES

- ±0.5 LSB DNL
- ±1 LSB INL
- 14-Bit Monotonic
- Low Noise: 10 nV/√Hz
 Low Power: I_{DD} = 2 μA
- Analog Power Supply: +2.7 V to +5.5 V
- 1.66 mA Full-Scale Current, with V_{REF} = 10 V
- Settling Time: 0.5 μs
- 4-Quadrant Multiplying Reference
- Reference Bandwidth: 8 MHz
- Reference Input: ±15 V
- Reference Dynamics: –105 dB THD
- SSOP-28 Package
- Industry-Standard Pin Configuration

APPLICATIONS

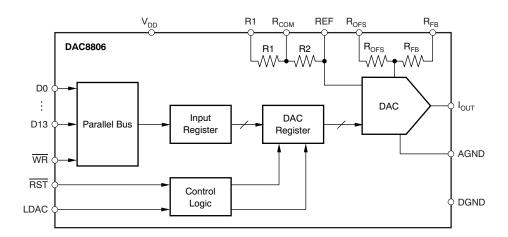
- Automatic Test Equipment
- Instrumentation
- Digitally Controlled Calibration
- Industrial Control PLCs

DESCRIPTION

The DAC8806, a multiplying digital-to-analog converter (DAC), is designed to operate from a single 2.7 V to 5.5 V supply.

The applied external reference input voltage V_{REF} determines the full-scale output current. An internal feedback resistor (R_{FB}) provides temperature tracking for the full-scale output when combined with an external, current-to-voltage (I/V) precision amplifier.

A parallel interface offers high-speed communications. The DAC8806 is packaged in a space-saving SSOP-28 package and has an industry-standard pinout.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUC	MINIMUM RELATIVE ACCURACY T (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE- LEAD (DESIGNATOR)	EAD TEMPERATURE		ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8806		. 1	DB-28 (SSOP) -40°C to +85°C		DAC8806	DAC8806IDB	Tubes, 48
DACOOU) ±1	±1	DB-20 (330P)	-40 C to +65 C	DAC6606	DAC8806IDBR	Tape and Reel, 2000

⁽¹⁾ For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted)

		DAC8806	UNIT
V _{DD} to GND		-0.3 to +7	V
Digital input volta	age to GND	-0.3 to +V _{DD} + 0.3	V
V (I _{OUT}) to GND		-0.3 to +V _{DD} + 0.3	V
Operating tempe	rature range	-40 to +85	°C
REF, R _{OFS} , R _{FB} ,	R1, R _{COM} to AGND, and DGND	±25	V
Storage tempera	ture range	-65 to +150	°C
Junction tempera	ature range (T _J max)	+125	°C
Power dissipation	n	$(T_J \max - T_A)/R_{\theta JA}$	W
Thermal impedar	nce, R _{eJA}	55	°C/W
ESD roting	Human body model (HBM)	4000	V
ESD rating	Charged device model (CDM)	1000	V

⁽¹⁾ Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

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ELECTRICAL CHARACTERISTICS

All specifications at -40° C to $+85^{\circ}$ C, V_{DD} = +2.7 V to +5.5 V, I_{OUT} = virtual GND, GND = 0 V, V_{REF} = 10 V, and T_A = full operating temperature, unless otherwise noted.

			DAC8806 MIN TYP MAX		
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE				-	
Resolution		14			Bits
Relative accuracy	DAC8806			±1	LSB
Differential nonlinearity			±0.5	±1	LSB
Output leakage current	Data = 0000h, T _A = +25°C			5	nA
Output leakage current	Data = 0000h, T _A = T _{MAX}			10	nA
Full-scale gain error	Unipolar, data = 3FFFh		1	±4	LSB
	Bipolar, data = 3FFFh		1	±4	LSB
Full-scale temperature coefficient			1	2	ppm/°C
Bipolar zero scale error			±1	±3	LSB
PSRR	Power-supply rejection ratio; V _{DD} = 5 V ±10%		±0.1	±1	LSB/V
OUTPUT CHARACTERISTICS ⁽¹⁾		"		1	
Output current			1.66		mA
Output capacitance	Code dependent		50		pF
REFERENCE INPUT					
V _{REF} range		-15		15	V
R _{REF}	Input resistance (unipolar)	4.5	6	7.5	kΩ
Input capacitance			5		pF
R1/R2	R1/R2 resistance (bipolar)	9	12	15	kΩ
R _{OFS} , R _{FB}	Feedback and offset resistance	9	12	15	kΩ
LOGIC INPUTS AND OUTPUT ⁽¹⁾				<u> </u>	
Input low voltage V _{IL}	V _{DD} = +2.7 V			0.6	V
V _{IL}	V _{DD} = +5 V			0.8	V
	V _{DD} = +2.7 V	2.1			V
V _{IH}	V _{DD} = +5 V	2.4			V
Input leakage current I _{IL}			0.001	1	μА
Input capacitance C _{IL}				8	pF
INTERFACE TIMING, V _{DD} = +5.0V ⁽¹⁾	(See Figure 40 and Table 1)			-	
t _{DS}	Data to WR setup time	20			ns
t _{DH}	Data to WR hold time	0			ns
t _{WR}	WR pulse width	20			ns
	LDAC pulse width	20			ns
Data setup time t _{RST}		20			ns
Data hold time t _{LWD}	WR to LDAC delay time	0			ns
INTERFACE TIMING, V _{DD} = +2.7V ⁽¹⁾	(See Figure 40 and Table 1)			1	
t _{DS}	Data to WR setup time	35			ns
t _{DH}	Data to WR hold time	0			ns
t _{WR}	WR pulse width	35			ns
t _{LDAC}	LDAC pulse width	35			ns
Data setup time t _{RST}		35			ns
Data hold time t _{LWD}		0			ns

⁽¹⁾ Specified by design and characterization; not production tested.



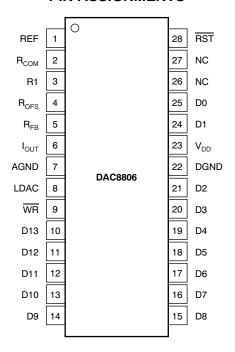
ELECTRICAL CHARACTERISTICS (continued)

All specifications at -40° C to $+85^{\circ}$ C, V_{DD} = +2.7 V to +5.5 V, I_{OUT} = virtual GND, GND = 0 V, V_{REF} = 10 V, and T_A = full operating temperature, unless otherwise noted.

			DAC8806				
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS		
POWER REQUIREMENTS		•		,			
V_{DD}		2.7		5.5	V		
I _{DD} (normal operation)	Logic inputs = 0V			5	μΑ		
V _{DD} = +4.5 V to +5.5 V	$V_{IH} = V_{DD}$ and $V_{IL} = GND$		3	5	μΑ		
V _{DD} = +2.7 V to +3.6 V	$V_{IH} = V_{DD}$ and $V_{IL} = GND$		1	2.5	μΑ		
AC CHARACTERISTICS ⁽²⁾							
Output current settling time			0.5		μs		
Reference multiplying BW	V _{REF} = 5 V _{PP} , Data = 3FFFh		8		MHz		
DAC glitch impulse	V _{REF} = 0 V to 10 V, Data = 1FFFh to 2000h to 1FFFh		2		nV-s		
Feedthrough error V _{OUT} /V _{REF}	Data = 0000h, V _{REF} = 10 kHz; ±10 V _{PP}		-70		dB		
Digital feedthrough	L_{DAC} = logic low, V_{REF} = -10 V to +10 V Any code change		2		nV-s		
Total harmonic distortion	V _{REF} = 6 V _{RMS} , Data = 3FFF, f = 1 kHz		-105		dB		
Output spot noise voltage			10		nV/√ Hz		

⁽²⁾ Specified by design and characterization; not production tested.

PIN ASSIGNMENTS



TERMINAL FUNCTIONS

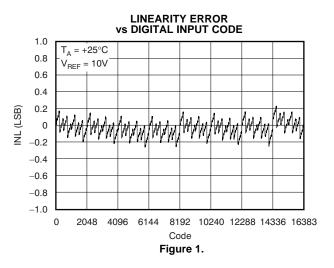
PIN#	NAME	DESCRIPTION		
1	REF	Reference input and 4-quadrant Resistor (R2).		
2	R _{COM}	Center tap of two 4-quadrant resistors (R1 and R2).		
3	R1	4-quadrant resistor (R1).		
4	R _{OFS}	Bipolar offset resistor		
5	R _{FB}	Internal matching feedback resistor		
6	I _{OUT}	DAC current output		
7	AGND	Analog ground		
8	Digital input load DAC control. When LDAC is h data is loaded from input register into a DAC register, updating the DAC output.			
9	WR	Write control digital input. Active low. When WR is taken to logic low, data is loaded from the digital input pins (D0–D13) into a14-bit input register.		
10–21	D13-D2	Digital input data bits. D13 is MSB.		
22	DGND	Digital ground		
23	V_{DD}	Positive power supply		
24, 25	D1, D0	Digital Input data bits. D0 is LSB.		
26, 27	NC	No connection		
28	RST	Reset. Active low. When RST is taken to logic low, the DAC register is set to zero code, resulting in the DAC output being set to 0 V.		

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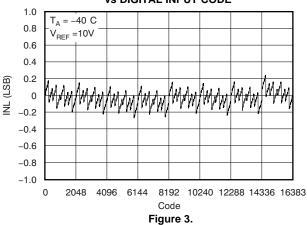
TYPICAL CHARACTERISTICS: V_{DD} = +5V

At $T_A = +25$ °C, unless otherwise noted.



DIFFERENTIAL LINEARITY ERROR VS DIGITAL INPUT CODE 1.0 $T_A = +25^{\circ}C$ 0.8 $V_{REF} = 10V$ 0.6 0.4 DNL (LSB) 0.2 0 -0.2-0.4 -0.6-0.8-1.00 2048 4096 6144 8192 10240 12288 14336 16383

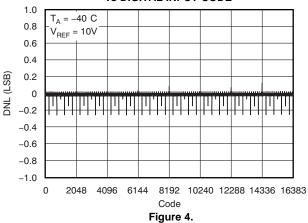
LINEARITY ERROR VS DIGITAL INPUT CODE



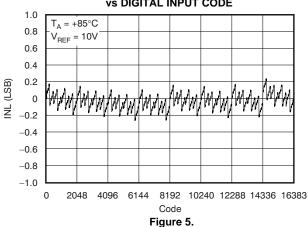
DIFFERENTIAL LINEARITY ERROR VS DIGITAL INPUT CODE

Code

Figure 2.



LINEARITY ERROR VS DIGITAL INPUT CODE



DIFFERENTIAL LINEARITY ERROR VS DIGITAL INPUT CODE

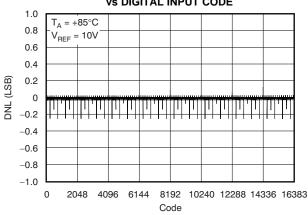
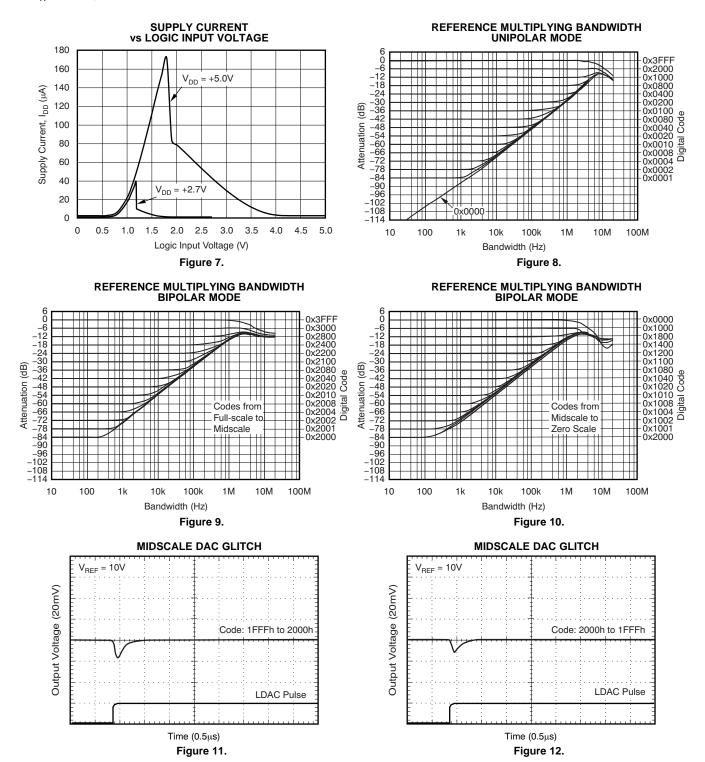


Figure 6.



TYPICAL CHARACTERISTICS: $V_{DD} = +5V$ (continued)

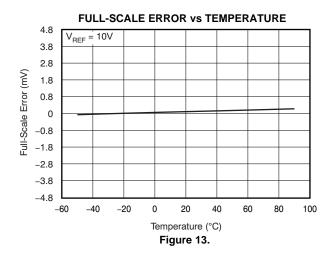
At $T_A = +25$ °C, unless otherwise noted.

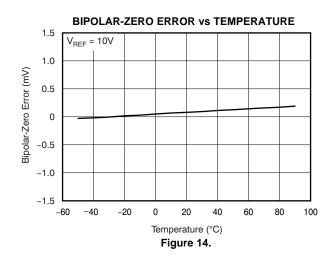




TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At $T_A = +25$ °C, unless otherwise noted.

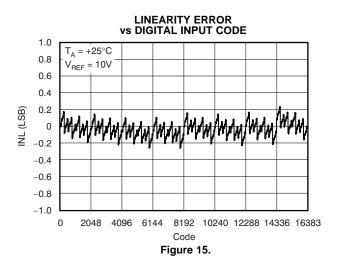


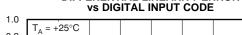




TYPICAL CHARACTERISTICS: V_{DD} = +2.7V

At $T_A = +25^{\circ}C$, unless otherwise noted.





DIFFERENTIAL LINEARITY ERROR

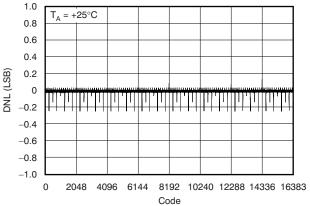
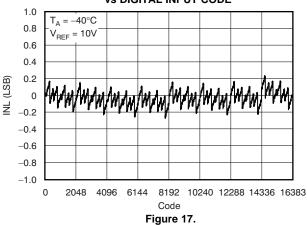


Figure 16.





DIFFERENTIAL LINEARITY ERROR VS DIGITAL INPUT CODE

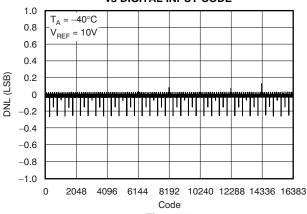


Figure 18.

LINEARITY ERROR VS DIGITAL INPUT CODE

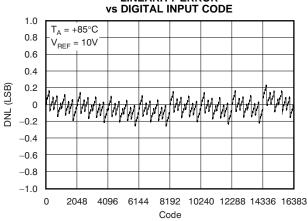


Figure 19.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

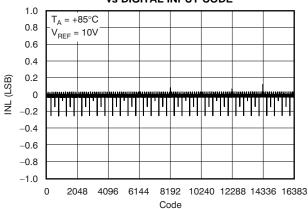


Figure 20.



TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At $T_A = +25$ °C, unless otherwise noted.

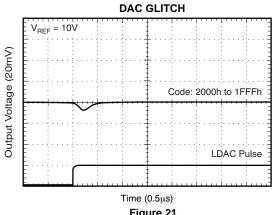


Figure 21.

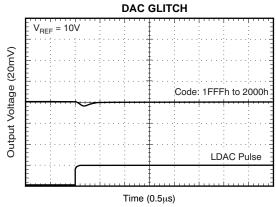
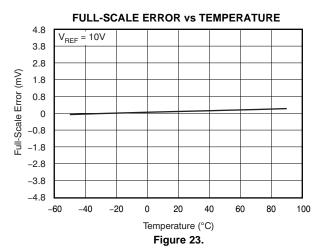
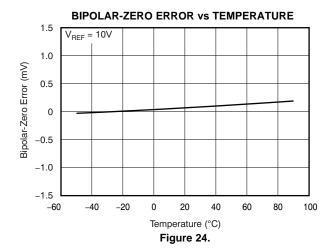


Figure 22.

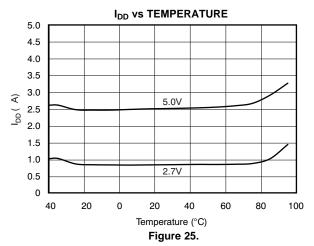


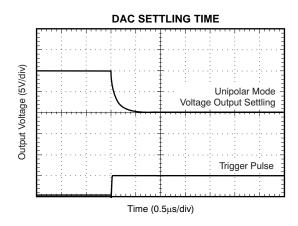




TYPICAL CHARACTERISTICS

At $T_A = +25^{\circ}C$, unless otherwise noted.





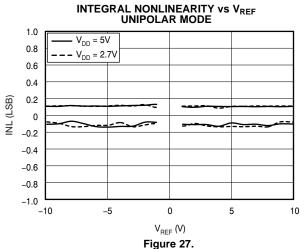
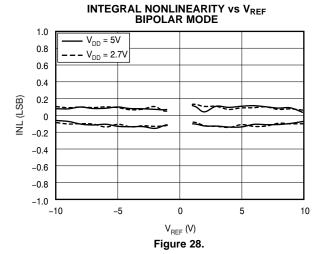
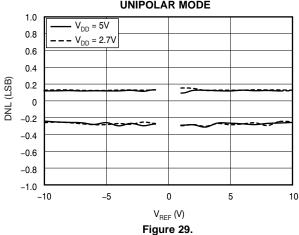


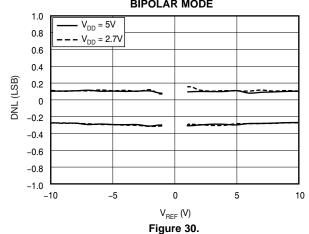
Figure 26.



DIFFERENTIAL NONLINEARITY vs V_{REF}UNIPOLAR MODE



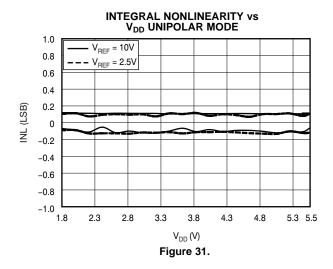
DIFFERENTIAL NONLINEARITY vs V_{REF} BIPOLAR MODE

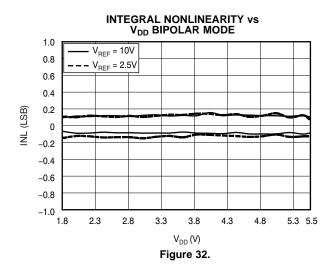


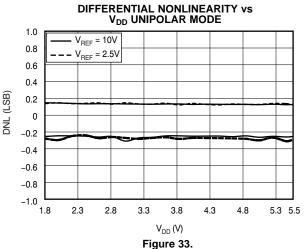


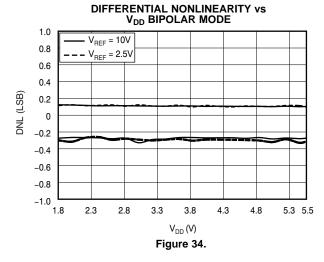
TYPICAL CHARACTERISTICS (continued)

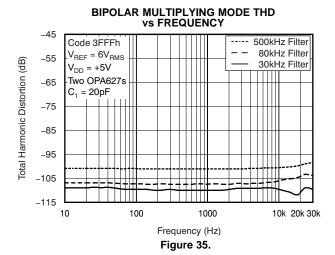
At $T_A = +25^{\circ}C$, unless otherwise noted.

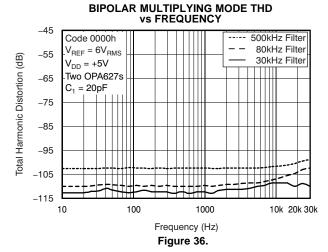






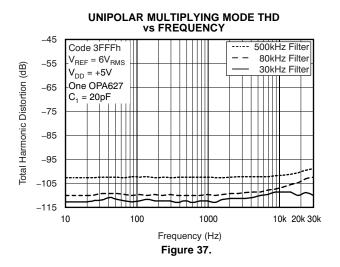






TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^{\circ}C$, unless otherwise noted.



THEORY OF OPERATION

The DAC8806 is a multiplying, single-channel current output, 14-bit DAC. The architecture, illustrated in Figure 38, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to GND or to the I_{OUT} terminal. The I_{OUT} terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input (V_{REF}) that determines the DAC full-scale current. The R-2R ladder presents a code independent load impedance to the external reference of 6 k Ω ±25%. The external reference voltage can vary in a range of –10 V to +10 V, thus providing bipolar I_{OUT} current operation. By using an external I/V converter op amp and the R_{FB} resistor in the DAC8806, an output voltage range of $-V_{REF}$ to $+V_{REF}$ can be generated.

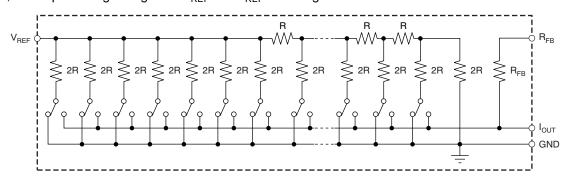


Figure 38. Equivalent R-2R DAC Circuit

The DAC output voltage is determined by V_{REF} and the digital data (D) according to Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{D}{16384} \tag{1}$$

Each DAC code determines the 2R-leg switch position to either GND or I_{OUT} . The external I/V converter op amp noise gain will also change because the DAC output impedance (as seen looking into the I_{OUT} terminal) changes versus code. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC I_{OUT} terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC8806 because of offset modulation versus DAC code. For best linearity performance of the DAC8806, an op amp (OPA277) is recommended; see Figure 39. This circuit allows V_{REF} to swing from -10 V to +10 V.

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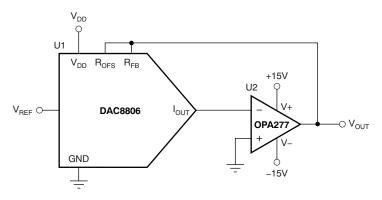


Figure 39. Voltage Output Configuration

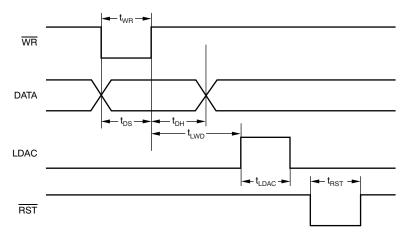


Figure 40. DAC8806 Timing Diagram

Table 1. Function of Control Inputs

CONTROL INPUTS		JTS						
RST	WR	LDAC	REGISTER OPERATION					
0	Х	Х	Asynchronous operation. The DAC register is set to zero code, resulting in the DAC output being set to 0 V. The DAC input register contents are not reset by the RST signal.					
1	0	0	oad the input register with all 14 data bits.					
1	1	1	Load the DAC register with the contents of the input register.					
1	0	1	The input and DAC register are transparent.					
1	1 7 7		LDAC and WR are tied together and programmed as a pulse. The 14 data bits are loaded into the input register on the falling edge of the pulse and then loaded into the DAC register on the rising edge of the pulse.					
1	1	0	No register operation.					

APPLICATION INFORMATION

Multiplying Mode THD versus Frequency

Figure 35 and Figure 36 show the DAC8806 bipolar 4-quadrant multiplying mode total harmonic distortion (THD) versus frequency. Figure 35 shows the bipolar mode THD with the DAC8806 set to a full-scale code of 3FFFh. Figure 36 shows the bipolar multiplying mode THD with the DAC8806 set to a minus full-scale code of 0000h. In both graphs, two OPA627s are used for both the DAC output op amp and the reference inverting amplifier. A 6 V_{RMS} sine wave is used for the reference input V_{REF} and is swept in frequency from 10 Hz to 30 kHz. The THD levels versus frequency are illustrated at various DAC output filtering levels using an external ac-coupled low-pass filter.

Figure 37 illustrates the DAC8806 unipolar 2-quadrant multiplying mode THD versus frequency. The DAC8806 is set to a full-scale code of 3FFFh. A single OPA627 is used for the DAC output op amp.

Stability Circuit

For a current-to-voltage (I/V) design, as shown in Figure 41, the DAC8806 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and laid out according to correct printed circuit board (PCB) layout design. For each code change there is a step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, a compensation capacitor C1 (4 pF to 20 pF, typ) can be added to the design for circuit stability, as shown in Figure 41.

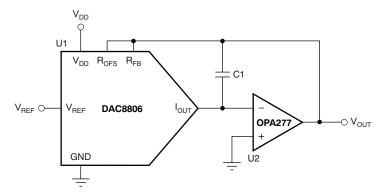


Figure 41. Gain Peaking Prevention Circuit with Compensation Capacitor

Bipolar Output Circuit

The DAC8806, as a 4-quadrant multiplying DAC, can be used to generate a bipolar output. The polarity of the full-scale output (I_{OUT}) is the inverse of the input reference voltage at V_{RFF} .

Using a dual op amp, such as the OPA2277, full 4-quadrant operation can be achieved with minimal components. Figure 42 demonstrates a $\pm 10 \, V_{OUT}$ circuit with a fixed $\pm 10 \, V$ reference.

$$V_{OUT} = \left(\frac{D}{8192} - 1\right) \times V_{REF} \tag{2}$$



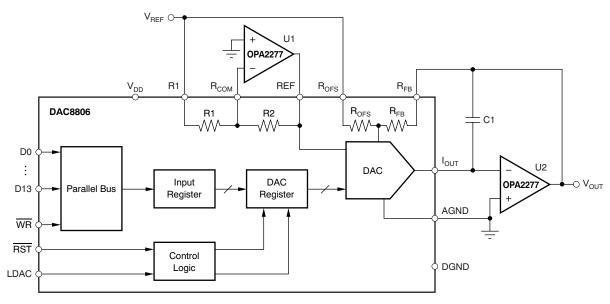


Figure 42. Bipolar Output Circuit

Programmable Current Source Circuit

A DAC8806 can be integrated into the circuit in Figure 43 to implement an improved Howland current pump for precise V/I conversions. Bidirectional current flow and high-voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by Equation 3:

$$I_{L} = \frac{(R2 + R3)/R1}{R3} \times V_{REF} \times D \tag{3}$$

The value of R3 in the previous equation can be reduced to increase the output current drive of U3. U3 can drive ± 20 mA in both directions with voltage compliance limited up to 15 V by the U3 voltage supply. Elimination of the circuit compensation capacitor (C1) in the circuit is not suggested as a result of the change in the output impedance (Z_0), according to Equation 4:

$$Z_{o} = \frac{R1'R3(R1 + R2)}{R1(R2' + R3') - R1'(R2 + R3)}$$
(4)

As shown in Equation 4, Z_O with matched resistors is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used, Z_O is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating C1 into the circuit, possible oscillation problems are eliminated. The value of C1 can be determined for critical applications; for most applications, however, a value of several pF is suggested.



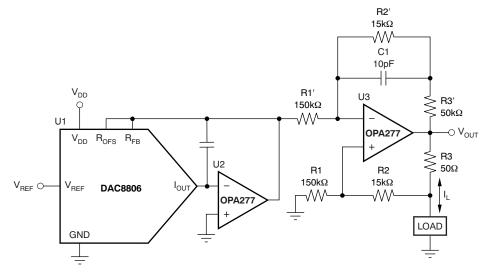


Figure 43. Programmable Bidirectional Current Source Circuit

Cross-Reference

The DAC8806 has an industry-standard pinout. Table 2 provides the cross-reference information.

Table 2. Cross-Reference

PRODUCT	BIT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS- REFERENCE PART
DAC8806IDB	14	±1	±1	-40°C to +85°C	SSOP-28	SSOP-28	LTC1591AIG



Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2006) to Revision B	Page
Changed front page block diagram	1
Fixed typo on 2nd Interface Timing subheader; changed from 5.0V to 2.7V	3
Changed pin 28 description text in Terminal Functions table	4
Changed first row description text in Table 1	
Changed Figure 42	
Changes from Original (April 2006) to Revision A	Page
Changed from "voltage-to-current" to "current-to-voltage"	1
Changed from (V/I) to (I/V)	14





com 12-Feb-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
DAC8806IDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8806IDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8806IDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8806IDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

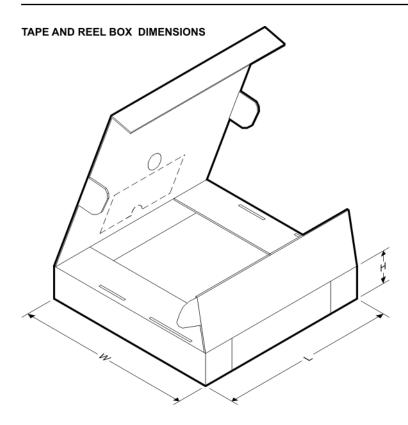
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8806IDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8806IDBR	SSOP	DB	28	2000	346.0	346.0	33.0

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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