FEATURES

- TI AM1808 ARM9 Application Processor
  - 456 MHz ARM926EJ-S MPU
  - 16 KB L1 Program Cache
  - 16 KB L1 Data Cache
  - 8 KB Internal RAM
  - 64 KB boot ROM
  - JTAG Emulation/Debug
- 128 MB mDDR2 CPU RAM
- 256 MB Parallel NAND FLASH
- 8 MB SPI based NOR FLASH
- Integrated Power Management
- Standard SO-DIMM-200 Interface
  - 10/100 EMAC MII / RMII / MDIO
  - 2 UARTS
  - 2 McBSPs, 2 SPI, 2HPI
  - 2 USB Ports
  - Video, LCD Output
  - Camera/Video Input
  - MMC/SD
  - SATA
  - ePWM, eCAP
  - EMIFA
  - Single 3.3V Power Supply

(actual size)

APPLICATIONS

- Industrial Automation
- Industrial Instrumentation
- Embedded Control Processing
- Embedded User Interfaces
- Test and Measurement
- Medical Devices

BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity and Interface Options
- Rich User Interfaces
- High System Integration
- High Level OS Support
  - Real-Time Linux Kernel 2.6
  - QNX 6.4
  - Windows XP Embedded

DESCRIPTION

The MityARM-1808 is a highly configurable, very small form-factor processor card that features a Texas Instruments AM1808 456 MHz ARM Applications Processor, FLASH (NAND, and NOR) and mDDR2 RAM memory subsystems. The MityARM-1808 provides a complete and flexible CPU infrastructure necessary for the most demanding embedded applications development.

The AM1808 includes an ARM926EJ-S micro-processor unit (MPU) capable of running the rich software applications programming interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Real-Time Linux, QNX and Windows XP embedded. Linux drivers are available for all interfaces.

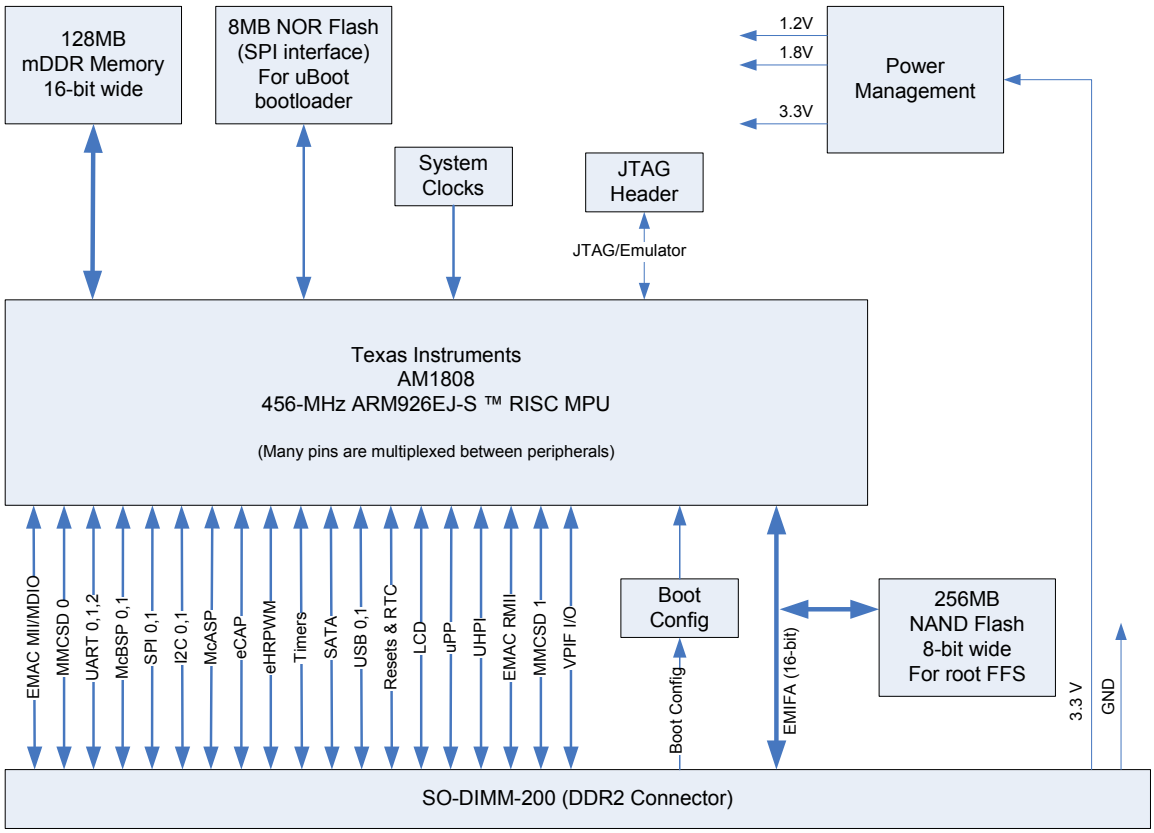

Figure 1 MityARM-1808 Block Diagram

Figure 1 provides a top level block diagram of the MityARM-1808 processor card. As shown in the figure, the primary interface to the MityARM-1808 is through a standard SO-DIMM-200 card edge interface. The interface provides power, synchronous serial connectivity, and a rich set of interfaces available for application defined interfacing. Details of the SO-DIMM-200 connector interface are included in the SO-DIMM-200 Interface Description, below.

AM1808 mDDR2 Memory Interface

The AM1808 includes a dedicated DDR2 SDRAM memory interface. The MityARM-1808 includes 128 MB of mDDR2 RAM integrated with the AM1808 processor. The bus interface is capable of burst transfer rates of 600 MB / second.

AM1808 SPI NOR FLASH Interface

The MityARM-1808 includes 8 MB of SPI NOR FLASH. This FLASH memory is intended to store a factory provided bootloader, and typically a compressed image of a linux kernel for the ARM core processor.

EMIFA / NAND FLASH Interface

The Asynchronous External Memory Interface (EMIFA) interface available on the AM1808 is available on the SO-DIMM-200 connector. The EMIFA interface includes 3

chip select spaces. The EMIF interface supports multiple data width transfers and bus wait state configurations based on chip select space. 8, and 16 bit data word sizes may be used.

256 MB of on-board NAND FLASH memory is connected to the AM1808 using the EMIFA bus. The FLASH memory is 8 bits wide and is connected to the third chip select line of the EMIFA (CE1). The FLASH memory is typically used to store the following types of data:

- ARM linux / windows XP / QNX embedded root file-system
- runtime ARM software
- runtime application data (non-volatile storage)

AM1808 Camera and Video Interfaces
The AM1808 includes an optional video port I/O interface commonly used to drive LCD screens as well as a camera input interface. These interfaces have been routed directly to the SO-DIMM-200 connector.

Debug Interface
The JTAG interface signals for the AM1808 processor have been brought out to a compact connector suitable for use on the module. Critical Link supplies an adapter cable to convert this compact connector to a standard interface suitable for JTAG emulation.

Software and Application Development Support
Users of the MityARM-1808 are encouraged to develop applications using the MityARM-1808 software development kit provided by Critical Link LLC. The development kit includes an implementation of an OpenEmbedded board support package providing an Angstrom based Linux distribution and compatible gcc compiler tool-chain with debugger.

Growth Options
The MityARM-1808 has been designed to support several upgrade options. These options include various speed grades, memory configurations, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a particular configuration not listed below, please contact a Critical Link sales representative.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage, Vcc	3.5 V
Storage Temperature Range	-65 to 80C
Shock, Z-Axis	±10 g
Shock, X/Y-Axis	±10 g

OPERATING CONDITIONS

Ambient Temperature Range	0°C to 70°C
Humidity	0 to 95% Non-condensing
Vibration, Z-Axis	TBS
Vibration, X/Y-Axis	TBS

SO-DIMM-200 Interface Description

The primary interface connector for the MityARM-1808 is the SO-DIMM card edge interface.

Table 1 SO-DIMM Pin-Out

Pin	I/O	Signal	Pin	I/O	Signal
1	-	+3.3 V in	2	-	+3.3 V in
3	-	+3.3 V in	4	-	+3.3 V in
5	-	+3.3 V in	6	-	+3.3 V in
7	-	GND	8	-	GND
9	-	GND	10	-	GND
11	I	RESET_IN#	12	I	EXT_BOOT#
13	O	SATA_TX_P	14	I/O	GP0_7
15	O	SATA_TX_N	16	I/O	GP0_10
17	I	SATA_RX_P	18	I/O	GP0_11
19	I	SATA_RX_N	20	I/O	GP0_15
21	I	USB0_ID	22	I/O	GP0_6
23	I/O	USB1_D_N	24	I/O	GP0_14
25	I/O	USB1_D_P	26	I/O	GP0_12
27	O	USB0_VBUS	28	I/O	GP0_5
29	I/O	USB0_D_N	30	I/O	GP0_13
31	I/O	USB0_D_P	32	I/O	GP0_1
33	O	USB0_DRVVBUS	34	I/O	GP0_4
35	-	3V RTC Battery	36	I/O	GP0_3
37	-	+3.3 V in	38	-	+3.3 V in
39	-	+3.3 V in	40	-	+3.3 V in
41	-	GND	42	-	GND
43	I/O	SPI1_MISO	44	I/O	GP0_2
45	I/O	SPI1_MOSI	46	I/O	GP0_0
47	I/O	SPI1_ENA	48	I/O	GP0_8
49	I/O	SPI1_CLK	50	I/O	GP0_9
51	I/O	SPI1_SCS[1]	52	I/O	MMCSD0_DAT[7]
53	-	Reserved	54	I/O	MMCSD0_DAT[6]

Pin	I/O	Signal	Pin	I/O	Signal
55	I/O	I2C0_SCL	56	I/O	MMCSD0_DAT[5]
57	I/O	I2C0_SDA	58	I/O	MMCSD0_DAT[4]
59	I/O	UART2_TXD / I2C1_SDA	60	I/O	MMCSD0_DAT[3]
61	I/O	UART2_RXD / I2C1_SCL	62	I/O	MMCSD0_DAT[2]
63	-	GND	64	-	GND
65	O	UART1_TXD	66	I/O	MMCSD0_DAT[1]
67	I	UART1_RXD	68	I/O	MMCSD0_DAT[0]
69	O	MDIO_CLK	70	I/O	MMCSD0_CMD
71	I/O	MDIO_D	72	O	MMCSD0_CLK
73	I	MII_RXCLK	74	I	MII_TXCLK
75	I	MII_RXDV	76	O	MII_TXD[3]
77	I	MII_RXD[0]	78	O	MII_TXD[2]
79	I	MII_RXD[1]	80	O	MII_TXD[1]
81	I	MII_RXD[2]	82	O	MII_TXD[0]
83	I	MII_RXD[3]	84	O	MII_TXEN
85	-	GND	86	-	GND
87	I	MII_CRS	88	I	MII_COL
89	I	MII_RXER	90	-	NC
91	O	EMA_CS[0]	92	I/O	UPP_CHA_START
93	O	EMA_OE	94	I	VP_CLKIN1
95	O	EMA_BA[0]	96	I/O	UPP_D[15] / RMII_TXD[1]
97	O	EMA_BA[1]	98	I/O	UPP_D[14] / RMII_TXD[0]
99	O	EMA_A[0]	100	I/O	UPP_D[13] / RMII_TXEN
101	O	EMA_A[1]	102	I/O	UPP_D[12] / RMII_RXD[1]
103	O	EMA_A[2]	104	I/O	UPP_D[11] / RMII_RXD[0]
105	O	EMA_A[3]	106	I/O	UPP_D[10] / RMII_RXER
107	-	GND	108	-	GND
109	O	EMA_A[4]	110	I/O	UPP_D[9] / RMII_REF_CLK
111	O	EMA_A[5]	112	I/O	UPP_D[8] / RMII_CRS_DV
113	O	EMA_A[6]	114	I/O	UPP_D[7]
115	O	EMA_A[7]	116	I/O	UPP_D[6]
117	O	EMA_A[8]	118	I/O	UPP_CHA_ENABLE
119	O	EMA_A[9]	120	I/O	UPP_D[5]
121	O	EMA_A[10]	122	I/O	UPP_D[4]
123	O	EMA_A[11]	124	I/O	UPP_D[3]
125	O	EMA_A[12]	126	I/O	UPP_D[2]
127	O	EMA_A[13]	128	I/O	UPP_CHA_WAIT
129	-	GND	130	-	GND
131	I/O	EMA_D[15]	132	I/O	UPP_D[1]
133	I/O	EMA_D[14]	134	I/O	UPP_D[0]
135	I/O	EMA_D[13]	136	I/O	UPP_CHA_CLK
137	I/O	EMA_D[12]	138	I/O	UPP_CHB_ENABLE
139	I/O	EMA_D[11]	140	O	VP_CLKOUT2
141	I/O	EMA_D[10]	142	I	VP_CLKIN2
143	I/O	EMA_D[9]	144	I/O	UPP_CHB_WAIT
145	I/O	EMA_D[8]	146	I/O	UPP_CHB_START
147	I/O	EMA_D[7]	148	I/O	UPP_CHB_CLK
149	I/O	EMA_D[6]	150	I	VP_CLKIN0
151	-	GND	152	-	GND
153	I/O	EMA_D[5]	154	I/O	LCD_D[15]

Pin	I/O	Signal	Pin	I/O	Signal
155	I/O	EMA_D[4]	156	I/O	LCD_D[14]
157	I/O	EMA_D[3]	158	I/O	LCD_D[13]
159	I/O	EMA_D[2]	160	I/O	LCD_D[12]
161	I/O	EMA_D[1]	162	I/O	LCD_D[11]
163	I/O	EMA_D[0]	164	I/O	LCD_D[10]
165	O	EMA_WEN_DQM[0]	166	I/O	LCD_D[9]
167	O	EMA_WEN_DQM[1]	168	I/O	LCD_D[8]
169	O	EMA_SDCKE	170	I/O	LCD_D[7]
171	O	EMA_CLK	172	I/O	LCD_D[6]
173	-	GND	174	-	GND
175	O	EMA_WE	176	O	LCD_VSYNC
177	O	EMA_CAS	178	O	LCD_HSYNC
179	O	EMA_RAS	180	I/O	LCD_D[5]
181	O	EMA_CS[2]	182	O	LCD_PCLK
183	O	EMA_CS[4]	184	I/O	LCD_D[4]
185	O	EMA_CS[5]	186	I/O	LCD_D[3]
187	OD	RESET_OUT	188	I/O	LCD_D[2]
189	I	VP_CLKIN3	190	I/O	LCD_D[1]
191	O	VP_CLKOUT3	192	I/O	LCD_D[0]
193	O	LCD_MCLK	194	O	LCD_AC_ENB_CS
195	-	GND	196	-	GND
197	O	EMA_A_RW	198	I	EMA_WAIT[0]
199	O	EMA_CS[3]	200	I	EMA_WAIT[1]

AM1808 JTAG Interface Description (J2)

Table 2 AM1808 JTAG Connector Pad

Pin	I/O	Signal	Pin	I/O	Signal
1	I	TMS	2	I	TRST
3	I	TDI	4	-	GND
5	-	3.3V	6	-	KEY
7	O	TDO	8	-	GND
9	O	RTCK	10	-	GND
11	I	TCK	12	-	GND
13	O	EMU0	14	O	EMU1

ELECTRICAL CHARACTERISTICS

Table 3: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V33	Voltage supply, 3.3 volt input.		3.2	3.3	3.4	Volts
I33	Quiescent Current draw, 3.3 volt input			TBS	TBS	mA
I33-max	Max current draw, positive 3.3 volt input.			TBS	TBS	mA
FCPU	CPU internal clock Frequency (PLL output)		25	456	456	MHz
FEMIF	EMIF bus frequency		-	100	-	MHz
	1. Power utilization of the MityARM-1808 is heavily dependant on end-user application. Major factors include: ARM CPU PLL configuration, and external DDR2 RAM utilization.					

ORDERING INFORMATION

The following table lists the orderable module configurations. For shipping status, availability, and lead time of these or other configurations please contact your Critical Link representative.

Table 4: Orderable Model Numbers

Model	ARM Speed	NOR Flash	NAND Flash	RAM	Operating Temp
1808-FX-225-RC	456 MHz	8MB	256MB	128MB	0°C to 70° C
1808-DX-225-RI	375 MHz	8MB	256MB	128MB	-40°C to 85° C

MECHANICAL INTERFACE

A mechanical outline of the MityARM-1808 is illustrated in Figure 2, below.

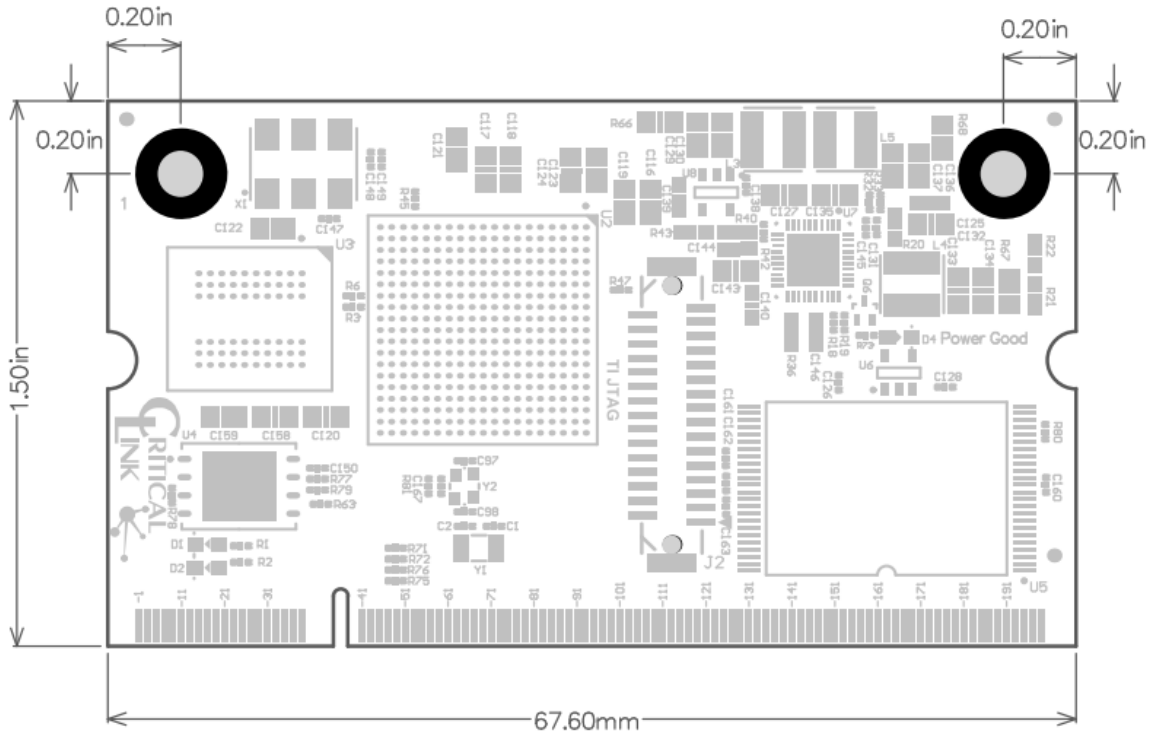

Figure 2 MityARM-1808 Mechanical Outline

REVISION HISTORY

Date	Change Description
7-JAN-2011	Initial Release
11-FEB-2011	Update DDR Speed to support 150 MHz clocking.
12-JUL-2011	Update NAND to indicate 8 bit data width. Update block diagram accordingly.