



## **DAC813**

# Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

## **FEATURES**

- ±1/2LSB NONLINEARITY OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- LOW POWER: 270mW typ
- DIGITAL INTERFACE DOUBLE BUFFERED: 12 AND 8 + 4 BITS
- SPECIFIED AT ±12V AND ±15V POWER SUPPLIES
- RESET FUNCTION TO BIPOLAR ZERO
- 0.3" WIDE DIP AND SO PACKAGES

### DESCRIPTION

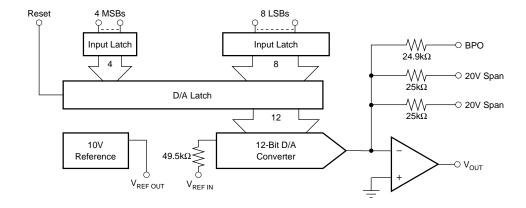
The DAC813 is a complete monolithic 12-bit digital-to-analog converter with a flexible digital interface. It includes a precision +10V reference, interface control logic, double-buffered latch and a 12-bit D/A

converter with voltage output operational amplifier. Fast current switches and laser-trimmed thin-film resistors provide a highly accurate, fast D/A converter.

Digital interfacing is facilitated by a double buffered latch. The input latch consists of one 8-bit byte and one 4-bit nibble to allow interfacing to 8-bit (right justified format) or 16-bit data buses. Input gating logic is designed so that the last nibble or byte to be loaded can be loaded simultaneously with the transfer of data to the D/A latch saving computer instructions.

A reset control allows the DAC813 D/A latch to asynchronously reset the D/A output to bipolar zero, a feature useful for power-up reset, recalibration, or for system re-initialization upon system failure.

The DAC813 is specified to  $\pm 1/2$ LSB maximum linearity error (J, A grades) and  $\pm 1/4$ LSB (K grade). It is packaged in 28-pin 0.3" wide plastic DIP and 28-lead plastic SOIC



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111 Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## **SPECIFICATIONS**

At  $T_A$  = +25°C,  $\pm V_{CC}$  =  $\pm 12V$  or  $\pm 15V$  and load on  $V_{OUT}$  =  $5k\Omega$  || 500pF to common, unless otherwise noted.

		DAC813JP, JU, AU			D/			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DIGITAL INPUTS  Resolution Codes(1) Digital Inputs Over Temperature Range(2)			USB, BOB	12		*	*	Bits
$\begin{array}{c} \text{Signature} \\ \text{V}_{\text{IH}}^{(3)} \\ \text{V}_{\text{IL}} \\ \text{DATA Bits, } \overline{\text{WR, }} \overline{\text{Reset, }} \overline{\text{LDAC, }} \overline{\text{LMSB, }} \overline{\text{LLSB}} \\ \text{I}_{\text{IH}} \\ \text{I}_{\text{IL}} \end{array}$	$V_{IN} = +2.7V$ $V_{IN} = +0.4V$	+2 0		+5.5 +0.8 ±10 ±10	*		* * * *	VDC VDC μA μA
ACCURACY Linearity Error Differential Linearity Error Gain Error <sup>(4)</sup> Unipolar Offset Error <sup>(5)</sup> Bipolar Zero Error <sup>(6)</sup> Monotonicity Power Supply Sensitivity: +V <sub>CC</sub> -V <sub>CC</sub>	20V Range		±1/4 ±1/2 ±0.05 ±0.01 ±0.02 Guaranteed 5 1	±1/2 ±3/4 ±0.2 ±0.02 ±0.2		±1/8 ±1/4 * * * *	±1/4 ±1/2 * * *	LSB LSB % % of FSR <sup>(7)</sup> % of FSR ppm of FSR/% ppm of FSR/%
DRIFT Gain Unipolar Offset Bipolar Zero Linearity Error Over Temperature Range Monotonicity Over Temperature Range	Over Specification Temperature Range		±5 ±1 ±3 ±1/2 Guaranteed	±30 ±3 ±10 ±3/4		* * * ±1/4 *	±15 ±3 ±5 ±1/2	ppm/°C ppm of FSR/°C ppm of FSR/°C LSB
SETTLING TIME(8) (To Within $\pm 0.01\%$ of FSR of Final Value; $5k\Omega \parallel 500pF$ load) For Full Scale Range Change For 1LSB Change at Major Carry(9) Slew Rate	20V Range 10V Range		4.5 3.3 2 10	6 5		* * *	*	μs μs μs V/μs
ANALOG OUTPUT  Voltage Range: Unipolar Bipolar  Output Current Output Impedance Short Circuit to Common Duration	$\pm V_{CC} > \pm 11.4V$ $\pm V_{CC} > \pm 11.4V$ At DC	±5	0 to +10 ±5, ±10 0.2 Indefinite		*	* * * *		V V mA Ω
REFERENCE VOLTAGE Voltage Source Current Available for External Loads Impedance Temperature Coefficient Short Circuit to Common Duration		+9.95 5	+10 2 ±5 Indefinite	+10.05 ±25	*	* * *	*	V mA Ω ppm/°C
$ \begin{array}{lll} \textbf{POWER SUPPLY REQUIREMENTS} \\ \textbf{Voltage:} & + \textbf{V}_{CC} \\ & - \textbf{V}_{CC} \\ \textbf{Current:} & + \textbf{V}_{CC} + \textbf{V}_{L} \\ & - \textbf{V}_{CC} \\ \textbf{Potential at DCOM with Respect to ACOM}^{(10)} \\ \textbf{Power Dissipation} \\ \end{array} $	No Load No Load	+11.4 -11.4 -3	+15 -15 13 -5	+16.5 -16.5 15 -7 +3 330	* *	* * * *	* * * * *	VDC VDC mA mA V mW
TEMPERATURE RANGE Specification: J, K A Operating: J, K A Storage: J, K A		0 -40 -40 -55 -60 -65		+70 +85 +85 +125 +100 +150	* * * * *		* * * * *	ဝံ ဝံ ဝံ ဝံ ဝံ

 $<sup>\</sup>ensuremath{\boldsymbol{\ast}}$  Same as specification for DAC813AU, JP, JU.

NOTES: (1) USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary. (2) TTL and 5V CMOS compatible. (3) Open DATA input lines will be pulled above  $\pm 5.5$ V. See discussion under LOGIC INPUT COMPATIBILITY in the OPERATION section. (4) Specified with  $500\Omega$  Pin 6 to 7. Adjustable to zero with external trim potentiometer. (5) Error at input code  $000_{HEX}$  for unipolar mode, FSR = 10V. (6) Error at input code  $800_{HEX}$  for bipolar range. Specified with  $100\Omega$  Pin 6 to 4 and with  $500\Omega$  pin 6 to 7. See page 9 for zero adjustment procedure. (7) FSR means Full Scale Range and is 20V for the  $\pm 10$ V range. (8) Maximum represents the  $3\sigma$  limit. Not 100% tested for this parameter. (9) At the major carry,  $7FF_{HEX}$  to  $800_{HEX}$  and  $800_{HEX}$  to  $7FF_{HEX}$ . (10) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.



#### PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1		
2, 3	+V <sub>L</sub> 20V Range	Positive supply pin for logic circuits. Connect to +V <sub>CC</sub> .  Connect Pin 2 or Pin 3 to Pin 9 (V <sub>OUT</sub> ) for a 20V  FSR. Connect both to Pin 9 for a 10V FSR.
4	ВРО	Bipolar offset. Connect to Pin 6 ( $V_{REFOUT}$ ) through $100\Omega$ resistor or $200\Omega$ potentiometer for bipolar operation.
5	ACOM	Analog common, ±V <sub>CC</sub> supply return.
6	V <sub>REF OUT</sub>	+10V reference output referred to ACOM.
7	V <sub>REF IN</sub>	Connected to $V_{\text{REF OUT}}$ through a $1\text{k}\Omega$ gain adjustment potentiometer or a $500\Omega$ resistor.
8	+V <sub>CC</sub>	Analog supply input, nominally +12V to +15V referred to ACOM.
9	V <sub>OUT</sub>	D/A converter voltage output.
10	-V <sub>CC</sub>	Analog supply input, nominally –12V or –15V referred to ACOM.
11	WR	Master enable for LDAC, LLSB, and LMSB. Must be low for data transfer to any latch.
12	LDAC	Load DAC. Must be low with $\overline{\text{WR}}$ for data transfer to the D/A latch and simultaneous update of the D/A converter.
13	Reset	When low, resets the D/A latch such that a Bipolar Zero output is produced. This control overrides all other data input operations.
14	LMSB	Enable for 4-bit input latch of D <sub>8</sub> -D <sub>11</sub> data inputs.  NOTE: This logic path is slower than the WR path.
15	LLSB	Enable for 8-bit input latch of $D_0$ - $D_7$ data inputs. NOTE: This logic path is slower than the $\overline{\rm WR}$ path.
16	DCOM	Digital common.
17	D0	Data Bit 1, LSB.
18	D1	Data Bit 2.
19	D2	Data Bit 3.
20	D3	Data Bit 4.
21	D4	Data Bit 5.
22	D5	Data Bit 6.
23	D6	Data Bit 7.
24	D7	Data Bit 8.
25	D8	Data Bit 9.
26	D9	Data Bit 10.
27	D10	Data Bit 11.
28	D11	Data Bit 12, MSB, positive true.

#### ABSOLUTE MAXIMUM RATINGS(1)

+V <sub>CC</sub> to ACOM 0 to +18V
-V <sub>CC</sub> to ACOM 0 to -18V
+V <sub>CC</sub> to -V <sub>CC</sub> 0 to +36V
DCOM with respect to ACOM ±4V
Digital Inputs (Pins 11–15, 17–28) to DCOM0.5V to +V <sub>CC</sub>
External Voltage Applied to BPO Span Resistor ±V <sub>CC</sub>
V <sub>REF OUT</sub> Indefinite Short to ACOM
V <sub>OUT</sub>
Power Dissipation
Lead Temperature (soldering, 10s)+300°C
Max Junction Temperature+165°C
Thermal Resistance, $\theta_{J-A}$ :Plastic DIP and SOIC
Ceramic DIP85°C/W

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

#### PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>	TEMPERATURE RANGE	LINEARITY ERROR, MAX AT +25°C (LSB)	GAIN DRIFT (ppm/°C)
DAC813JP	28-Pin Plastic DIP	246	0°C to +70°C	±1/2	±30
DAC813JU	28-Lead Plastic SOIC	217	0°C to +70°C	±1/2	±30
DAC813KP	28-Pin Plastic DIP	246	0°C to +70°C	±1/4	±15
DAC813KU	28-Lead Plastic SOIC	217	0°C to +70°C	±1/4	±15
DAC813AU	28-Lead Plastic SOIC	217	-40°C to +85°C	±1/2	±30

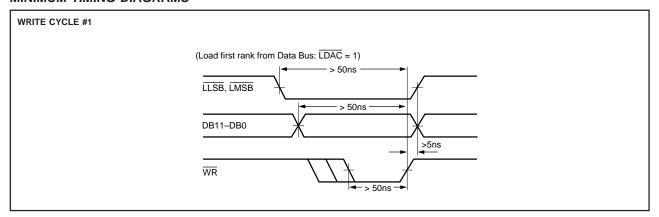
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

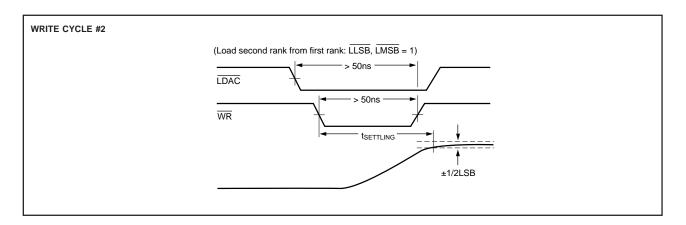
The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

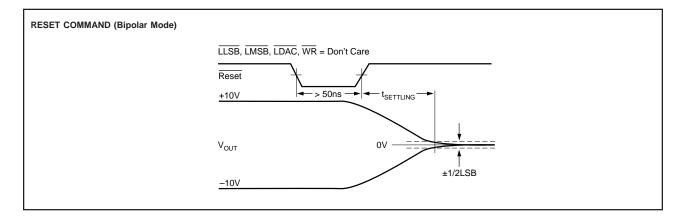
3



#### **MINIMUM TIMING DIAGRAMS**

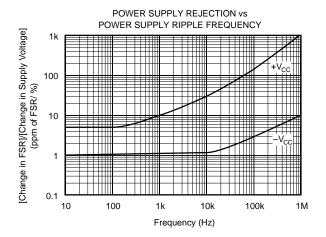


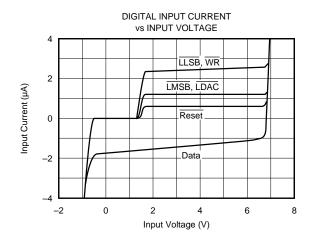


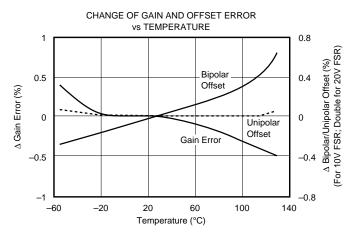


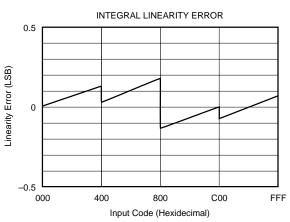
## **TYPICAL PERFORMANCE CURVES**

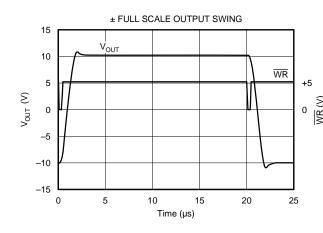
At  $T_A$  = +25°C,  $V_{CC}$  = ±15V, unless otherwise noted.

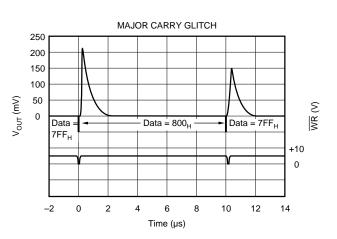






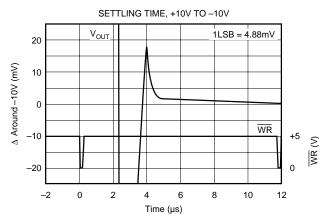


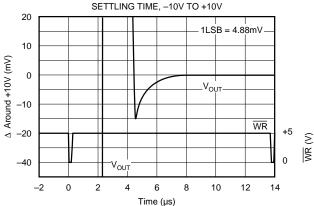




## TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A$  = +25°C,  $V_{CC}$  = ±15V, unless otherwise noted.





## DISCUSSION OF SPECIFICATIONS

#### **INPUT CODES**

The DAC813 accepts positive-true binary input codes. DAC813 may be connected by the user for any one of the following codes: USB (Unipolar Straight Binary), BOB (Bipolar Offset Binary) or, using an external inverter on the MSB line, BTC (Binary Two's Complement). See Table I.

DIGITAL	ANALOG OUTPUT							
INPUT  MSB to LSB	USB	BOB	BTC*					
	Unipolar	Bipolar	Binary					
	Straight	Offset	Two's					
	Binary	Binary	Complement					
FFF <sub>HEX</sub>	+ Full Scale	+ Full Scale	Zero – 1LSB					
800 <sub>HEX</sub>	+ 1/2 Full Scale	Zero	– Full Scale					
7FF <sub>HEX</sub>	+ 1/2 Full Scale – 1LSB	Zero – 1LSB	+ Full Scale					
000 <sub>HEX</sub>	Zero	– Full Scale	Zero					
* Invert MSB of BOB code with external inverter to obtain BTC code.								

TABLE I. Digital Input Codes.

#### LINEARITY ERROR

Linearity error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all "1s" and all "0s"). The DAC813 linearity error is specified at  $\pm 1/4$ LSB (max) at +25°C K grades, and  $\pm 1/2$ LSB (max) for J grades.

#### DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the input changes from one state to the next. Monotonicity requires that DLE be less than 1LSB over the temperature range of interest.

#### MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. All grades of DAC813 are monotonic over their specification temperature range.

#### **DRIFT**

Gain Drift is a measure of the change in the Full Scale Range (FSR) output over the specification temperature range. Gain Drift is expressed in parts per million per degree Celsius (ppm/°C).

Unipolar Offset Drift is measured with a data input of  $000_{\rm HEX}$ . The D/A is configured for unipolar output. Unipolar Offset Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

Bipolar Zero Drift is measured with a data input of 800<sub>HEX</sub>. The D/A is configured for bipolar output. Bipolar Zero Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

#### **SETTLING TIME**

Settling Time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to  $\pm 0.012\%$  of Full Scale Range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry (7FF $_{\rm HEX}$  to  $800_{\rm HEX}$  and  $800_{\rm HEX}$  to  $7FF_{\rm HEX}$ ), the input transition at which worst-case settling time occurs.

#### REFERENCE SUPPLY

DAC813 contains an on-chip +10V reference. This voltage (pin 6) has a tolerance of  $\pm 50 \text{mV}$ .  $V_{REF\ OUT}$  must be connected to  $V_{REF\ IN}$  through a gain adjust resistor with a nominal value of  $500\Omega$ . The connection can be made through an optional  $1k\Omega$  trim resistor to provide adjustment to zero



gain error. The reference output may be used to drive external loads, sourcing at least 5mA. This current should be constant, otherwise the gain of the converter will vary.

#### POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a ppm of FSR output change per percent of change in either  $+V_{CC}$  or  $-V_{CC}$  about the nominal voltages expressed in ppm of FSR/%. The first performance curve on page 5 shows typical power supply rejection versus power supply ripple frequency.

## **OPERATION**

DAC813 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 1.

#### **INTERFACE LOGIC**

Input latches hold data temporarily while a complete 12-bit word is assembled before loading into the D/A latch. This double-buffered organization prevents the generation of spurious analog output values. Each latch is independently addressable.

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for the control signals is presented in Table II.

WR	LLSB	LMSB	LDAC	RESET	OPERATION			
1	Х	Х	Х	1	No operation			
X	X	Х	X	0	D/A latch set to 800 <sub>HEX</sub>			
0	1	0	1	1	Enables 4 MSBs input latch			
0	0	1	1	1	Enables 8 LSBs input latch			
0	1	1	0	1	Loads D/A latch from input latches			
0	0	0	0	1	Makes all latches transparent			
"X" =	"X" = Don't Care							

TABLE II. DAC813 Interface Logic Truth Table.

**CAUTION:** DAC813 was designed to use  $\overline{WR}$  as the fast strobe.  $\overline{WR}$  has a much faster logic path than  $\overline{EN}_X$  (or  $\overline{LDAC}$ ). Therefore, if one permanently wires  $\overline{WR}$  to DCOM and uses only  $\overline{EN}_X$  to strobe data into the latches, the DATA HOLD time will be long, approximately 15ns to 30ns, and this time will vary considerably in this range from unit to unit. DATA HOLD time using  $\overline{WR}$  is 5ns max.

#### LOGIC INPUT COMPATIBILITY

The DAC813 digital inputs are TTL, 5V CMOS compatible over the operating range of  $+V_{CC}$ . The input switching threshold remains at the TTL threshold over the supply range. An equivalent circuit of a digital input is shown in Figure 2.

The logic input current over temperature is low enough to permit driving the DAC813 directly from the outputs of 5V CMOS devices.

Open DATA input lines will float to 7V or more. Although this will not harm the DAC813, current spikes will occur in the input lines when a logic 0 is asserted and, in addition,

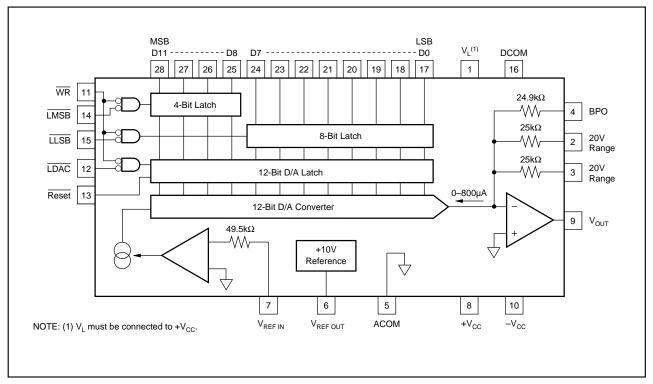


FIGURE 1. DAC813 Block Diagram.



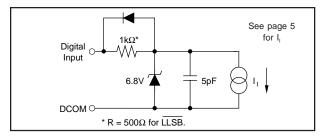


FIGURE 2. Equivalent Input Circuit for Digital Inputs.

the speed of the interface will be slower. A digital output driving a DATA input line of the DAC813 must not drive, **or let the DATA input float**, above +5.5V. Unused DATA inputs should be connected to DCOM.

#### **RESET FUNCTION**

When asserted low (<0.8V),  $\overline{\text{RESET}}$  (Pin 13) forces the D/A latch to  $800_{\text{HEX}}$  regardless of any other input logic condition. If the analog output is connected for bipolar operation (either  $\pm 10V$  or  $\pm 5V$ ), the output will be reset to Bipolar Zero (0V). If the analog output is connected for unipolar operation (0 to +10V), the output will be reset to half-scale (+5V).

If  $\overline{\text{RESET}}$  is not used, it should be connected to a voltage greater than +2V but not greater than +5.5V. If this voltage is not available  $\overline{\text{Reset}}$  can be connected to +V<sub>CC</sub> through a  $100 \text{k}\Omega$  to  $1\text{M}\Omega$  resistor to limit the input current.

#### **GAIN AND OFFSET ADJUSTMENTS**

Figures 3 and 4 illustrate the relationship of offset and gain adjustments to unipolar and bipolar D/A converter output.

#### **OFFSET ADJUSTMENT**

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the offset potentiometer for zero output. For bipolar (BOB,

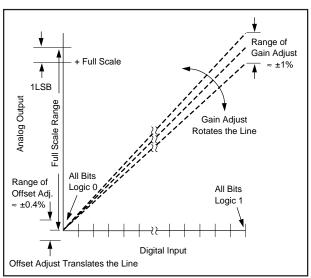


FIGURE 3. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. Example: If the full scale range is connected for 20V, the maximum negative output voltage is –10V. See Table III for corresponding codes.

#### **GAIN ADJUSTMENT**

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table III for positive full scale voltages.

DIGITAL INPUT	ANALOG OUTPUT							
MSB to LSB	0 to +10V	±5V	±10V					
FFF <sub>HEX</sub>	+9.9976V	+4.9976V	+9.9951V					
800 <sub>HEX</sub>	+5.0000V	0.0000V	0.0000V					
7FF <sub>HEX</sub>	+4.9976V	-0.0024V	-0.0049V					
000 <sub>HEX</sub>	0.0000V	-5.0000V	-10.0000V					
1LSB	2.44mV	2.44mV	4.88mV					

TABLE III. Digital Input/Analog Output.

### INSTALLATION

#### POWER SUPPLY CONNECTIONS

Note that the lid of the ceramic packaged DAC813 is connected to  $-V_{CC}$ . Take care to avoid accidental short circuits in tightly spaced installations.

Power supply decoupling capacitors should be added as shown in Figure 5. Optimum settling performance occurs using a 1 to  $10\mu F$  tantalum capacitor at  $-V_{CC}$  and at least a  $0.01\mu F$  ceramic capacitor at  $+V_{CC}$ . Applications with less critical settling time may be able to use  $0.01\mu F$  at  $-V_{CC}$  as well. The  $0.01\mu F$  capacitors should be located close to the DAC813.

Pin 1 supplies internal logic and must be connected to  $+V_{CC}$ .

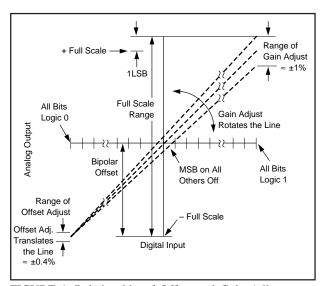


FIGURE 4. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.



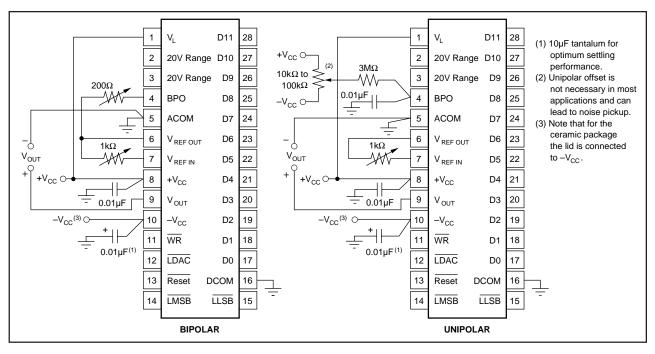


FIGURE 5. Power Supply, Gain, and Offset Connections.

DAC813 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both Analog Common (ACOM, Pin 5) and Digital Common (DCOM, Pin 16) be connected directly to a ground plane under the package. If a ground plane is not used, connect the ACOM and DCOM pins together close to the package. Since the reference point for  $V_{\text{OUT}}$  and  $V_{\text{REF OUT}}$  is the ACOM pin, it is also important to connect the load directly to the ACOM pin. Refer to Figure 5.

The change in current in the Analog Common pin (ACOM, Pin 5) due to an input data word change from  $000_{HEX}$  to  $FFF_{HEX}$  is only 800 $\mu$ A.

#### **OUTPUT RANGE CONNECTIONS**

Internal scaling resistors provided in the DAC813 may be connected to produce bipolar output voltage ranges of  $\pm 10$ V and ±5V or unipolar output voltage range of 0 to +10V. Refer to Figure 6.

The internal feedback resistors (25k $\Omega$ ) and the bipolar offset resistor (24.9k $\Omega$ ) are trimmed to an absolute tolerance of less than ±2%. Therefore, one can change the range by adding a series resistor in various feedback circuit configurations. For example, a  $600\Omega$  resistor in series with the 20V range terminal can be used to obtain a 20.48V (±10.24V) range (5mV LSB). A  $7.98k\Omega$  resistor in series with the 10V range connection (20V ranges in parallel) gives a 16.384V (±8.192V) bipolar range (4mV LSB). Gain drift will be affected by the mismatch of the temperature coefficient of the external resistor with the internal D/A resistors.

## **APPLICATIONS**

#### MICROCOMPUTER BUS INTERFACING

The DAC813 interface logic allows easy interface to microcomputer bus structures. The control signal is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines  $\overline{LMSB}$ ,  $\overline{LLSB}$ , and  $\overline{LDAC}$  determine which of the latches are selected. It is permissible to enable two or more latches simultaneously, as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC813s and later strobed into the D/A latch of all D/As, simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are used, the base address decoder can be simplified or eliminated altogether.

#### 8-BIT INTERFACE

The control logic of DAC813 permits interfacing to rightjustified data formats, illustrated in Figure 7. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figure 8 illustrates an addressing scheme for right-justified data. The base address is decoded from the high-order address bits. A0 and A1 address the appropriate latches. Note that adjacent addresses are used. X10<sub>HEX</sub> loads the 8 LSBs and X01<sub>HEX</sub> loads the 4 MSBs and simultaneously transfers input latch data to the D/A latch. Addresses  $X00_{HEX}$  and  $X11_{HEX}$  are not used.



9

**DAC813** 

## INTERFACING MULTIPLE DAC813s IN 8-BIT SYSTEMS

Many applications, such as automatic test systems, require that the outputs of several D/A converters be updated simultaneously. The interface shown in Figure 9 uses a 74LSB138 decoder to decode a set of eight adjacent addresses to load the input latches of four DAC813s. The example uses a right-justified data format.

A ninth address using A3 causes all DAC813s to be updated simultaneously. If a certain DAC813 is always loaded last (for instance, D/A #4), A3 is not needed, saving 8 address

 $24.9k\Omega$ NC ₩ BPO  $25k\Omega$ ₩ 20V 0 TO +10V  $25k\Omega$ RANGE ₩ J <sub>20</sub>∨ 9 0 to +10V  $I_{DAC}$  $V_{OUT}$ ACOM 🕂  $V_{REF\,OUT}$ 24 9kO ₩ ВРО  $200\Omega$  pot or 25kΩ  $100\Omega$  fixed 2 20V ₩ ±10V 25kΩ RANGE NC ₩ 3 20V 9 O +10V  $I_{DAC}$ 5 ACOM  $V_{\mathsf{REF}\,\mathsf{OUT}}$ 24.9kΩ ₩  $200\Omega$  pot or BPO 25kΩ  $100\Omega$  fixed 2 20V ₩ ±5V 25kΩ RANGE ₩ 20V ○ ±5V IDAC 5 ACOM

FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

spaces for other uses. Incorporate A3 into the base address decoder, remove the inverter, connect the common  $\overline{LDAC}$  line to  $\overline{LLSB}$  of D/A #4, and connect D1 of the 74LS138 to +5V.

#### 12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application the input latch enable lines,  $\overline{LMSB}$  and  $\overline{LLSB}$ , are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC813, is selected by the address decoder and strobed by  $\overline{WR}$ .

Be sure and read the CAUTION statement in the LOGIC INPUT COMPATIBILITY section.



FIGURE 7. 12-Bit Data Format for 8-Bit Systems.

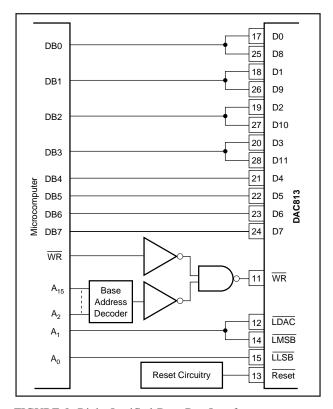


FIGURE 8. Right-Justified Data Bus Interface.



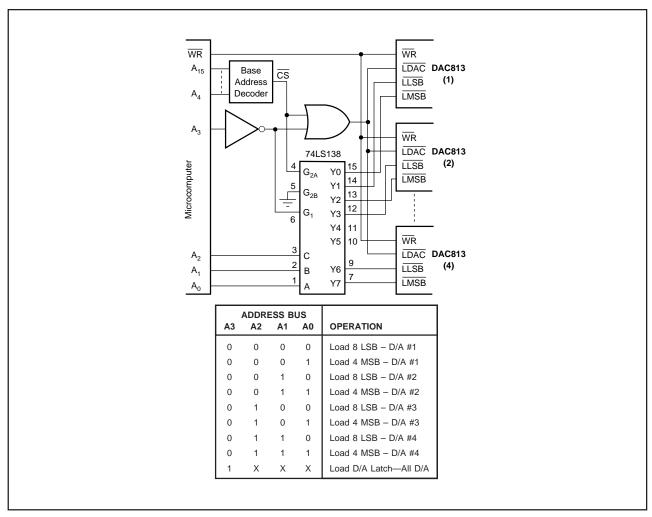


FIGURE 9. Interfacing Multiple DAC813s to an 8-Bit Bus.



28-Aug-2010

## **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
DAC813AU	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Contact TI Distributor or Sales Office
DAC813AU/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
DAC813AU/1KG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
DAC813AUG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Contact TI Distributor or Sales Office
DAC813JP	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Replaced by DAC813JU
DAC813JPG4	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Samples Not Available
DAC813JU	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Contact TI Distributor or Sales Office
DAC813JU/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
DAC813JU/1KG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
DAC813JUG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Contact TI Distributor or Sales Office
DAC813KP	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Replaced by DAC813KU
DAC813KPG4	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Samples Not Available
DAC813KU	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Contact TI Distributor or Sales Office
DAC813KUG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



## PACKAGE OPTION ADDENDUM

28-Aug-2010

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## PACKAGE MATERIALS INFORMATION

www.ti.com 18-Mar-2011

## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC813AU/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
DAC813JU/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

www.ti.com 18-Mar-2011



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC813AU/1K	SOIC	DW	28	1000	346.0	346.0	49.0
DAC813JU/1K	SOIC	DW	28	1000	346.0	346.0	49.0

#### IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		

**TI E2E Community Home Page** 

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated

e2e.ti.com