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155 Mbps to 4.25 Gbps Limiting Amplifier With LOS and RSSI

FEATURES

- Multi-Rate Operation from 155 Mbps up to 4.25 Gbps
- 89 mW Power Consumption
- Input Offset Cancellation
- High Input Dynamic Range
- Output Disable
- CML Data Outputs
- Receive Signal Strength Indicator (RSSI)
- Loss of Signal Detection
- Polarity Select
- Single 3.3-V Supply
- Surface Mount Small Footprint 3-mm × 3-mm 16-Pin QFN Package
- Pin-Compatible with the ONET2501PA and ONET3301PA

APPLICATIONS

- Multi-Rate OC3 to OC-48 FEC SONET/SDH Transmission Systems
- 1.0625 Gbps, 2.125 Gbps, and 4.25 Gbps Fibre Channel Receivers
- Gigabit Ethernet Receivers

DESCRIPTION

The ONET4201PA is a versatile high-speed, 3.3-V limiting amplifier for multiple fiber optic applications with data rates up to 4.25 Gbps.

This device provides a gain of about 50 dB, which ensures a fully differential output swing for input signals as low as $3 \text{ mV}_{\text{p-p}}$.

The high input signal dynamic range ensures low jitter output signals even when overdriven with input signal swings as high as 1200 mV_{p-p}.

The ONET4201PA provides a loss of signal detection as well as a received signal strength indicator.

The part is available in a small footprint 3-mm \times 3-mm 16-pin QFN package and is pin-compatible with the ONET2501PA and ONET3301PA.

This power efficient limiting amplifier typically dissipates less than 89 mW and it is characterized for operation from -40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



BLOCK DIAGRAM

A simplified block diagram of the ONET4201PA is shown in Figure 1.

This compact, low power 4.25 Gbps limiting amplifier consists of a high-speed data path with offset cancellation block, a loss of signal and RSSI detection block, and a bandgap voltage reference and bias current generation block.

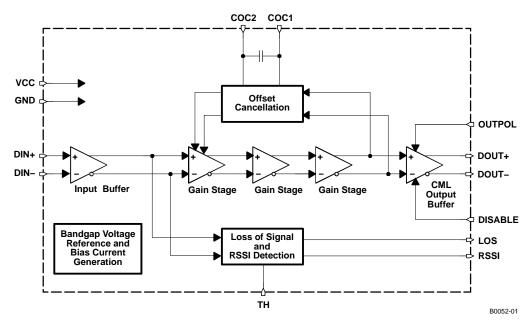


Figure 1. Simplified Block Diagram of the ONET4201PA

HIGH SPEED DATA PATH

The high-speed data signal is applied to the data path by means of the input signal pins DIN+/DIN–. The data path consists of the input stage with 2×50 - Ω on-chip line termination to VCC, three gain stages, which provide the required typical gain of about 50 dB, and a CML output stage. The amplified data output signal is available at the output pins DOUT+/DOUT-, which provide 2×50 - Ω back-termination to VCC. The output stage also includes a data polarity switching function, which is controlled by the OUTPOL input, and a disable function, controlled by the signal applied to the DISABLE input pin.

Offset cancellation compensates for internal offset voltages and thus ensures proper operation even for very small input data signals.

The low frequency cutoff is typically as low as 25 kHz with the built-in filter capacitor.

For applications which require even lower cutoff frequencies, an additional external filter capacitor may be connected to the COC1/COC2 pins.

LOSS OF SIGNAL AND RSSI DETECTION

The output signal of the input buffer is monitored by the loss of signal and RSSI detection circuitry. In this block a signal is generated that is linearly proportional to the input amplitude over a wide input voltage range. This signal is available at the RSSI output pin.

Furthermore, this circuit block compares the input signal to a threshold which can be programmed by means of an external resistor connected to the TH pin. If the input signal falls below the specified threshold, a loss of signal is indicated at the LOS pin.

The relation between the LOS assert voltage V_{AST} (in mV_{p-p}) and the external resistor R_{TH} (in $k\Omega$) connected to the TH pin can be approximated as given below:



$$R_{TH} \approx \frac{20.8 \text{ k}\Omega}{\left(V_{AST}/mV_{p-p} - 1\right)} + 300 \Omega$$

$$V_{AST} \approx \frac{20.8 \text{ mV}_{p-p}}{R_{TH}/k\Omega - 0.3} + 1 \text{ mV}_{p-p}$$
(2)

BANDGAP VOLTAGE AND BIAS GENERATION

The ONET4201PA limiting amplifier is supplied by a single 3.3-V±10% supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

An on-chip bandgap voltage circuit generates a supply voltage independent reference from which all other internally required voltages and bias currents are derived.

PACKAGE

For the ONET4201PA a small footprint 3-mm \times 3-mm 16-pin QFN package, with a lead pitch of 0,5 mm, is used. The pin out is shown in Figure 2.

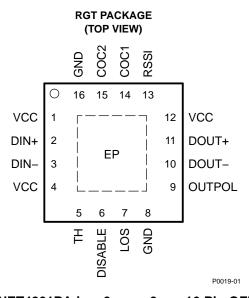


Figure 2. Pinout of ONET4201PA in a 3mm x 3mm 16 Pin QFN Package (Top View)

TERMINAL FUNCTIONS

TERI	TERMINAL		DECODIDATION
NO.	NAME	TYPE	DESCRIPTION
1, 4, 12	VCC	supply	3.3-V ± 10% supply voltage
2	DIN+	analog-in	Non-inverted data input. On-chip $50-\Omega$ terminated to VCC.
3	DIN-	analog-in	Inverted data input. On-chip 50- Ω terminated to VCC.
5	TH	analog-in	LOS threshold adjustment with resistor to GND.
6	DISABLE	CMOS-in	Disables CML output stage when set to high level.
7	LOS	CMOS-out	High level indicates that the input signal amplitude is below the programmed threshold level.
8, 16, EP	GND	supply	Circuit ground. Exposed die pad (EP) must be grounded.
9	OUTPOL	CMOS-in	Output data signal polarity select (internally pulled high). Setting to a high level or leaving the pin open selects normal polarity. Low level selects inverted polarity.
10	DOUT-	CML-out	Inverted data output. On-chip 50- Ω back-terminated toVCC.
11	DOUT+	CML-out	Non-inverted data output. On-chip $50-\Omega$ back-terminated to VCC.



TERMINAL FUNCTIONS (continued)

	TERMINAL	TYPE	DESCRIPTION
NO.	NAME	ITPE	DESCRIPTION
13	RSSI	analog-out	Analog output voltage proportional to the input data amplitude. Indicates the strength of the received signal (RSSI).
14	COC1	analog	Offset cancellation filter capacitor terminal 1. Connect an additional filter capacitor between this pin and COC2 (pin 15). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).
15	COC2	analog	Offset cancellation filter capacitor terminal 2. Connect an additional filter capacitor between this pin and COC1 (pin 14). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE/UNIT
V _{CC}	Supply voltage (2)	-0.3 V to 4.0 V
V_{DIN+}, V_{DIN-}	Voltage at DIN+, DIN-(2)	0.5 V to 4.0 V
V _{TH} , V _{DISABLE} , V _{LOS} , V _{OUTPOL} , V _{DOUT+} , V _{DOUT-} , V _{RSSI} , V _{COC1} , V _{COC2}	Voltage at TH, DISABLE, LOS, OUTPOL, DOUT+, DOUT-, RSSI, COC1, COC2 (2)	-0.3 V to 4.0 V
$V_{COC,DIFF}$	Differential voltage between COC1 and COC2	±1 V
$V_{\text{DIN,DIFF}}$	Differential voltage between DIN+ and DIN-	±2.5 V
I _{LOS}	Current into LOS	-1 to 9 mA
I _{DIN+} , I _{DIN-} , I _{DOUT+} , I _{DOUT-}	Continuous current at inputs and outputs	–25 mA to 25 mA
ESD	ESD rating at all pins	2 kV (HBM)
$T_{J(max)}$	Maximum junction temperature	125°C
T _{STG}	Storage temperature range	−65 to 85°C
T _A	Characterized free-air operating temperature range	−40 to 85°C
T _{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T _A	Operating free-air temperature	-40		85	°C
V _{IH}	CMOS input high voltage	2.1			V
V _{IL}	CMOS input low voltage			0.6	V

⁽²⁾ All voltage values are with respect to network ground terminal.



DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage		3	3.3	3.6	V
	Cumply august	DISABLE = low (includes CML output current)		35	45	A
Ivcc	Supply current	DISABLE = low (excludes CML output current)	27 35			mA
V	Differential data autout valtage auting	DISABLE = high		0.25	10	m\/
V _{OD}	Differential data output voltage swing	DISABLE = low, 5 mV _{p-p} \leq V _{IN} \leq 1200 mV _{p-p}	520 760		1200	mV _{p-p}
R _{IN} , R _{OUT}	Data input/output resistance	Single-ended		50		Ω
	DCCI autaut valta aa	Input = 8 mV _{p-p} , $R_{RSSI} \ge 10 \text{ k}\Omega$		200		mV
	RSSI output voltage	Input = 80 mV _{p-p} , $R_{RSSI} \ge 10 \text{ k}\Omega$	1900		1117	
	RSSI linearity	$8 \text{ mV}_{p-p} \le V_{IN} \le 80 \text{ mV}_{p-p}$		±3%		
V _{IN(MIN)}	Data input sensitivity	BER < 10 ⁻¹⁰		3	5	mV_{p-p}
V _{IN(MAX)}	Data input overload		1200			mV_{p-p}
	LOS high voltage	I _{SOURCE} = 30 μA	2.4			V
	LOS low voltage	I _{SINK} = 1 mA			0.4	V

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions, typical operating condition is at $V_{CC} = 3.3 \text{ V}$ and $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequency –3 dB bandwidth		C _{OC} = open		25		1-1-1-
		$C_{OC} = 0.54 \mu F$		0.8		kHz
	Data rate		4.25			Gb/s
v _{NI}	Input referred noise			230		μV_{RMS}
		K28.5 pattern at 4.25 Gbps		3	19	
DJ	Deterministic jitter	K28.5 pattern at 2.125 Gbps		4	35	ps _{p-p}
		K28.5 pattern at 1.0625 Gbps		4	72	
D .	Dandan iittar	Input = 5 mVpp		9		
RJ	Random jitter	Input = 10 mVpp		4		ps _{RMS}
t _R	Output rise time	20% to 80%		45	85	ps
t _F	Output fall time	20% to 80%		45	85	ps
	LOS hysteresis	K28.5 pattern at 4.25 Gbps, 20log (V _{DEA} /V _{AST})	2.5	4.5		dB
R _{TH}	LOS threshold adjustment resistor range	See (1)	1.2		6.8	kΩ
.,	100	$R_{TH} = 2.5 \text{ k}\Omega$, K28.5 pattern at 4.25 Gbps ⁽¹⁾		10		>/
V _{AST}	LOS assert voltage	$R_{TH} = 6.8 \text{ k}\Omega$, K28.5 pattern at 4.25 Gbps ⁽¹⁾	2	5		mV_{p-p}
.,	100 1 11	$R_{TH} = 2.5 \text{ k}\Omega$, K28.5 pattern at 4.25 Gbps ⁽¹⁾		17		.,
V_{DEA}	LOS de-assert voltage	$R_{TH} = 6.8 \text{ k}\Omega$, K28.5 pattern at 4.25 Gbps ⁽¹⁾		8	20	mV_{p-p}
T _{LOS}	LOS assert/deassert time		2		100	μs
T _{DIS}	Disable response time			20		ns

⁽¹⁾ For a given external resistor connected to the TH pin the LOS assert voltage value may vary due to part-to-part variations. If high precision is required, adjustment of this resistor for each device is mandatory.



TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).

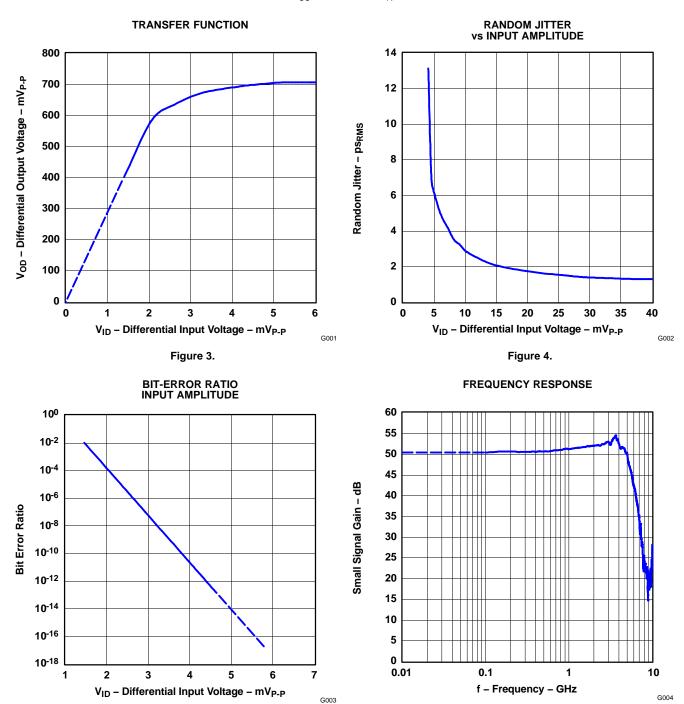


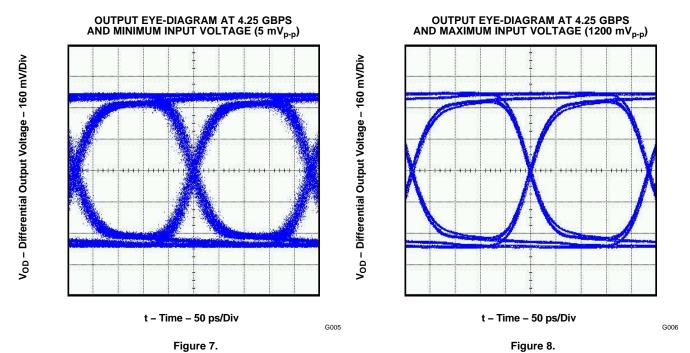
Figure 6.

Figure 5.



TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).





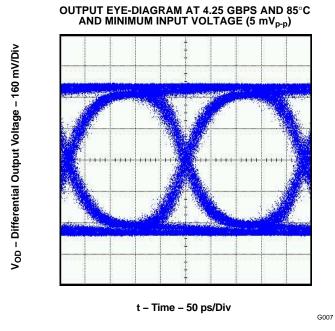
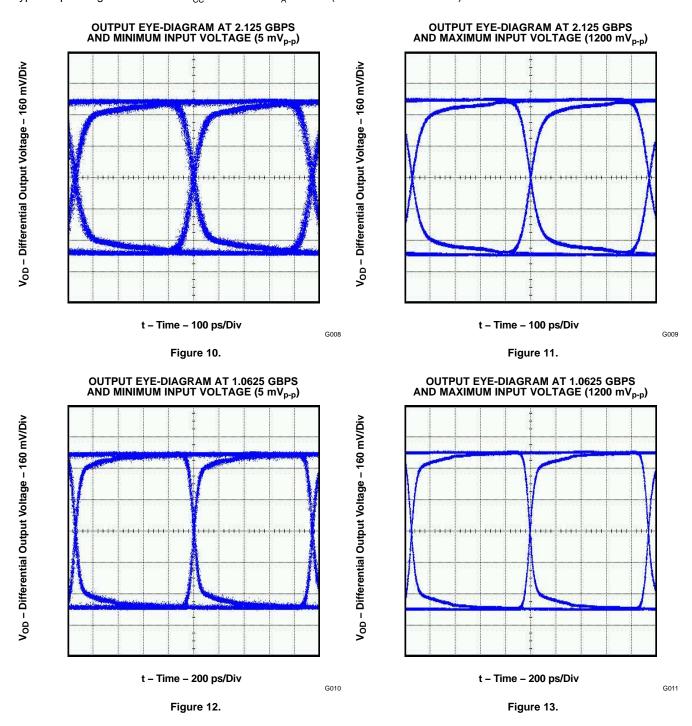


Figure 9.



TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).





TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).

Figure 16.

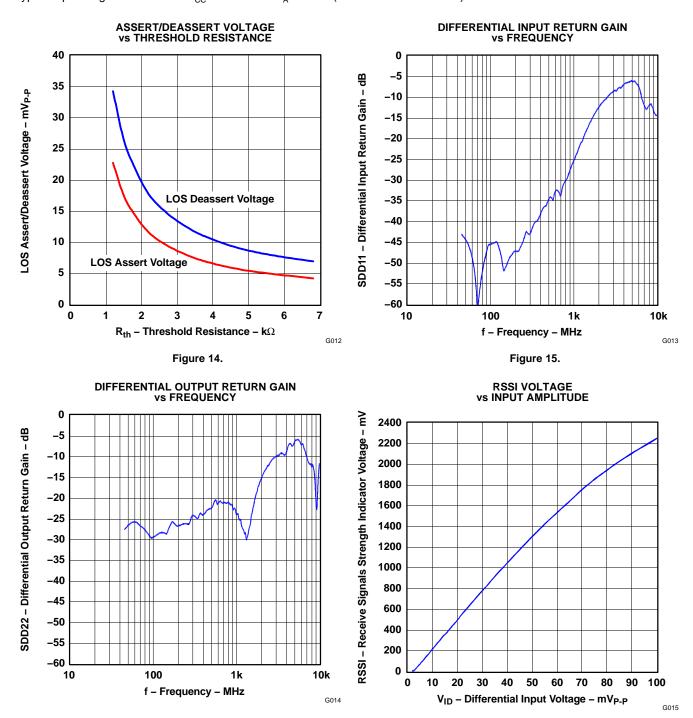


Figure 17.



APPLICATION INFORMATION

Figure 18 shows the ONET4201PA connected with an ac-coupled interface to the data signal source as well as to the output load.

Besides the ac-coupling capacitors C_1 through C_4 in the input and output data signal lines, the only required external component is the LOS threshold setting resistor R_{th} . In addition, an optional external filter capacitor (C_{OC}) may be used if a lower cutoff frequency is desired.

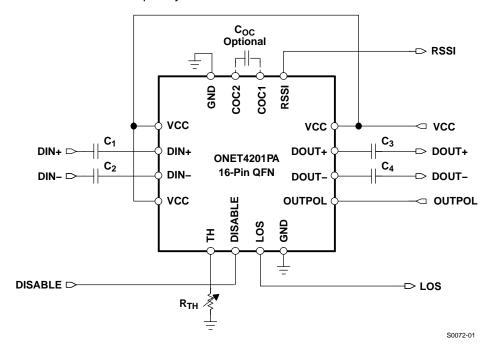


Figure 18. Basic Application Circuit With AC-Coupled I/Os





.com 21-Feb-2006

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
ONET4201PARGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ONET4201PARGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ONET4201PARGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ONET4201PARGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

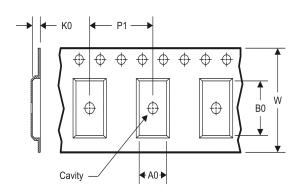
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET4201PARGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ONET4201PARGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ONET4201PARGTR	QFN	RGT	16	3000	338.1	338.1	20.6
ONET4201PARGTT	QFN	RGT	16	250	338.1	338.1	20.6

RGT (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD 3,15 2,85 - A В 3,15 2,85 PIN 1 INDEX AREA TOP AND BOTTOM 0,20 REF. SEATING PLANE 0,08 0,05 0,00 Ċ 16 THERMAL PAD SIZE AND SHAPE SHOWN ON SEPARATE SHEET

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

12

- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.

13

- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

16X $\frac{0,30}{0,18}$

0,50

0,10 M C A B 0,05 M C

4203495/H 10/11

F. Falls within JEDEC MO-220.



RGT (S-PVQFN-N16)

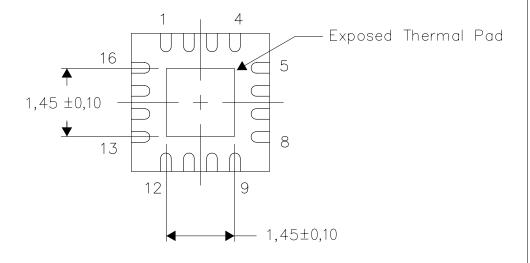
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

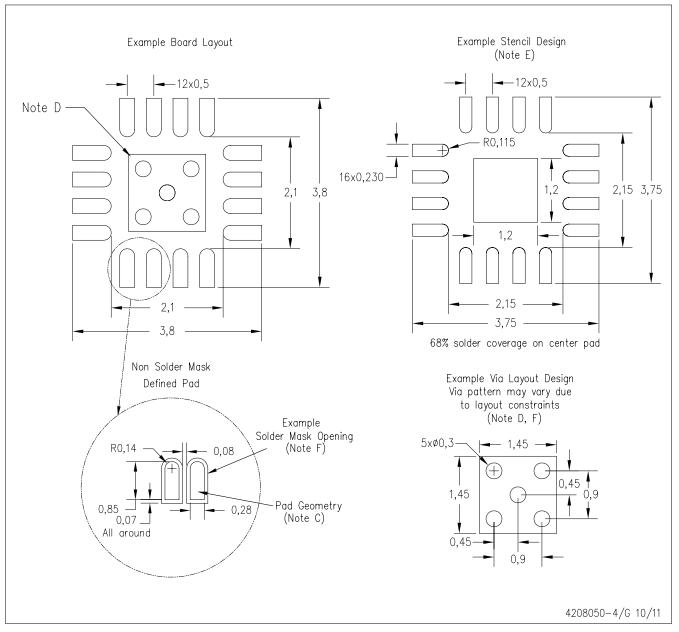
4206349-2/Q 10/11

NOTE: All linear dimensions are in millimeters



RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



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