SN54ABT16841...WD PACKAGE

SCBS222C - SEPTEMBER 1992 - REVISED MAY 1997

- Members of the Texas Instruments
 Widebus™ Family
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 5 V, T_A = 25°C
- High-Impedance State During Power Up and Power Down
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

These 20-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

SN74ABT16841 . . . DL PACKAGE (TOP VIEW) 56 U 1LE 10F 55 1D1 1Q1 **1**2 1Q2 43 54 1D2 GND 4 53 | GND 1Q3 **[**]5 52 1D3 1Q4 **[**]6 51 1D4 50 | V_{CC} V_{CC} 47 1Q5 🛮 8 49 🛮 1D5 1Q6 49 48 1 1D6 1Q7 4 10 47 **∐** 1D7 GND 🛚 11 46 | GND 1Q8 L 12 45 1D8 1Q9 13 44 L 1D9 43 🛮 1D10 1Q10 L 14 2Q1 L 15 42 2D1 2Q2 L 16 41 2D2 2Q3 [] 17 40 2D3 GND L 18 39 l gnd 19 38 2D4 2Q4 L 37 D 2D5 2Q5 **2**0 36 2D6 21 2Q6 L 35 🛮 V_{CC} 22 V_{CC} 2Q7 🛮 23 34 2D7

24

27

28

2Q8 L

2Q10

2OE

GND 25

2Q9 26

33

∐ 2D8

32 | GND

31 2D9

30 D 2D10

29 | 2LE

The 'ABT16841 can be used as two 10-bit latches or one 20-bit latch. The 20 transparent D-type latches provide true data at the outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($1\overline{OE}$ or $2\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



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description (continued)

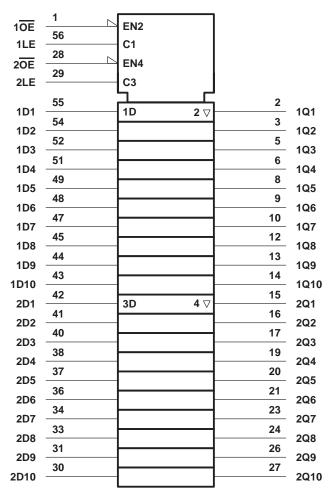
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16841 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16841 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 10-bit latch)

	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q ₀
Н	X	Χ	Z

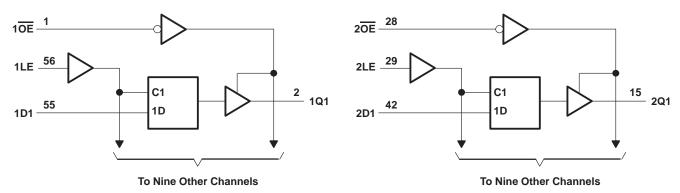
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 7 V
Input voltage range, V _I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V _O	. -0.5 V to 5.5 V
Current into any output in the low state, IO: SN54ABT16841	96 mA
SN74ABT16841	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Package thermal impedance, θ _{JA} (see Note 2): DL package	74°C/W
Storage temperature range, T _{stg}	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 3)

			SN54AB	Г16841	SN74AB1	UNIT	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		V	
V _{IL}	Low-level input voltage		0.8		0.8	V	
VI	Input voltage	0	VCC	0	VCC	V	
IOH	High-level output current			-24		-32	mA
l _{OL}	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



^{2.} The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

SCBS222C - SEPTEMBER 1992 - REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST C	ONDITIONS	Т	A = 25°C	;	SN54AB	Γ16841	SN74AB1	16841	UNIT		
PARAMETER	lesi co	CNUTTIONS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNII		
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2		-1.2		-1.2	V		
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.5			2.5		2.5				
Vou	$V_{CC} = 5 V$,	$I_{OH} = -3 \text{ mA}$	3			3		3		V		
VOH	V _{CC} = 4.5 V	$I_{OH} = -24 \text{ mA}$	2			2				V		
	VCC = 4.5 V	$I_{OH} = -32 \text{ mA}$	2*					2				
VOL	V _{CC} = 4.5 V	I _{OL} = 48 mA			0.55		0.55			V		
VOL	VCC = 4.5 V	I _{OL} = 64 mA			0.55*				0.55	V		
V _{hys}				100						mV		
tı	$V_{CC} = 0 \text{ to } 5.5 \text{ V}$	$V_1 = V_{CC}$ or GND			±1				±1	μΑ		
'1	$V_{CC} = 5 \text{ V}, V_{I} = 7$					±5			μΛ			
lozpu [‡]	$V_{CC} = 0 \text{ to } 2.1 \text{ V}$ $V_{O} = 0.5 \text{ V to } 2.7 \text{ V}$			±50		±50		±50	μА			
IOZPD [‡]	$V_{CC} = 2.1 \text{ V to } 0.000$ $V_{O} = 0.5 \text{ V to } 2.700$			±50		±50		±50	μΑ			
lozh	$V_{CC} = 2.1 \text{ V} \text{ to } 5$ $V_{O} = 2.7 \text{ V}, \overline{\text{OE}} \ge 1$				10		10		10	μΑ		
lozL	$V_{CC} = 2.1 \text{ V to } 5$ $V_{O} = 0.5 \text{ V}, \overline{\text{OE}} \ge 0.5 \text{ V}$				-10		-10		-10	μΑ		
l _{off}	V _C C = 0,	V_I or $V_O \le 4.5 \text{ V}$			±100				±100	μΑ		
I _{CEX} Outputs high	$V_{CC} = 5.5 \text{ V},$	V _O = 5.5 V			50		50		50	μΑ		
IO§	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.5 \text{ V}$	-50	-100	-180	-50	-180	-50	-180	mA		
Outputs high	,, ,,,,				0.5		0.5					
I _{CC} Outputs low	$V_{CC} = 5.5 \text{ V, I}_{O}$ $V_{I} = V_{CC} \text{ or GNI}$				89		89		89	mA		
Outputs disabled	1, 100 3, 91			0.5		0.5		0.5				
ΔICC¶	V _{CC} = 5.5 V, On Other inputs at V			1.5		1.5		1.5	mA			
C _i	$V_{l} = 2.5 \text{ V or } 0.5 \text{ V}$									pF		
Co	V _O = 2.5 V or 0.5	5 V		7.5						pF		

^{*} On products compliant to MIL-PRF-38535, this parameter does not apply.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54A	3T16841	
		V _{CC} = 5 V, T _A = 25°C	MIN MAX	UNIT
		MIN MAX	1	
t _W	Pulse duration, LE high or low	4	4	ns
t _{su}	Setup time, data before LE↓	3	3	ns
th	Hold time, data after LE↓	2.6	2.6	ns



[†] All typical values are at $V_{CC} = 5 \text{ V}$.

[‡] This parameter is characterized, but not production tested.

[§] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[¶] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SCBS222C - SEPTEMBER 1992 - REVISED MAY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		9	N74AB	T16841		
		V _{CC} = T _A = 2	5 V, 25°C	MIN	MAX	UNIT
		MIN MAX				
t _W	Pulse duration, LE high or low	4		4		ns
t _{su}	Setup time, data before LE↓	1		1		ns
th	Hold time, data after LE↓	2		2		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

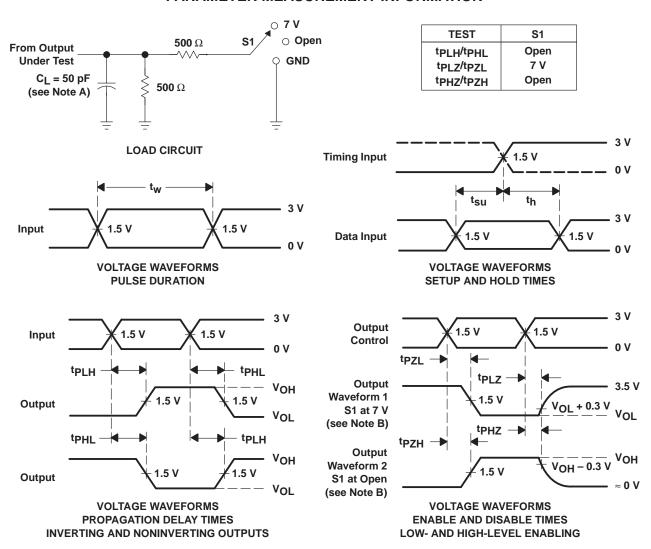
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V ₍	CC = 5 V A = 25°C	/, ;	MIN	MAX	UNIT
				TYP	MAX			
t _{PLH}	D	Q	1.1	3.2	4.3	1.1	5.7	ns
^t PHL	Б	~	1.6	3.5	4.5	1.6	5.3	110
t _{PLH}	LE	Q	1.1	3.2	4.4	1.1	5.6	ns
t _{PHL}	LL	3	1.6	3.4	5	1.6	5.5	113
^t PZH	ŌĒ	Q	1.2	3.2	4.7	1.2	5.8	ns
tPZL	OE	ά	1.7	3.6	5	1.7	5.7	115
^t PHZ	ŌĒ	Q	2.2	4.1	6.6	2.2	7.7	ns
^t PLZ	OE .	ζ	1.9	4.4	5.8	1.2	8.4	115

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN7	4ABT16	841		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V ₍	CC = 5 V 4 = 25°C	/, ;	MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	D	Q	1.1	3.2	4.3	1.1	5	ns
t _{PHL}		Q	1.6	3.5	4.5	1.6	5.1	115
t _{PLH}	LE	Q	1.1	3.2	4.4	1.1	5	ns
t _{PHL}	LL		1.6	3.4	4.6	1.6	5	115
^t PZH	ŌĒ	Q	1.2	3.2	4.7	1.2	5.7	ns
t _{PZL}	OE		1.7	3.6	5	1.7	5.6	115
t _{PHZ}	ŌĒ	Q	2.2	4.1	5.7	2.2	6.5	ne
tPLZ) OE		1.9	4.4	5.8	1.9	7.1	ns 1

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{f} \leq 2.5 \text{ ns.}$
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms







5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9564601QXA	ACTIVE	CFP	WD	56	1	TBD	Call TI	Call TI	
SN74ABT16841DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16841DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16841DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16841DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54ABT16841WD	ACTIVE	CFP	WD	56	1	TBD	A42	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ABT16841, SN74ABT16841:

● Catalog: SN74ABT16841

Military: SN54ABT16841

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications



TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16841DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1





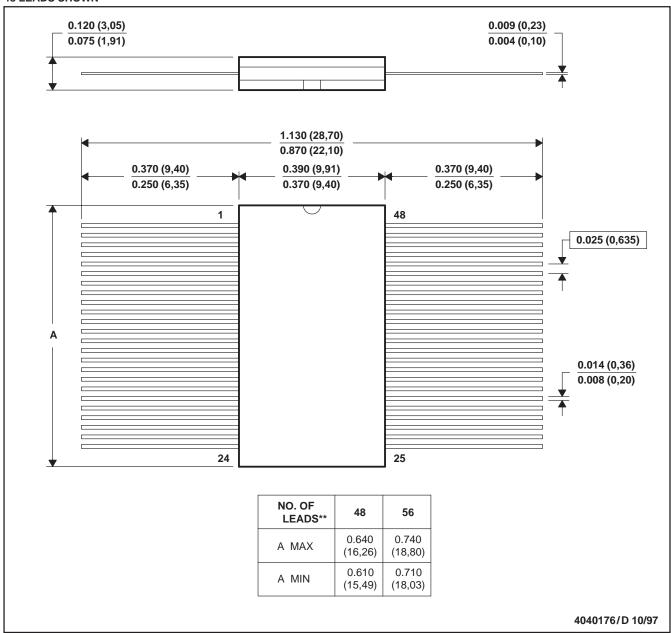
*All dimensions are nominal

ĺ	Device	Package Type	Package Drawing	Pins SPQ		Length (mm)	Width (mm)	Height (mm)	
I	SN74ABT16841DLR	SSOP	DL	56	1000	346.0	346.0	49.0	

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only
- E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA

GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G**)

48 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

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