SDAS098B - OCTOBER 1984 - REVISED JANUARY 1995

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- T/C Determines True or Complementary Data at Q Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

description

These 8-bit latches are designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus. The Q outputs are designed with bus-driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) input when the enable (\overline{EN}) input is low. Data can be read back onto the data inputs by taking the read (\overline{RD}) input low, in addition to having \overline{EN} low. When \overline{EN} is high, both the read-back and write modes are disabled. Transitions on \overline{EN} should only be made with CLK high to prevent false clocking.

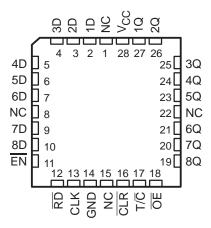
The polarity of the Q outputs can be controlled by the polarity (T/\overline{C}) input. When T/\overline{C} is high, Q is the same as is stored in the flip-flops. When T/\overline{C} is low, the output data is inverted. The Q outputs can be placed in the high-impedance state by taking the output-enable (\overline{OE}) input high. \overline{OE} does not affect the internal operation of the register. Old data can be retained or new data can be entered while the outputs are off.

A low level at the clear ($\overline{\text{CLR}}$) input resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

SN74ALS996 DW OR NT PACKAGE (TOP VIEW)										
1D [2D [3D [3D [5D [5D [5D [5D [7D [8D [8D [8D [7D [8D [7D [8D [7D [7D [7D [7D [7D [7D [7D [7	3 4 5 6 7 8 9 10	24 23 22 21 20 19 18 17 16 15 14 13	VCC 1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q 0E T/C CLR							

SN54ALS996 ... JT PACKAGE

SN54ALS996 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The -1 version of the SN74ALS996 is identical to the standard version, except that the recommended maximum I_{OL} for the -1 version is increased to 48 mA. There is no -1 version of the SN54ALS996.

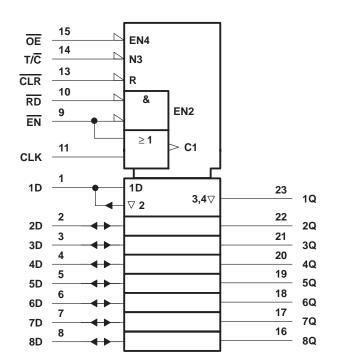
The SN54ALS996 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS996 is characterized for operation from 0°C to 70°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



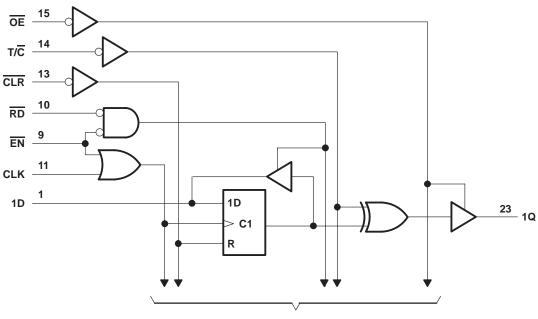
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logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)

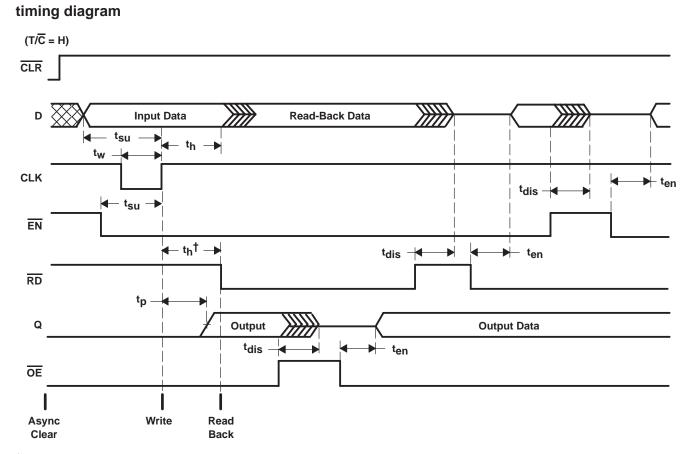


To Seven Other Channels

Pin numbers shown are for the DW, JT, and NT packages.



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[†] This hold time ensures that the read-back circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V _{CC}	
Input voltage, VI (OE, RD, EN, CLK, CLR, and T/C)	
Voltage applied to D inputs and to disabled 3-state outputs	5.5 V
Operating free-air temperature range, T _A : SN54ALS996	55°C to 125°C
SN74ALS996	
Storage temperature range	. −65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



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recommended operating conditions

			SN	SN54ALS996		SN74ALS996			UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V	
		All inputs				2				
VIH	High-level input voltage	All inputs except OE, RD	2						V	
		OE, RD	2.2							
V _{IL}	Low-level input voltage				0.8			0.8	V	
	I Pak Jacob and a summer	Q			-1			-2.6		
IOH	High-level output current	D			-0.4			-0.4	mA	
					12			24		
IOL	Low-level output current	Q						48†	mA	
		D			8			8		
fclock	Clock frequency		0		35	0		35	MHZ	
		CLR low	10			10				
tw	Pulse duration	CLK low	14.5			14.5			ns	
		CLK high	14.5			14.5				
		Data before CLK [↑]	15			15				
	O a transition a	EN low before CLK1	10			10				
t _{su}	Setup time	CLK high before EN↑‡	15			15			ns	
		CLR high (inactive) before CLK [↑]	10			10				
		Data after CLK [↑]	1			0				
t _h	Hold time	EN low after CLK↑	5			5			ns	
		RD high after CLK↑§	5			5				
TA	Operating free-air temperatur	e	-55		125	0		70	°C	

[†] Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25 V [‡] This setup time ensures that EN will not false clock the data register. § This hold time ensures that there will be no conflict on the input data bus.



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PARAMETER			SN	54ALS9	96	SN				
		TEST C	TEST CONDITIONS			MAX	MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lı = – 18 mA			-1.2			-1.2	V
	All outputs	V _{CC} = 4.5 V to 5.5 V,	I _{OH} = - 0.4 mA	Vcc -2	2		V _{CC} -2	2		
∨он		N 45.11	I _{OH} = – 1 mA	2.4	3.2					V
	Q	$V_{CC} = 4.5 V$	I _{OH} = – 2.6 mA				2.4	3.2		
		N 45.11	$I_{OL} = 4 \text{ mA}$		0.25	0.4				
	D	$V_{CC} = 4.5 V$	I _{OL} = 8 mA					0.35	0.5	
VOL	Q $V_{CC} = 4.5$ V		I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		$V_{CC} = 4.5 V$	I _{OL} = 24 mA					0.35	0.5	
			I _{OL} = 48 mA [‡]					0.35	0.5	
IOZH	Q	V _{CC} = 5.5 V,	V _O = 2.7 V			20			20	μΑ
IOZL	Q	V _{CC} = 5.5 V,	V _O = 0.4 V			-20			-20	μΑ
	D inputs		VI = 5.5 V			0.1			0.1	
lj –	All others	V _{CC} = 5.5 V	V _I = 7 V			0.1			0.1	mA
	D inputs§					20			20	
ΙН	All others	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μA
	D inputs§					-0.1			-0.1	
۱ _{IL}	All others	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
IO _l		<u>Vcc</u> = 5.5 V, CLR = 2.5 V	V _O = 2.25 V	-20		-112	-30		-112	mA
ICC			Outputs high		35	55		35	55	
		$\frac{V_{CC} = 5.5 \text{ V},}{\text{EN, RD low}}$	Outputs low		55	85		55	85	mA
			Outputs disabled		42	65		42	65	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

[†] All typical values are at $V_{CC} = 5 \text{ V}, \text{ T}_{A} = 25^{\circ}\text{C}.$

 \ddagger Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25 V

 \S For I/O ports (QA thru QH), the parameters IIH and IIL include the off-state output current.

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



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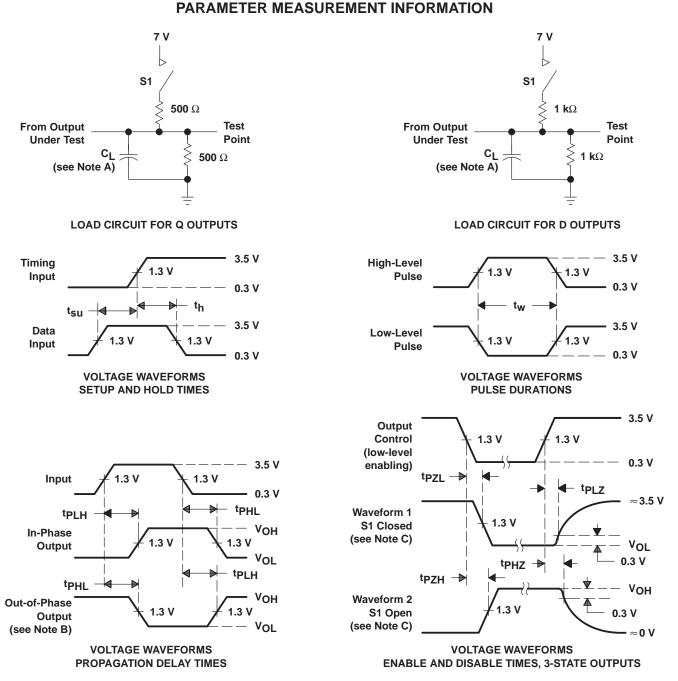
switching characteristics (see Figure 1)

PARAMETER	FROM	то	V _C C _L T _A	UNIT			
	(INPUT)	(OUTPUT)	SN54A	LS996	SN74A	LS996	0.111
			MIN	MAX	MIN	MAX	
fmax			35		35		MHz
^t PLH	CLK (T/C = H or L)	Q	5	30	5	28	20
^t PHL		Q	5	24	5	28	ns
^t PLH	$\overline{\text{CLR}}$ (T/ $\overline{\text{C}}$ = L)	0	5	27	7	27	~~
^t PHL	$\overline{\text{CLR}}$ (T/ $\overline{\text{C}}$ = H)	Q	5	23	7	23	ns
^t PLH	T/C	0	4	23	5	23	20
^t PHL	1/0	Q	5	23	5	23	ns
^t PHL	CLR	D	5	30	8	30	ns
t _{en} ‡		-	2	18	3	16	
t _{dis} §	RD	D	1	19	3	19	ns
t _{en} ‡		5	2	17	3	16	
t _{dis} §	EN	D	1	19	3	19	ns
t _{en} ‡	OE	Q	2	15	4	15	
t _{dis} §	UE	Q	1	11	1	10	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. [‡] t_{en} = t_{PZH} or t_{PZL} § t_{dis} = t_{PHZ} or t_{PLZ}



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NOTES: A. CL includes probe and jig capacitance.

- B. When measuring propagation delay times of 3-state outputs, switch S1 is open.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. All input pulses have the following characteristics: $PRR \le 1$ MHz, $t_f = t_f = 2$ ns, duty cycle = 50%.

Figure 1. Load Circuits and Voltage Waveforms





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5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-89945013A	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Call TI	
5962-8994501LA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Call TI	
SN74ALS996-1DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	
SN74ALS996-1NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS996-1NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS996DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS996DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS996DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS996DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS996DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS996NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS996NT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	
SN74ALS996NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54ALS996FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS996JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS996W	OBSOLETE	CFP	W	24		TBD	A42	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.



5-Sep-2011

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above. Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight

in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ALS996, SN74ALS996 :

Catalog: SN74ALS996

• Military: SN54ALS996

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

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*Δ

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS996DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS996DWR	SOIC	DW	24	2000	346.0	346.0	41.0

MECHANICAL DATA

MCER004A - JANUARY 1995 - REVISED JANUARY 1997

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



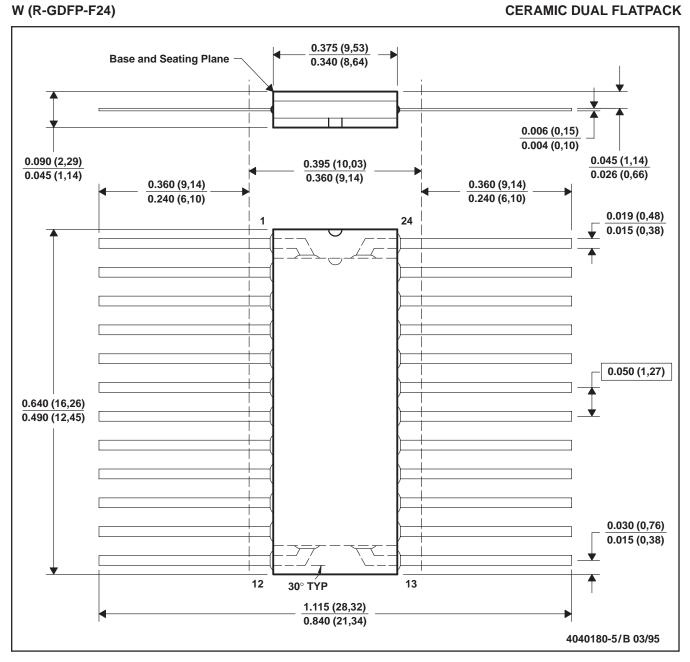
NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB



MECHANICAL DATA

MCFP007 - OCTOBER 1994



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a ceramic lid using glass frit.

- D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
- E. Index point is provided on cap for terminal identification only.



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. Falls within JEDEC MS-004



NT (R-PDIP-T**) 24 pins shown

PLASTIC DUAL-IN-LINE PACKAGE



All integrations are in minimeters. Dimensioning and toil
B. This drawing is subject to change without notice.

The 28 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AD.



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