SCLS453B - FEBRUARY 2001 - REVISED MAY 2003

16 🛛 7 Q

14 6D

13 5D

12 5Q

11 || LE

15 6Q

- 4.5-V to 5.5-V V_{CC} Operation
- Wide Operating Temperature Range of –55°C to 125°C
- **Balanced Propagation Delays and Transition Times**
- Standard Outputs Drive Up To 10 LS-TTL Loads
- Significant Power Reduction Compared to **LS-TTL Logic ICs**
- Inputs Are TTL-Voltage Compatible

description/ordering information

The 'HCT373 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{\mathsf{OE}}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\mathsf{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

TA	PAC	KAGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING						
–55°C to 125°C	PDIP – E	Tube	CD74HCT373E	CD74HCT373E						
	SOIC – M	Tube	CD74HCT373M	НСТ373М						
-55 C 10 125 C	3010 - 111	Tape and reel	CD74HCT373M96							
	CDIP – F	Tube	CD54HCT373F3A	CD54HCT373F3A						

ORDERING INFORMATION

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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CD74HCT373 E OR M PACKAGE (TOP VIEW)									
OE [1 1Q [2 1D [3 2D [4	U ₂₀] V _{CC}] 8Q							
1Q []2	19	_ 8Q							
1D 🛛 3	18	8D							
2D 🛛 4	17	0 7D							

2Q 15

3Q 16

3D 🛛 7

4D 🛛 8

40 9

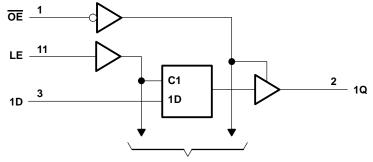
GND 10

CD54HCT373 ... F PACKAGE

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	FUNCTION TABLE (each latch)										
INPUTS OUTPUT											
OE	LE	Q									
L	Н	Н	Н								
L	н	L	L								
L	L	Х	Q ₀ Z								
Н	Х	Х	Z								

logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	
Output clamp current, I_{OK} (V _O < 0 or V _O > V _{CC}) (see Note 1)	±20 mA
Continuous output drain current per output, $I_O (V_O = 0 \text{ to } V_{CC})$	±35 mA
Continuous output source or sink current per output, $I_O (V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	69°C/W
M package	58°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 3)

		T _A = 2	25°C	T _A = - TO 12		T _A = - TO 8		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
VCC	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		2		V
VIL	Low-level input voltage		0.8		0.8		0.8	V
٧I	Input voltage		VCC		VCC		VCC	V
Vo	Output voltage		VCC		VCC		VCC	V
$\Delta t/\Delta v$	Input transition rise or fall rate		500		500		500	ns

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST (Vcc	T _A = 25°C		T _A = −55°C TO 125°C		T _A = −40°C TO 85°C		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	AX V 0.1 V ±1 μΑ
Veu	$V_{I} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -20 \ \mu A$		4.5 V	4.4		4.4		4.4		V
VOH	VI = VIH OL VIL	I _{OH} = –6 mA	4.5 V	3.98		3.7		3.84		v
Vei	VI = VIH or VIL	I _{OL} = 20 μA	4.5 V		0.1		0.1		0.1	V
VOL	VI = VIH OI VIL	I _{OL} = 6 mA	4.5 V		0.26		0.4		0.33	v
Ц	$V_I = V_{CC} \text{ or } 0$		5.5 V		±0.1		±1		±1	μA
loz	$V_{O} = V_{CC} \text{ or } 0$		5.5 V		±0.5		±10		±5	μΑ
Icc	$V_{I} = V_{CC} \text{ or } 0,$	I <mark>O</mark> = 0	5.5 V		8		160		80	μΑ
∆lCC‡	One input at V _{CC} – 2.1	V, Other inputs at 0 or $V_{\mbox{\scriptsize CC}}$	4.5 V to 5.5 V		360		490		450	μΑ
Ci					10		10		10	pF
Co					10		10		10	pF

[‡]Additional quiescent supply current per input pin, TTL inputs high, 1 unit load. For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

		-04	DING	IADL					
IN	PUT	U	UNIT LOAD						
(DE		1.5						
Ar	ıy D		0.4						
l	E		1						
Unit	load	is	∆lcc	limit					
spec	ified	in	elec	ctrical					
chara	acterist	tics	table	(e.a					

HCT INPUT LOADING TABLE

360 μA max at 25°C).



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timing requirements over recommended operating free-air temperature range, V_{CC} = 4.5 V (unless otherwise noted) (see Figure 1)

		T _A = 2	25°C	T _A = - TO 12	-55°C 25°C	T _A = - TO 8	UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	
tw	Pulse duration, LE high	16		24		20		ns
t _{su}	Setup time, data before LE \downarrow	13		20		16		ns
th	Hold time, data after LE \downarrow	10		15		13		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 4.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)			T _A = 25°C	T _A = −55°C TO 125°C	T _A = −40°C TO 85°C	UNIT
		(001F01)	CAPACITANCE	MIN MAX	MIN MAX	MIN MAX	
.	D	Q	$C_{\rm L} = 50 \rm pE$	32	48	40	ns
^t pd	LE	ý	CL = 50 pF	35	53	44	115
^t en	OE	Q	C _L = 50 pF	35	53	44	ns
^t dis	OE	Q	C _L = 50 pF	35	53	44	ns
tt		Q	C _L = 50 pF	12	18	15	ns

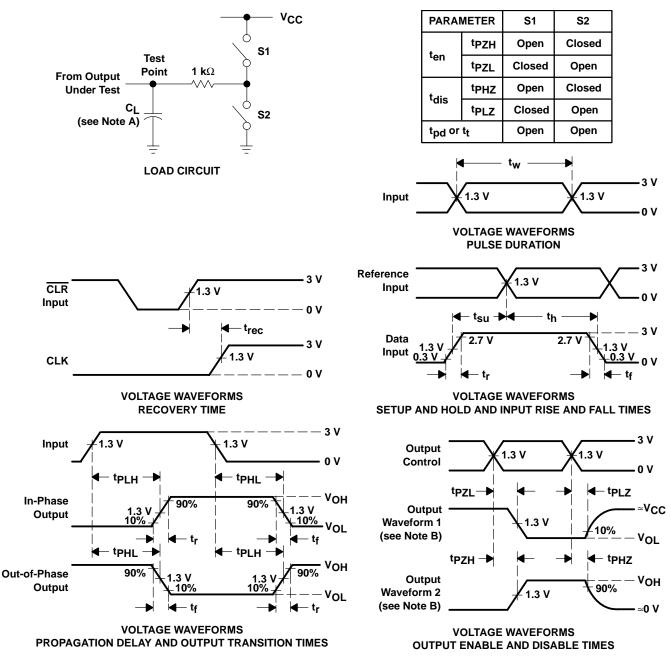
operating characteristics, V_{CC} = 5 V, T_A = 25° C

	PARAMETER					
Cpd	Power dissipation capacitance	53	pF			

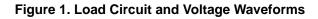


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- NOTES: A. CL includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following
 - characteristics: PRR \leq 1 MHz, Z_Q = 50 Ω , t_f = 6 ns. t_f = 6 ns.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time with one input transition per measurement.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. tpLH and tpHL are the same as t_{pd} .





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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All	dimensions	are	nominal
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Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT373M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT373M96	SOIC	DW	20	2000	346.0	346.0	41.0

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



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PACKAGING INFORMATION

RUMENTS

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD54HCT373F	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
CD54HCT373F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
CD74HCT373E	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT373EE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT373M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT373M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT373M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT373MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All	dimensions	are	nominal
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Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT373M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT373M96	SOIC	DW	20	2000	346.0	346.0	41.0

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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