



# 14-Bit, Quad Channel, Ultra-Low Glitch, Voltage Output DIGITAL-TO-ANALOG CONVERTER with 2.5V, 2ppm/°C Internal Reference

Check for Samples: DAC8164

### FEATURES

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- **Relative Accuracy: 1LSB**
- Glitch Energy: 0.15nV-s
- **Internal Reference:** 
  - 2.5V Reference Voltage (enabled by default)
  - 0.004% Initial Accuracy (typ)
  - 2ppm/°C Temperature Drift (typ)
  - 5ppm/°C Temperature Drift (max)
  - 20mA Sink/Source Capability
- **Power-On Reset to Zero-Scale**
- Ultra-Low Power Operation: 1mA at 5V
- Wide Power Supply Range: +2.7V to +5.5V
- 14-Bit Monotonic Over Temperature Range
- Settling Time: 10µs to ±0.006% Full-Scale Range (FSR)
- Low-Power Serial Interface with Schmitt-Triggered Inputs: Up to 50MHz
- **On-Chip Output Buffer Amplifier with Rail-to-Rail Operation**
- 1.8V to 5.5V Logic Compatibility
- Temperature Range: -40°C to +105°C

### APPLICATIONS

- **Portable Instrumentation**
- **Closed-Loop Servo-Control**
- **Process Control, PLCs**
- **Data Acquisition Systems**
- **Programmable Attenuation**
- PC Peripherals

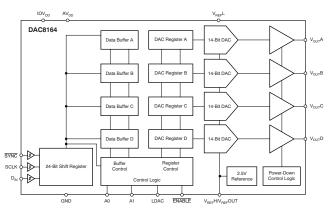
RELATED DEVICES	16-BIT	14-BIT	12-BIT
Pin and Functionally Compatible	DAC8564	DAC8164	DAC7564
Functionally Compatible	DAC8565	DAC8165	DAC7565

## DESCRIPTION

The DAC8164 is a low-power, voltage-output, four-channel, 14-bit digital-to-analog converter (DAC). The device includes a 2.5V, 2ppm/°C internal reference (enabled by default), giving a full-scale output voltage range of 2.5V. The internal reference has an initial accuracy of 0.004% and can source up to 20mA at the V<sub>REF</sub>H/V<sub>REF</sub>OUT pin. The device is monotonic, provides very good linearity, and minimizes undesired code-to-code transient voltages (glitch). The DAC8164 uses a versatile 3-wire serial interface that operates at clock rates up to 50MHz. The interface is compatible with standard SPI™, QSPI™, Microwire™, and digital signal processor (DSP) interfaces.

The DAC8164 incorporates a power-on-reset circuit that ensures the DAC output powers up at zero-scale and remains there until a valid code is written to the device. The device contains a power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 1.3µA at 5V. Power consumption is 2.6mW at 3V, reducing to 1.4µW in power-down mode. The low power consumption, internal reference, and small footprint make this device ideal for portable, battery-operated equipment.

The DAC8164 is drop-in and functionally compatible with the DAC7564 and DAC8564, and functionally compatible with the DAC7565, DAC8165 and DAC8565. All these devices are available in a TSSOP-16 package.





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# DAC8164



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT	RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	REFERENCE DRIFT (ppm/°C)	PACKAGE- LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING							
DAC8164A	±4	±1	25	TSSOP-16	PW	–40°C to +105°C	DAC8164							
DAC8164B	±2	±1	25	TSSOP-16	PW	–40°C to +105°C	DAC8164B							
DAC8164C	±4	±1	5	TSSOP-16	PW	–40°C to +105°C	DAC8164							
DAC8164D	±2	±1	5	TSSOP-16	PW	–40°C to +105°C	DAC8164D							

### PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

### **ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Over operating free-air temperature range (unless otherwise noted).

		DAC8164	UNIT			
AV <sub>DD</sub> to GND		–0.3 to +6	V			
Digital input vol	tage to GND	–0.3 to +V <sub>DD</sub> + 0.3	V			
V <sub>OUT</sub> to GND		–0.3 to +V <sub>DD</sub> + 0.3	V			
V <sub>REF</sub> to GND		-0.3 to +V <sub>DD</sub> + 0.3	V			
Operating temp	perature range	-40 to +125	°C			
Storage temper	rature range	-65 to +150	°C			
Junction tempe	rature range (T <sub>J</sub> max)	+150				
Power dissipati	on	$(T_J max - T_A)/\theta_{JA}$	W			
Thermal imped	ance, θ <sub>JA</sub>	+118	°C/W			
Thermal impedance, $\theta_{JA}$ Thermal impedance, $\theta_{JC}$		+29	°C/W			
COD rating	Human body model (HBM)	4000	V			
ESD rating	Charged device model (CDM)	1500	V			

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



## **ELECTRICAL CHARACTERISTICS**

At AV<sub>DD</sub> = 2.7V to 5.5V and  $-40^{\circ}$ C to  $+105^{\circ}$ C range (unless otherwise noted).

			D	AC8164				
PARAMETER	TES	T CONDITIONS	MIN	TYP M	AX	UNIT		
STATIC PERFORMANCE <sup>(1)</sup>								
Resolution			14			Bits		
	Measured by the line	DAC8164A, DAC8164C		±1	±4	LSB		
Relative accuracy	passing through codes 120 and 16200	DAC8164B, DAC8164D		±1	±2	LSB		
Differential nonlinearity	14-bit monotonic			±0.3	±1	LSB		
Offset error				±5	±8	mV		
Offset error drift	Measured by the line r	bassing through codes 120 and		±1		µV/°C		
Full-scale error	16200.			±0.2 ±	0.5	% of FSR		
Gain error				±0.05 ±	0.2	% of FSR		
0	$AV_{DD} = 5V$			±1		ppm of		
Gain temperature coefficient	AV <sub>DD</sub> = 2.7V			±2		FSR/°C		
PSRR Power-supply rejection rati	o Output unloaded			1		mV/V		
OUTPUT CHARACTERISTICS <sup>(2)</sup>								
Output voltage range			0	V	REF	V		
Output voltage settling time	To ±0.006% FSR, 008 0pF < C <sub>L</sub> < 200pF	0h to 3F40h, $R_L = 2k\Omega$ ,		8	10	μs		
	$R_L = 2k\Omega, C_L = 500pF$			12				
Slew rate				2.2		V/µs		
	R <sub>L</sub> = ∞			470		_		
Capacitive load stability	$R_L = 2k\Omega$			1000		pF		
Code change glitch impulse	1LSB change around	major carry		0.15		nV-s		
Digital feedthrough	SCLK toggling, SYNC	high		0.15		nV-s		
Channel-to-channel dc crosstalk	Full-scale swing on ad	jacent channel		0.25		LSB		
Channel-to-channel ac crosstalk	1kHz full-scale sine wa	ave, outputs unloaded		-100		dB		
DC output impedance	At mid-code input			1		Ω		
Short-circuit current				50		mA		
	Coming out of power-o	down mode, AV <sub>DD</sub> = 5V		2.5				
Power-up time	Coming out of power-o	down mode, AV <sub>DD</sub> = 3V		5		μs		
AC PERFORMANCE <sup>(2)</sup>	L							
SNR				87		dB		
THD	T <sub>A</sub> = +25°C, BW = 20k	KHz, V <sub>DD</sub> = 5V, f <sub>OUT</sub> = 1kHz.		-78		dB		
SFDR		noved for SNR calculation.		79		dB		
SINAD				77		dB		
DAC output noise density	T <sub>A</sub> = +25°C, at mid-co	de input, f <sub>OUT</sub> = 1kHz		120		nV/√Hz		
DAC output noise	T <sub>A</sub> = +25°C, at mid-co	de input, 0.1Hz to 10Hz		6		μV <sub>PP</sub>		
REFERENCE								
	$AV_{DD} = 5.5V$			360		μA		
Internal reference current consumption	AV <sub>DD</sub> = 3.6V			348		μA		
External reference current	External V <sub>REF</sub> = 2.5V, all four channels active	if internal reference is disabled,		80		μA		
Reference input range V <sub>REF</sub> H voltage	$V_{REF}L < V_{REF}H, AV_{DD}$	$-(V_{REF}H + V_{REF}L)/2 > 1.2V$	0	A	/ <sub>DD</sub>	V		
Reference input range V <sub>REF</sub> L voltage	$V_{REF}L < V_{REF}H, AV_{DD}$	$-(V_{REF}H + V_{REF}L)/2 > 1.2V$	0	AV		V		
Reference input impedance				31		kΩ		

Linearity calculated using a reduced code range of 120 to 16200; output unloaded.
 Ensured by design or characterization; not production tested.

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# **ELECTRICAL CHARACTERISTICS (continued)**

At AV<sub>DD</sub> = 2.7V to 5.5V and  $-40^{\circ}$ C to +105°C range (unless otherwise noted).

			C	DAC8164			
	PARAMETER	TEST CONDITIONS	MIN	TYP MAX		UNIT	
REFERENCE	OUTPUT						
Output voltage	)	$T_A = +25^{\circ}C$	2.4975	2.5	2.5025	V	
Initial accuracy	/	$T_A = +25^{\circ}C$	-0.1	±0.004	0.1	%	
	tomporaturo drift	DAC8164A, DAC8164B <sup>(3)</sup>		5	25	nnm/°C	
Output voitage	e temperature drift	DAC8164C, DAC8164D <sup>(4)</sup>		2	5	ppm/°C	
Output voltage	e noise	f = 0.1Hz to 10Hz		12		$\mu V_{PP}$	
		$T_A = +25^{\circ}C, f = 1MHz, C_L = 0\mu F$		50			
Output voltage (high-frequenc		$T_A = +25^{\circ}C, f = 1MHz, C_L = 1\mu F$		20		nV/√Hz	
(ingit noquono		$T_A = +25^{\circ}C, f = 1MHz, C_L = 4\mu F$		16			
Load regulatio	n, sourcing <sup>(5)</sup>	$T_A = +25^{\circ}C$		30		µV/mA	
Load regulatio	n, sinking <sup>(5)</sup>	$T_A = +25^{\circ}C$		15		µV/mA	
Output current	load capability <sup>(6)</sup>			±20		mA	
Line regulation	1	T <sub>A</sub> = +25°C		10		μV/V	
Long-term stat	bility/drift (aging) <sup>(5)</sup>	$T_{A} = +25^{\circ}C$ , time = 0 to 1900 hours		50		ppm	
		First cycle		100			
Thermal hyste	resis <sup>(3)</sup>	Additional cycles		25		ppm	
LOGIC INPUT	S <sup>(6)</sup>	-	I				
Input current				±1		μA	
		$2.7V \le IOV_{DD} \le 5.5V$		0.3	3 × IOV <sub>DD</sub>	· · ·	
V <sub>IN</sub> L	Logic input LOW voltage	$1.8V \le IOV_{DD} \le 2.7V$		0.	1 × IOV <sub>DD</sub>	V	
		$2.7V \le IOV_{DD} \le 5.5V$ $0.7 \times IOV_{DD}$					
V <sub>IN</sub> H	Logic input HIGH voltage	$1.8V \le IOV_{DD} \le 2.7V$	0.95 × IOV <sub>DD</sub>	)		V	
Pin capacitanc	æ			,	3	pF	
POWER REQ					-	·	
AV <sub>DD</sub>			2.7		5.5	V	
IOV <sub>DD</sub>			1.8		5.5	V	
IOI <sub>DD</sub> <sup>(6)</sup>				10	20	μA	
- 00		$AV_{DD} = IOV_{DD} = 3.6V$ to 5.5V V <sub>IN</sub> H = IOV <sub>DD</sub> and V <sub>IN</sub> L = GND		1	1.6		
I <sub>DD</sub> <sup>(7)</sup>	Normal mode	$AV_{DD} = IOV_{DD} = 2.7V \text{ to } 3.6V$ $V_{IN}H = IOV_{DD} \text{ and } V_{IN}L = GND$		0.95	1.5	mA	
DD Y	All power-down modes	$\begin{array}{l} {AV}_{DD} = {IOV}_{DD} = 3.6 V \text{ to } 5.5 V \\ {V}_{IN} H = {IOV}_{DD} \text{ and } {V}_{IN} L = GND \end{array}$		1.3	3.5	μA	
	All power-down modes	$AV_{DD} = IOV_{DD} = 2.7V$ to 3.6V $V_{IN}H = IOV_{DD}$ and $V_{IN}L = GND$		0.5	2.5	μA	
	Normal mode	$AV_{DD} = IOV_{DD} = 3.6V$ to 5.5V $V_{IN}H = IOV_{DD}$ and $V_{IN}L = GND$		3.6	8.8	mW	
Power		$AV_{DD} = IOV_{DD} = 2.7V$ to 3.6V $V_{IN}H = IOV_{DD}$ and $V_{IN}L = GND$		2.6	5.4	mVV	
Dissipation (7)	All power-down modes	$AV_{DD} = IOV_{DD} = 3.6V$ to 5.5V $V_{IN}H = IOV_{DD}$ and $V_{IN}L = GND$		4.7	19	μW	
		$\begin{array}{l} AV_{DD} = IOV_{DD} = 2.7V \text{ to } 3.6V \\ V_{IN}H = IOV_{DD} \text{ and } V_{IN}L = GND \end{array}$		1.4	9	hu	
TEMPERATU	RE RANGE						
Specified perfo	ormance		-40		+105	°C	

(3) Reference is trimmed and tested at room temperature, and is characterized from -40°C to +120°C.

(4) Reference is trimmed and tested at two temperatures (+25°C and +105°C), and is characterized from -40°C to +120°C.

(5) Explained in more detail in the Application Information section of this data sheet.

(6) Ensured by design or characterization; not production tested.

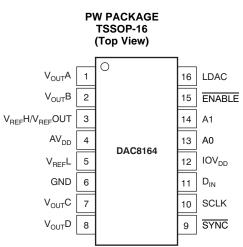
(7) Input code = 8192, reference current included, no load.

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### **PIN CONFIGURATIONS**

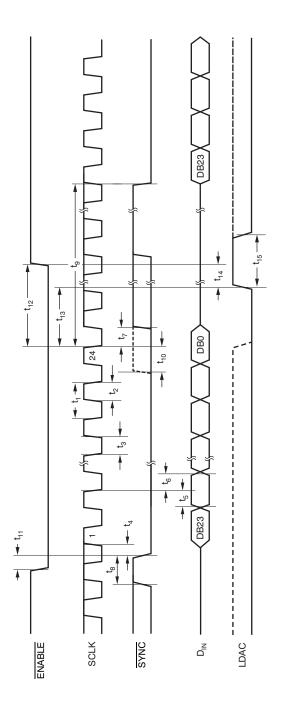


### **PIN DESCRIPTIONS**

PIN	NAME	DESCRIPTION
1	V <sub>OUT</sub> A	Analog output voltage from DAC A
2	V <sub>OUT</sub> B	Analog output voltage from DAC B
3	V <sub>REF</sub> H/ V <sub>REF</sub> OUT	Positive reference input / reference output 2.5V if internal reference used.
4	$AV_{DD}$	Power-supply input, 2.7V to 5.5V
5	$V_{REF}L$	Negative reference input
6	GND	Ground reference point for all circuitry on the part
7	V <sub>OUT</sub> C	Analog output voltage from DAC C
8	V <sub>OUT</sub> D	Analog output voltage from DAC D
9	SYNC	Level-triggered control input (active low). This input is the frame synchronization signal for the input data. When SYNC goes low, it enables the input shift register, and data are sampled on subsequent falling clock edges. The DAC output updates following the 24th clock. If SYNC is taken high before the 24th clock edge, the rising edge of SYNC acts as an interrupt, and the write sequence is ignored by the DAC8164. Schmitt-Trigger logic input.
10	SCLK	Serial clock input. Data can be transferred at rates up to 50MHz. Schmitt-Trigger logic input.
11	D <sub>IN</sub>	Serial data input. Data are clocked into the 24-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input.
12	$IOV_{DD}$	Digital input-output power supply
13	A0	Address 0—sets device address; see Table 5.
14	A1	Address 1—sets device address; see Table 5.
15	ENABLE	The enable pin (active low) connects the SPI interface to the serial port
16	LDAC	Load DACs; rising edge triggered, loads all DAC registers



# SERIAL WRITE OPERATION



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### TIMING REQUIREMENTS<sup>(1)</sup> <sup>(2)</sup>

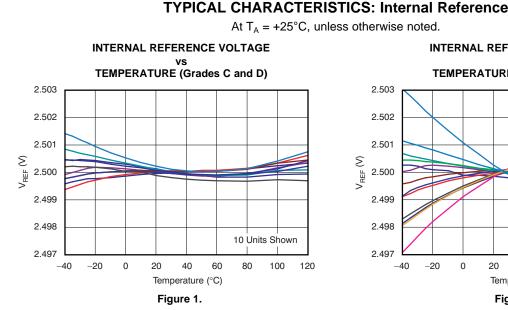
At  $AV_{DD} = IOV_{DD} = 2.7V$  to 5.5V and  $-40^{\circ}C$  to  $+105^{\circ}C$  range (unless otherwise noted).

			D	AC816	4					
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT				
(3)	SCI K avala tima	$IOV_{DD} = AV_{DD} = 2.7V$ to 3.6V	40			2				
1 (*)	SCLK cycle time	$IOV_{DD} = AV_{DD} = 3.6V$ to 5.5V	20			ns				
		$IOV_{DD} = AV_{DD} = 2.7V$ to 3.6V	20							
2	SCLK HIGH time	$IOV_{DD} = AV_{DD} = 3.6V$ to 5.5V	10			ns				
		$IOV_{DD} = AV_{DD} = 2.7V$ to 3.6V	20			20				
3	SCLK LOW time	$IOV_{DD} = AV_{DD} = 3.6V$ to 5.5V	10			ns				
	$IOV_{DD} = AV_{DD} = 2.7V \text{ to } 3.6V$ 0									
4	SYNC to SCLK rising edge setup time	$IOV_{DD} = AV_{DD} = 3.6V$ to 5.5V	0			ns				
	Data astur tima	$IOV_{DD} = AV_{DD} = 2.7V$ to 3.6V	5							
5	Data setup time	$IOV_{DD} = AV_{DD} = 3.6V$ to 5.5V	5			ns				
	Data hold time	$IOV_{DD} = AV_{DD} = 2.7V$ to 3.6V	4.5	4.5						
6	Data hold time	$IOV_{DD} = AV_{DD} = 3.6V$ to 5.5V	4.5			ns				
		0								
,	SCLK falling edge to SYNC rising edge	$IOV_{DD} = AV_{DD} = 3.6V$ to 5.5V	0			ns				
	Minimum SYNC HIGH time	$\frac{10V_{DD} = AV_{DD} = 2.7V \text{ to } 3.6V}{10V_{DD} = 4V_{DD} = 2.7V \text{ to } 3.6V}$								
3	Minimum SYNC HIGH time	$IOV_{DD} = AV_{DD} = 3.6V$ to 5.5V	20			ns				
	$24$ COLIC felling radius to $\overline{O(A)O}$ felling radius	$IOV_{DD} = AV_{DD} = 2.7V \text{ to } 3.6V$				ns				
)	24th SCLK falling edge to SYNC falling edge	IOV <sub>DD</sub> = $AV_{DD}$ = 3.6V to 5.5V								
	SYNC rising edge to 24th SCLK falling edge									
0	(for successful SYNC interrupt)	$IOV_{DD} = AV_{DD} = 3.6V$ to 5.5V	15			ns				
		$IOV_{DD} = AV_{DD} = 2.7V$ to 3.6V	15							
1	ENABLE failing edge to Stric failing edge	$\overrightarrow{ABLE} \text{ falling edge to } \overrightarrow{SYNC} \text{ falling edge} \qquad \overrightarrow{IOV_{DD} = AV_{DD} = 3.6V \text{ to } 5.5V}$				ns				
	24th COLIC felling adapt to ENADLE vising adapt	$IOV_{DD} = AV_{DD} = 2.7V$ to 3.6V	10							
12	24th SCLK falling edge to ENABLE rising edge	$IOV_{DD} = AV_{DD} = 3.6V$ to 5.5V	10			ns				
	24th COLIX felling adapted DAO rising adapt	$IOV_{DD} = AV_{DD} = 2.7V$ to 3.6V	50							
3	24th SCLK falling edge to LDAC rising edge	$IOV_{DD} = AV_{DD} = 3.6V$ to 5.5V	50			ns				
		$IOV_{DD} = AV_{DD} = 2.7V \text{ to } 3.6V$				<i></i>				
4	LDAC rising edge to ENABLE rising edge	$IOV_{DD} = AV_{DD} = 3.6V$ to 5.5V	10			ns				
		$IOV_{DD} = AV_{DD} = 2.7V$ to 3.6V	10							
15	LDAC HIGH time	$IOV_{DD} = AV_{DD} = 3.6V$ to 5.5V	10			ns				

(1) All input signals are specified with  $t_R = t_F = 3ns (10\% \text{ to } 90\% \text{ of } V_{DD})$  and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ . (2) See the Serial Write Operation timing diagram. (3) Maximum SCLK frequency is 50MHz at IOV<sub>DD</sub> =  $V_{DD} = 3.6V$  to 5.5V and 25MHz at IOV<sub>DD</sub> =  $AV_{DD} = 2.7V$  to 3.6V.

EXAS STRUMENTS

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(-40°C to +120°C, Grades C and D)

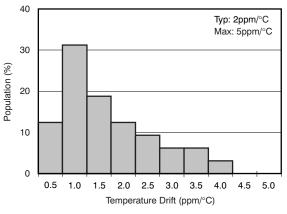
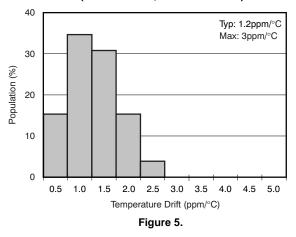
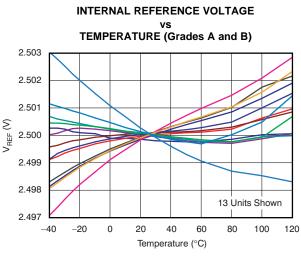


Figure 3.

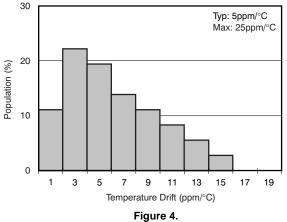
**REFERENCE OUTPUT TEMPERATURE DRIFT** (0°C to +120°C, Grades C and D)





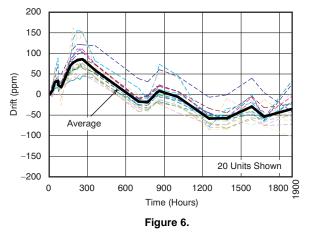


**REFERENCE OUTPUT TEMPERATURE DRIFT** (-40°C to +120°, Grades A and B)



LONG-TERM

STABILITY/DRIFT (1)



Explained in more detail in the Application Information section of this data sheet. (1)



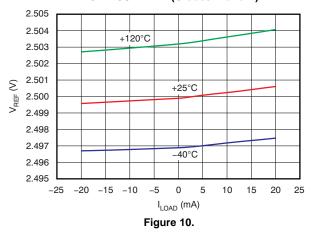
# At $T_A = +25^{\circ}C$ , unless otherwise noted. INTERNAL REFERENCE NOISE DENSITY INTERNAL REFERENCE NOISE vs FREQUENCY 0.1Hz TO 10Hz 12µV (peak-to-peak) V<sub>NOISE</sub> (5µV/div) Reference Unbuffered $C_{REF} = 0 \mu F$ $C_{REF} = 4.8 \mu F$

**TYPICAL CHARACTERISTICS: Internal Reference (continued)** 

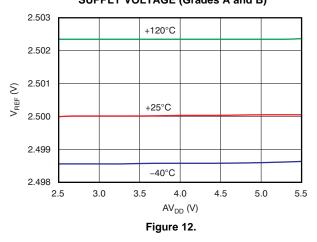
Time (2s/div)

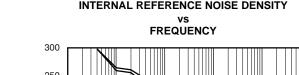
#### Figure 8.

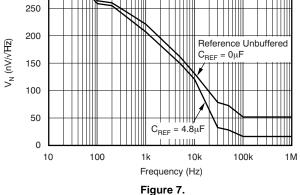




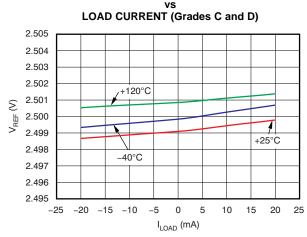
# INTERNAL REFERENCE VOLTAGE vs SUPPLY VOLTAGE (Grades A and B)





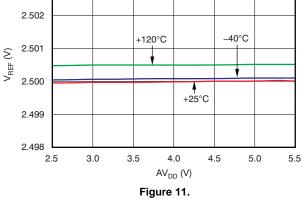






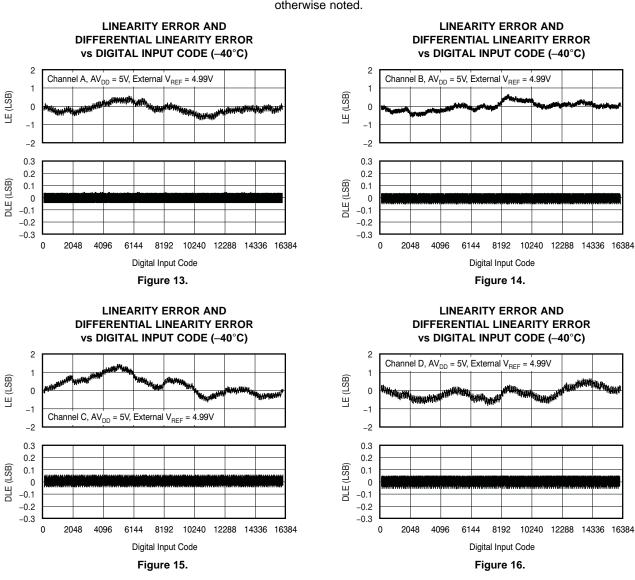


INTERNAL REFERENCE VOLTAGE vs SUPPLY VOLTAGE (Grades C and D)



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# TYPICAL CHARACTERISTICS: DAC at $AV_{DD} = 5V$

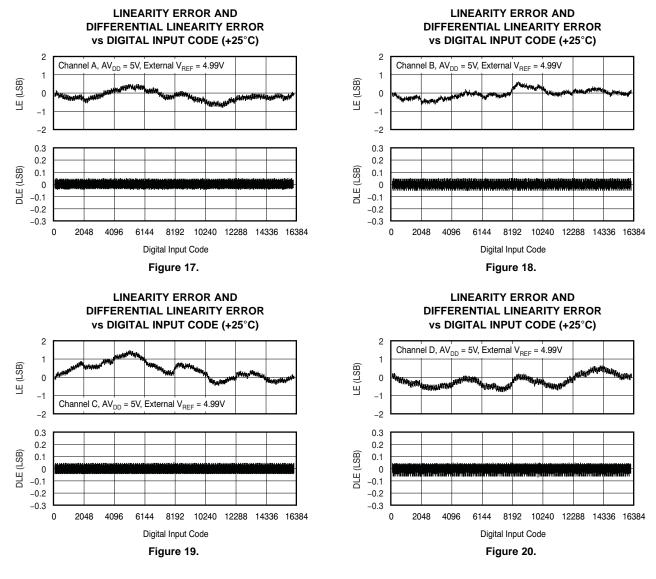
DAC8164



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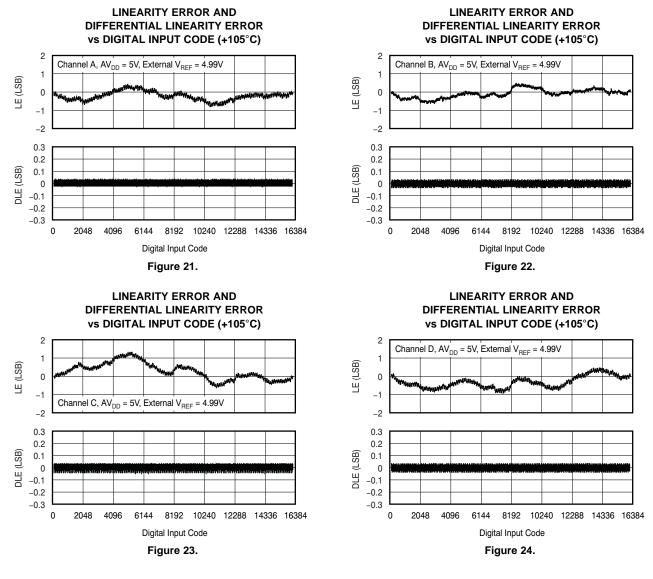
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## TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 5V (continued)



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# TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 5V (continued)



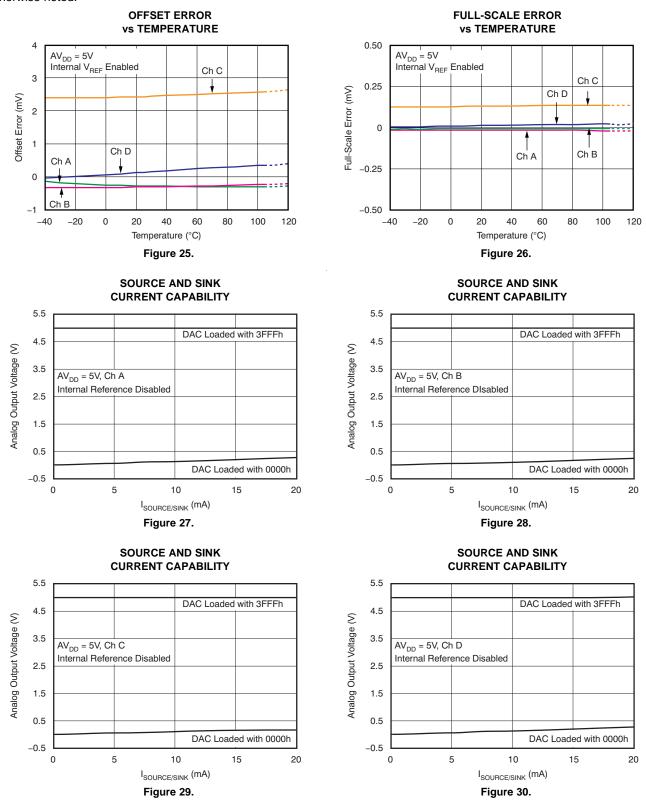
DAC8164



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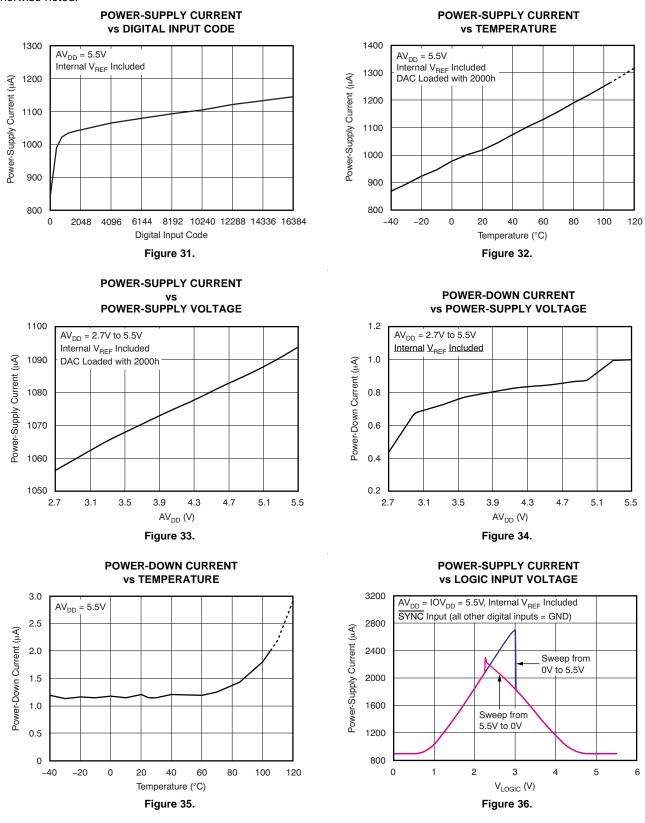
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# TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 5V (continued)



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# TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 5V (continued)



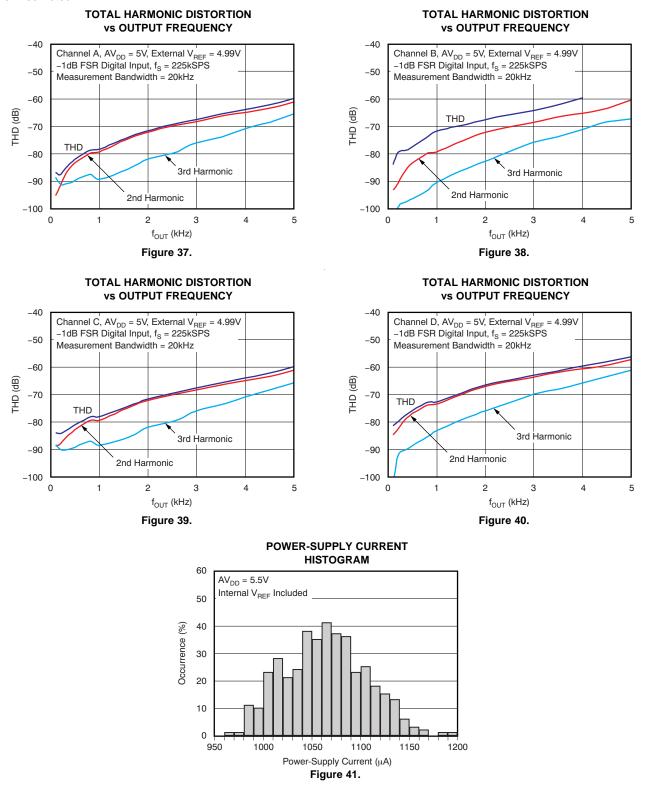


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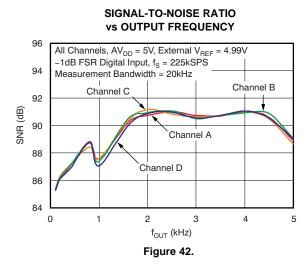
### TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 5V (continued)





### TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 5V (continued)

At T<sub>A</sub> = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.





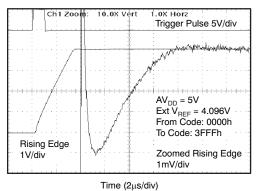
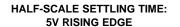
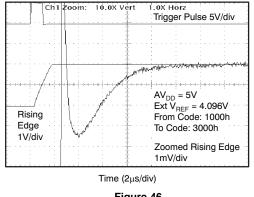


Figure 44.







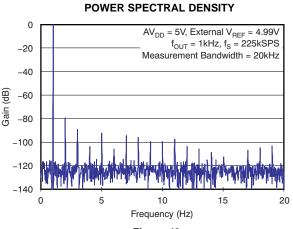


Figure 43.



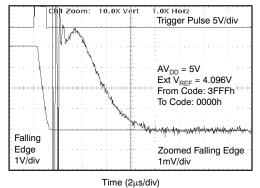
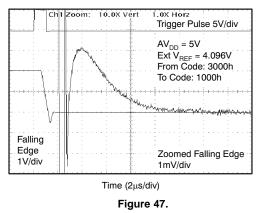


Figure 45.

#### HALF-SCALE SETTLING TIME: **5V FALLING EDGE**





1.0X Horz

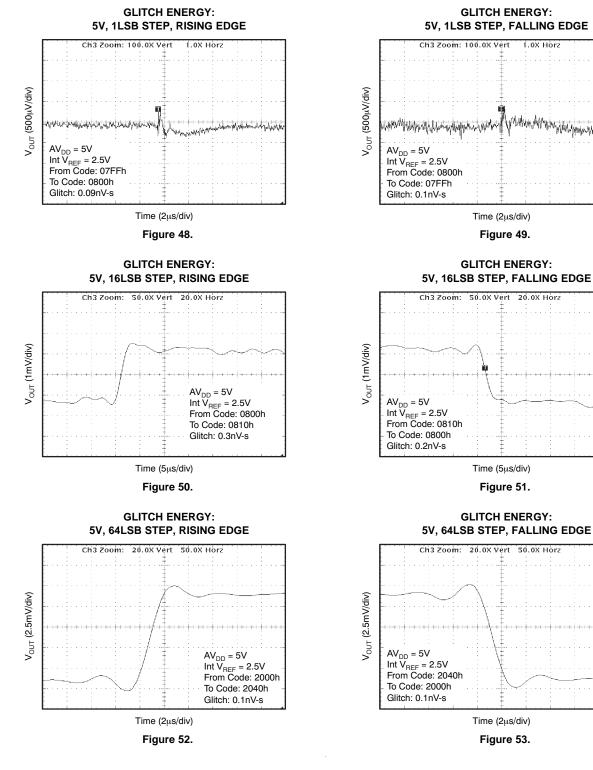
Figure 49.

Figure 51.

Figure 53.

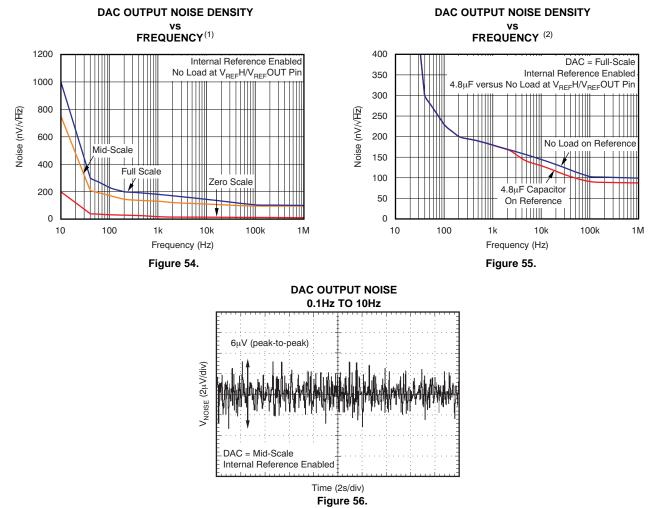
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TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 5V (continued)



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# TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 5V (continued)



- (1) Explained in more detail in the Application Information section of this data sheet.
- (2) See the Application Information section for more information.

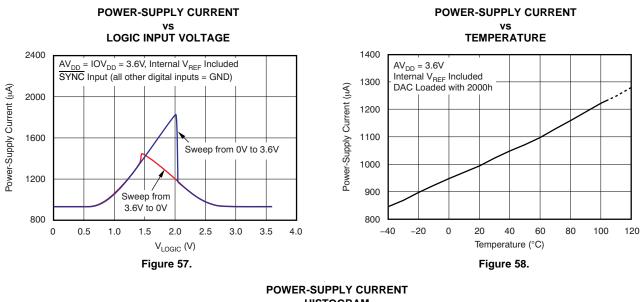




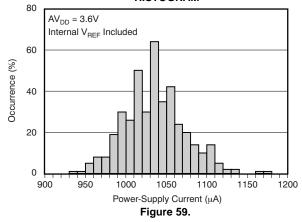
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# TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 3.6V

At T<sub>A</sub> = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

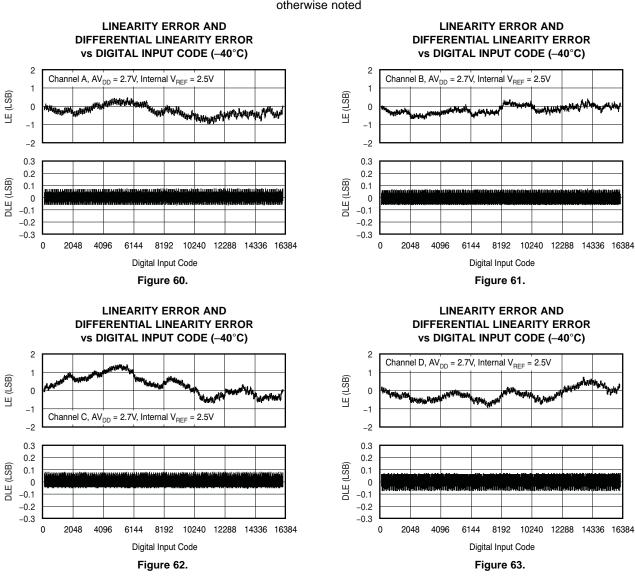


HISTOGRAM





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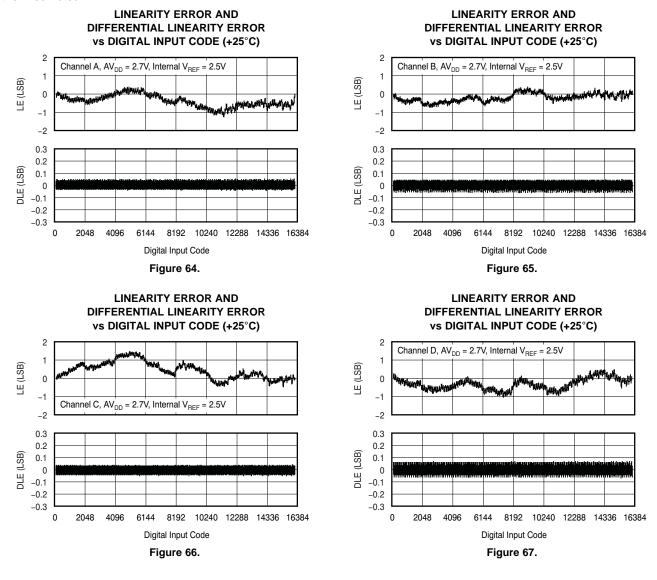


### TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 2.7V



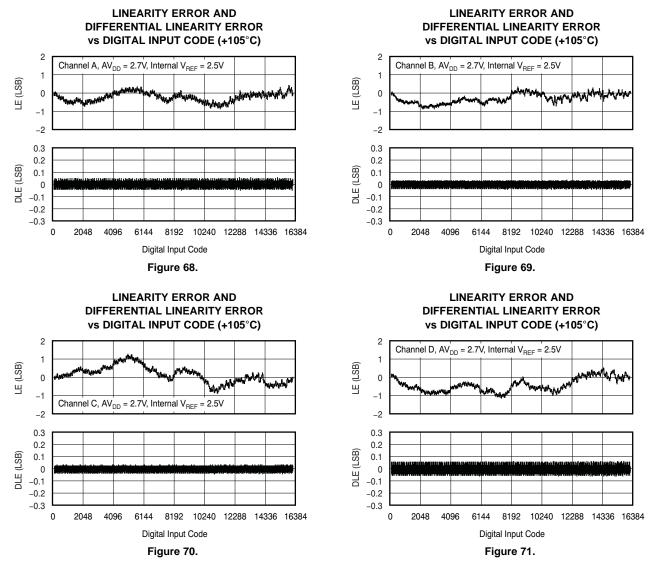
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# TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 2.7V (continued)





# TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 2.7V (continued)



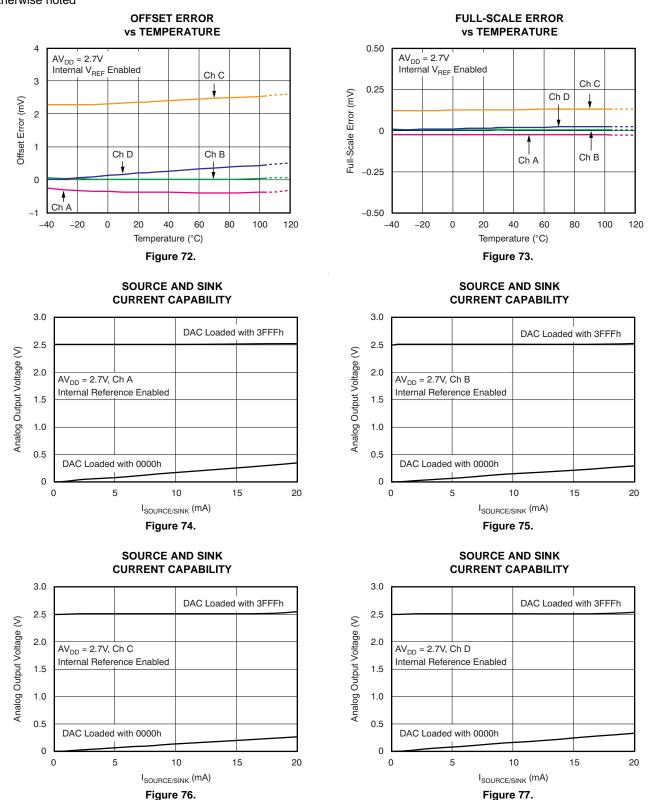


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### TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 2.7V (continued)



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# TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 2.7V (continued)

At T<sub>A</sub> = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

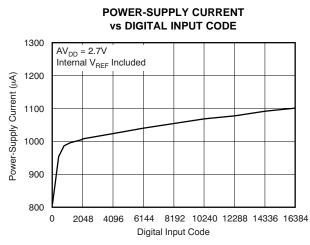


Figure 78.



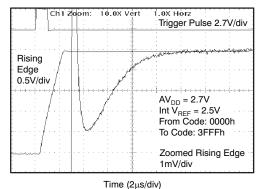
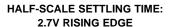
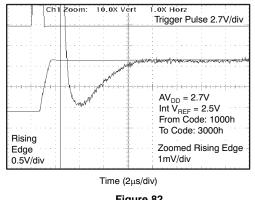
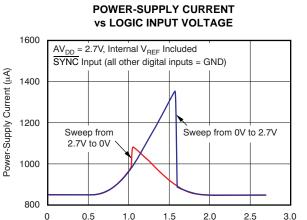


Figure 80.











#### FULL-SCALE SETTLING TIME: 2.7V FALLING EDGE

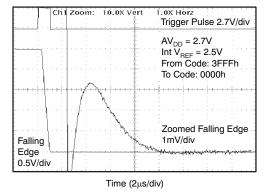
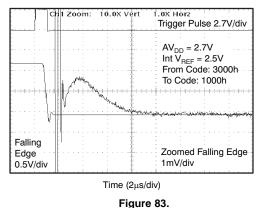


Figure 81.

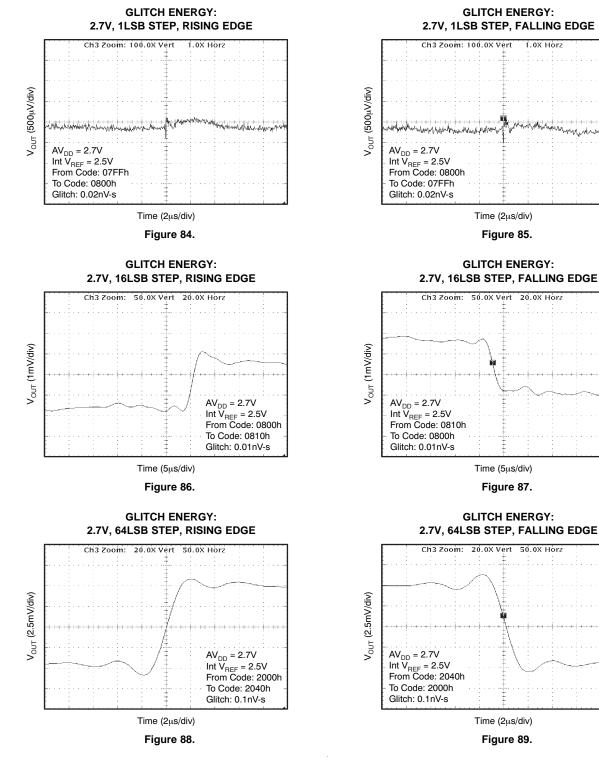
#### HALF-SCALE SETTLING TIME: 2.7V FALLING EDGE





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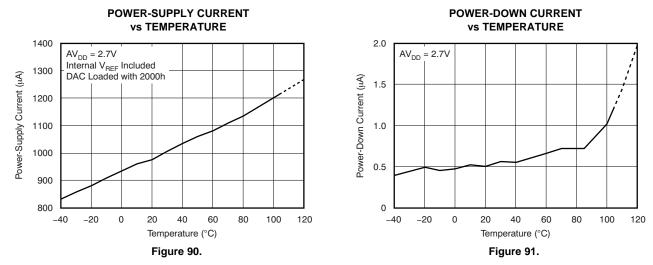
TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 2.7V (continued)





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# TYPICAL CHARACTERISTICS: DAC at AV<sub>DD</sub> = 2.7V (continued)





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# THEORY OF OPERATION

### **DIGITAL-TO-ANALOG CONVERTER (DAC)**

The DAC8164 architecture consists of a string DAC followed by an output buffer amplifier. Figure 92 shows a block diagram of the DAC architecture.

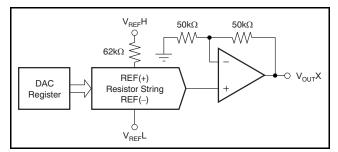


Figure 92. DAC8164 Architecture

The input coding to the DAC8164 is straight binary, so the ideal output voltage is given by Equation 1.

$$V_{OUT}X = 2 \times V_{REF}L + (V_{REF}H - V_{REF}L) \times \frac{D_{IN}}{16384}$$
(1)

where  $D_{IN}$  = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 16383. X represents channel A, B, C, or D.

### **RESISTOR STRING**

The resistor string section is shown in Figure 93. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is monotonic because it is a string of resistors.

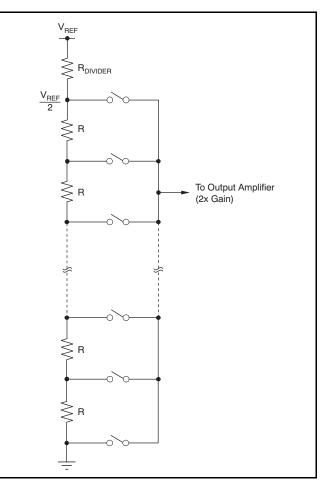


Figure 93. Resistor String

### OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0V to AV<sub>DD</sub>. It is capable of driving a load of  $2k\Omega$  in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics. The slew rate is 2.2V/µs, with a full-scale settling time of 8µs with the output unloaded.

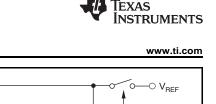
### INTERNAL REFERENCE

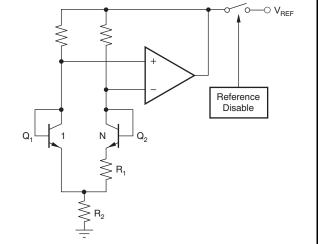
The DAC8164 includes a 2.5V internal reference that is enabled by default. The internal reference is externally available at the  $V_{REF}H/V_{REF}OUT$  pin. A minimum 100nF capacitor is recommended between the reference output and GND for noise filtering.

The internal reference of the DAC8164 is a bipolar transistor-based, precision bandgap voltage reference. Figure 94 shows the basic bandgap topology. Transistors  $Q_1$  and  $Q_2$  are biased such that the current density of  $Q_1$  is greater than that of  $Q_2$ . The difference of the two base-emitter voltages (V<sub>BE1</sub> - V<sub>BE2</sub>) has a positive temperature coefficient and is forced across resistor R1. This voltage is gained up and added to the base-emitter voltage of Q<sub>2</sub>, which has a negative temperature coefficient. The resulting output voltage is virtually independent of temperature. The short-circuit current is limited by design to approximately 100mA.

### Enable/Disable Internal Reference

The internal reference in the DAC8164 is enabled by default and operates in automatic mode; however, the reference can be disabled for debugging, evaluation purposes, or when using an external reference. A serial command that requires a 24-bit write sequence (see the *Serial Interface* section) must be used to disable the internal reference, as shown in Table 1. During the time that the internal reference is disabled, the DAC functions normally using an external reference is disconnected from the V<sub>REF</sub>H/V<sub>REF</sub>OUT pin (3-state output). Do not attempt to drive the V<sub>REF</sub>H/V<sub>REF</sub>OUT pin externally and internally at the same time indefinitely.





### Figure 94. Simplified Schematic of the Bandgap Reference

To then enable the internal reference, either perform a power-cycle to reset the device, or write the 24-bit serial command shown in Table 2. These actions put the internal reference back into the default mode. In the default mode, the internal reference powers down automatically when all DACs power down in any of the power-down modes (see the *Power-Down Modes* section); the internal reference powers up automatically when any DAC is powered up.

The DAC8164 also provides the option of keeping the internal reference powered on all the time, regardless of the DAC(s) state (powered up or down). To keep the internal reference powered on, regardless of the DAC(s) state, write the 24-bit serial command shown in Table 3.

(internal reference always powered down—012000h)											
DB23	DB16 DB13	DB0									
0 0 0 0	0 0 0 1 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0	Х									
	Data Bits										
Table 2. Write Sequence for Enabling Internal Reference           (internal reference powered up to default mode—010000h)											
DB23	DB16	DB0									
0 0 0 0	0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Х									
	Data Bits										
Table 3. Write Sequence for Enabling Internal Reference         (internal reference always powered up—011000h)											
DB23	DB16 DB12	DB0									
0 0 0 0	0 0 0 1 0 0 1 0 0 1 0 X	Х									

Data Bits -

# Table 1. Write Sequence for Disabling Internal Reference (internal reference always powered down—012000h)



### SERIAL INTERFACE

The DAC8164 has a 3-wire serial interface ( $\overline{SYNC}$ , SCLK, and  $D_{IN}$ ) compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See the Serial Write Operation timing diagram for an example of a typical write sequence.

The DAC8164 input shift register is 24 bits wide, consisting of eight control bits (DB23 to DB16) and 14 data bits (DB15 to DB2). Bits DB0 and DB1 are ignored by the DAC and should be treated as don't care bits. All 24 bits of data are loaded into the DAC under the control of the serial clock input, SCLK. DB23 (MSB) is the first bit that is loaded into the DAC shift register, and is followed by the rest of the 24-bit word pattern, left-aligned. This configuration means that the first 24 bits of data are latched into the shift register and any further clocking of data is ignored. The DAC8164 receives all 24 bits of data and decodes the first eight bits to determine the DAC operating/control mode. The 14 bits of data that follow are decoded by the DAC to determine the equivalent analog output, while the last two bits (DB1 and DB0) are ignored. The data format is straight binary with all '0's corresponding to 0V output and all '1's corresponding to full-scale output (that is,  $V_{REF}$  – 1 LSB). For all documentation purposes, the data format and representation here is a true 14-bit pattern (that is, 3FFFh for full-scale), even if the usable 14 bits of data are extracted from a left-justified 16-bit data format that the DAC8164 requires.

The write sequence begins by bringing the SYNC line low. Data from the  $D_{IN}$  line are clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 50MHz, making the DAC8164 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked into the shift register and the shift register locks. Further clocking does not change the shift register data. After 24 bits are locked into the shift register, the eight MSBs are used as control bits and the following 14 LSBs are used as data. After receiving the 24th falling clock edge, the DAC8164 decodes the eight control bits and 14 data bits to perform the required function, without waiting for a SYNC rising edge. A new write sequence starts at the next falling edge of SYNC. A rising edge of SYNC before the 24-bit sequence is complete resets the SPI interface; no data transfer occurs. After the 24th falling edge of SCLK is received, the SYNC line may be kept LOW or brought HIGH. In either case, the minimum delay time from the 24th falling SCLK edge to the next falling SYNC edge must be met in order to properly begin the next cycle. To assure the lowest power consumption of the device, care should be taken that the levels are as close to each rail as possible. Refer to the Typical Characteristics section for Figure 36, Figure 57, and Figure 79 (*Supply Current vs Logic Input Voltage*).

### IOV<sub>DD</sub> AND VOLTAGE TRANSLATORS

The  $IOV_{DD}$  pin powers the the digital input structures of the DAC8164. For single-supply operation, it can be tied to AV<sub>DD</sub>. For dual-supply operation, the IOV<sub>DD</sub> pin provides interface flexibility with various CMOS logic families and should be connected to the logic supply of the system. Analog circuits and internal logic of the DAC8164 use AV<sub>DD</sub> as the supply voltage. The external logic high inputs translate to AV<sub>DD</sub> by level shifters. These level shifters use the IOV<sub>DD</sub> voltage as a reference to shift the incoming logic HIGH levels to AV<sub>DD</sub>. IOV<sub>DD</sub> is ensured to operate from 2.7V to 5.5V regardless of the AV<sub>DD</sub> voltage, assuring compatibility with various logic families. Although specified down to 2.7V, IOV<sub>DD</sub> operates at as low as 1.8V with degraded timing and temperature performance. For lowest power consumption, logic  $V_{\mbox{\scriptsize IH}}$  levels should be as close as possible to  $IOV_{DD}$ , and logic  $V_{IL}$  levels should be as close as possible to GND voltages.

### INPUT SHIFT REGISTER

The input shift register (SR) of the DAC8164 is 24 bits wide, as shown in Table 4, and consists of eight control bits (DB23 to DB16), 14 data bits (DB15 to DB2), and two don't care bits. The first two control bits (DB23 and DB22) are the address match bits. The DAC8164 offers hardware-enabled addressing capability, allowing a single host to talk to up to four DAC8164s through a single SPI bus without any glue logic, enabling up to 16-channel operation. The state of DB23 should match the state of pin A1; similarly, the state of DB22 should match the state of pin A0. If there is no match, the control command and the data (DB21...DB0) are ignored by the DAC8164. That is, if there is no match, the DAC8164 is not addressed. Address matching can be overridden by the broadcast update.

DB23											DB12
A1	A0	LD1	LD0	0	DAC Select 1	DAC Select 0	PD0	D13	D12	D11	D10
DB11											DB0
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Х	Х

### Table 4. Data Input Register Format



LD1 (DB21) and LD0 (DB20) control the loading of each analog output with the specified 14-bit data value or power-down command. Bit DB19 must always be '0'. The DAC channel select bits (DB18, DB17) control the destination of the data (or power-down command) from DAC A through DAC D. The final control bit, PD0 (DB16), selects the power-down mode of the DAC8164 channels as well as the power-down mode of the internal reference.

The DAC8164 supports a number of different load commands. The load commands include broadcast commands to address all the DAC8164s on an SPI bus. The load commands are summarized as follows:

**DB21 = 0 and DB20 = 0: Single-channel store.** The data buffer corresponding to a DAC selected by DB18 and DB17 updates with the contents of SR data (or power-down).

**DB21 = 0 and DB20 = 1: Single-channel update.** The data buffer and DAC register corresponding to a DAC selected by DB18 and DB17 update with the contents of SR data (or power-down).

**DB21 = 1 and DB20 = 0: Simultaneous update.** A channel selected by DB18 and DB17 updates with the SR data; simultaneously, all the other channels update with previously stored data (or power-down) from data buffers.

**DB21 = 1 and DB20 = 1: Broadcast update.** All the DAC8164s on the SPI bus respond, regardless of address matching. If DB18 = 0, SR data are ignored and any channels from all DAC8164s update with previously stored data (or power-down). If DB18 = 1, SR data (or power-down) update any channels of all DAC8164s in the system. This broadcast update feature allows the simultaneous update of up to 16 channels.

Refer to Table 5 for more information.

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13-DB2	DB1-DB0									
A1	A0	LD 1	LD 0	0	DAC Sel 1	DAC Sel 0	PD0	MSB	MSB-1	MSB-2LSB	Don't Care									
(Address	Select)											DESCRIPTION								
0/1	0/1					See	e Below					This address selects one of four possible devices on a single SPI data bus based on the address pin(s) state of each device.								
		0	0	0	0	0	0	Data X				Write to buffer A with data								
	0 0 0 0 1 0 Data X					Х	Write to buffer B with data													
	0		0 0 0 1 0 0				0		Data	a	х	Write to buffer C with data								
A0 and A1 should correspond to the package address		0	0	0	1	1	0		Data	a	х	Write to buffer D with data								
		0	0	0	(00, 01, 1	10, or 11)	1	See	Table 6	0	х	Write to buffer (selected by DB17 and DB18) with power-down command								
		0	1	0	(00, 01, 1	10, or 11)	0		Data	a	х	Write to buffer with data and load DAC (selected by DB17 and DB18)								
set via pin and 14	ns 13	0	1	0	(00, 01, 1	10, or 11)	1	See	Table 6	0	х	Write to buffer with power-down command and load DAC (selected by DB17 and DB18)								
		1	0	0	(00, 01, 1	I0, or 11)	0		Data		х	Write to buffer with data (selected by DB17 and DB18) and then load all DACs simultaneously from their corresponding buffers								
		1	0	0	(00, 01, 1	I0, or 11)	1	See Table 6		See Table 6 0		Write to buffer with power-down command (selected by DB17 and DB18) and then load all DACs simultaneously from their corresponding buffers								
					Br	oadcast Mode	s													
х	х	1	1	0	0	х	х	x			х	Simultaneously update all channels of all DAC8164 devices in the system with data stored in each channels data buffer								
х	х	1	1	0	1	х	0	Data		Data		Data		Data		Data X		Data X		Write to all devices and load all DACs with SR data
х	х	1	1	0	1	х	1	See	Table 6	0	х	Write to all devices and load all DACs with power-down command in SR								

#### Table 5. Control Matrix for the DAC8164



### SYNC INTERRUPT

In a normal write sequence, the SYNC line stays low for at least 24 falling edges of SCLK and the addressed DAC register updates on the 24th falling edge. However, if SYNC is brought high before the 24th falling edge, it acts as an interrupt to the write sequence; the shift register resets and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents, nor a change in the operating mode occurs (as shown in Figure 95).

### **POWER-ON RESET TO ZERO-SCALE**

The DAC8164 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC registers are filled with zeros and the output voltages are set to zero-scale; they remain that way until a valid write sequence and load command are made to the respective DAC channel. The power-on reset is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up.

No device pin should be brought high before power is applied to the device. The internal reference is powered on by default and remains that way until a valid reference-change command is executed.

### LDAC FUNCTIONALITY

The DAC8164 offers both a software and hardware simultaneous update function. The DAC double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs.

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DAC8164 data updates are synchronized with the falling edge of the 24th SCLK cycle, which follows a falling edge of SYNC. For such synchronous updates. the LDAC pin is not required and it must be connected to GND permanently. The LDAC pin is used as a positive edge triggered timing signal for asynchronous DAC updates. To do an LDAC operation, single-channel store(s) should be done (loading DAC buffers) by setting LD0 and LD1 to '0'. Multiple single-channel updates can be done in order to set different channel buffers to desired values and then make a rising edge on LDAC. Data buffers of all channels must be loaded with desired data before an LDAC rising edge. After a low-to-high LDAC transition, all DACs are simultaneously updated with the contents of the corresponding data buffers. If the contents of a data buffer are not changed by the serial interface, the corresponding DAC output remains unchanged after the LDAC trigger.

### ENABLE PIN

For normal operation, the enable pin must be driven to a logic low. If the enable pin is driven high, the DAC81<u>64 stops</u> listening to the serial port. However, SCLK, SYNC, and  $D_{IN}$  must not be kept floating, but must be at some logic level. This feature can be useful for applications that share the same serial port.

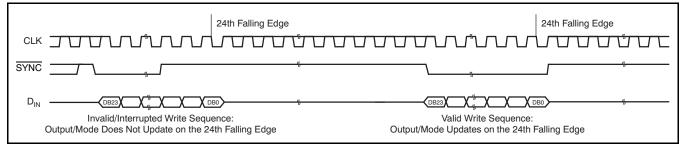


Figure 95. SYNC Interrupt Facility

### **POWER-DOWN MODES**

The DAC8164 has two separate sets of power-down commands. One set is for the DAC channels and the other set is for the internal reference. For more information on powering down the reference, see the *Enable/Disable Internal Reference* section.

### **DAC Power-Down Commands**

The DAC8164 uses four modes of operation. These modes are accessed by setting three bits (PD2, PD1, and PD0) in the shift register. Table 6 shows how to control the operating mode with data bits PD0 (DB16), PD1 (DB15), and PD2 (DB14).

 Table 6. DAC Operating Modes

PD0 (DB16)	PD1 (DB15)	PD2 (DB14)	DAC OPERATING MODES
0	Х	Х	Normal operation
1	0	1	Output typically $1k\Omega$ to GND
1	1	0	Output typically $100k\Omega$ to GND
1	1	1	Output high-impedance

The DAC8164 treats the power-down condition as data; all the operational modes are still valid for power-down. It is possible to broadcast a power-down condition to all the DAC8164s in a system; it is also possible to simultaneously power-down a channel while updating data on other channels.

When the PD0 bit is set to '0', the device works normally with its typical current consumption of 1mAat 5.5V with an input code = 8192. The reference current is included with the operation of all four



DACs. However, for the three power-down modes, the supply current falls to  $1.3\mu$ A at 5.5V ( $0.5\mu$ A at 3.6V). Not only does the supply current fall, but the output stage also switches internally from the output of the amplifier to a resistor network of known values.

The advantage of this switching is that the output impedance of the device is known while it is in power-down mode. As described in Table 6, there are three different power-down options.  $V_{OUT}$  can be connected internally to GND through a 1k $\Omega$  resistor, a 100k $\Omega$  resistor, or open circuited (High-Z). The output stage is shown in Figure 96. In other words, DB16, DB15, and DB14 = '111' represent a power-down condition with Hi-Z output impedance for a selected channel. '101' represents a power-down condition with 1k $\Omega$  output impedance, and '110' represents a power-down condition with 100k $\Omega$  output impedance.

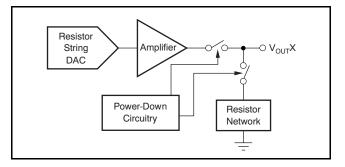


Figure 96. Output Stage During Power-Down

All analog channel circuitries are shut down when the power-down mode is exercised. However, the contents of the DAC register are unaffected when in power down. The time required to exit power-down is typically 2.5 $\mu$ s for V<sub>DD</sub> = 5V, and 5 $\mu$ s for V<sub>DD</sub> = 3V. See the Typical Characteristics for more information.



### **OPERATING EXAMPLES: DAC8164**

For the following examples, ensure that DAC pins A0 and A1 are both connected to ground. Pins A0 and A1 must always match data bits DB22 and DB23 within the SPI write sequence/protocol. X = don't care; value can be either '0' or '1'.

### Example 1: Write to Data Buffer A Through Buffer D; Load DAC A Through DAC D Simultaneously

• 1st: Write to data buffer A:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	0	0	0	0	0	D13	D12	D11	D10-D0	Х

• 2nd: Write to data buffer B:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	0	0	0	1	0	D13	D12	D11	D10-D0	Х

• 3rd: Write to data buffer C:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	0	0	1	0	0	D13	D12	D11	D10-D0	Х

4th: Write to data buffer D and simultaneously update all DACs:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	1	0	0	1	1	0	D13	D12	D11	D10-D0	Х

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously settle to the specified values upon completion of the 4th write sequence. (The DAC voltages update simultaneously after the 24th SCLK falling edge of the fourth write cycle).

### Example 2: Load New Data to DAC A Through DAC D Sequentially

• 1st: Write to data buffer A and load DAC A: DAC A output settles to specified value upon completion:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	1	0	0	0	0	D13	D12	D11	D10-D0	Х

• 2nd: Write to data buffer B and load DAC B: DAC B output settles to specified value upon completion:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	1	0	0	1	0	D13	D12	D11	D10-D0	Х

• 3rd: Write to data buffer C and load DAC C: DAC C output settles to specified value upon completion:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	1	0	1	0	0	D13	D12	D11	D10-D0	Х

• 4th: Write to data buffer D and load DAC D: DAC D output settles to specified value upon completion:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	1	0	1	1	0	D13	D12	D11	D10-D0	Х

After completion of each write cycle, DAC analog output settles to the voltage specified.

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# Example 3: Power-Down DAC A and DAC B to $1k\Omega$ and Power-Down DAC C and DAC D to $100k\Omega$ Simultaneously

1st: Write power-down command to data buffer A: DAC A to 1kΩ.

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	0	0	0	0	1	0	1	Х	Х	Х

2nd: Write power-down command to data buffer B: DAC B to 1kΩ.

B23 A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	0	0	0	1	1	0	1	х	Х	Х

• 3rd: Write power-down command to data buffer C: DAC C to 100kΩ.

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	0	0	1	0	1	1	0	Х	Х	Х

• 4th: Write power-down command to data buffer D: DAC D to 100kΩ and simultaneously update all DACs.

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	1	0	0	1	1	1	1	0	Х	Х	Х

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously power-down to each respective specified mode upon completion of the fourth write sequence.

### Example 4: Power-Down DAC A Through DAC D to High-Impedance Sequentially

• 1st: Write power-down command to data buffer A and load DAC A: DAC A output = Hi-Z:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	1	0	0	0	1	1	1	Х	Х	Х

• 2nd: Write power-down command to data buffer B and load DAC B: DAC B output = Hi-Z:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	1	0	0	1	1	1	1	Х	Х	х

• 3rd: Write power-down command to data buffer C and load DAC C: DAC C output = Hi-Z:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	1	0	1	0	1	1	1	Х	Х	Х

• 4th: Write power-down command to data buffer D and load DAC D: DAC D output = Hi-Z:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB2	DB1-DB0
0	0	0	1	0	1	1	1	1	1	Х	Х	Х

The DAC A, DAC B, DAC C, and DAC D analog outputs sequentially power-down to high-impedance upon completion of the first, second, third, and fourth write sequences, respectively.



DAC8164

### Example 5: Power-Down All Channels Simultaneously while Reference is Always Powered Up

• 1st: Write sequence for enabling the DAC8164 internal reference all the time:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB2	DB1-DB0
0	0	0	0	0	0	0	1	0	0	0	1	Х	Х

#### • 2nd: Write sequence to power-down all DACs to high-impedance:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB2	DB1-DB0
0	0	1	1	0	1	0	1	1	1	Х	Х	Х	Х

The DAC A, DAC B, DAC C, and DAC D analog outputs sequentially power-down to high-impedance upon completion of the first and second write sequences, respectively.

### Example 6: Write a Specific Value to All DACs while Reference is Always Powered Down

 1st: Write sequence for disabling the DAC8164 internal reference all the time (after this sequence, the DAC8164 requires an external reference source to function):

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB2	DB1-DB0
0	0	0	0	0	0	0	1	0	0	1	0	Х	Х

• 2nd: Write sequence to write specified data to all DACs:

B23 A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB2	DB1-DB0
0	0	1	1	0	1	0	0	D13	D12	D11	D10	D9–D0	Х

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously settle to the specified values upon completion of the fourth write sequence. (The DAC voltages update simultaneously after the 24th SCLK falling edge of the fourth write cycle). Reference is always powered-down.

# Example 7: Write a Specific Value to DAC A, while Reference is Placed in Default Mode and All Other DACs are Powered Down to High-Impedance

 1st: Write sequence for placing the DAC8164 internal reference into default mode. Alternately, this step can be replaced by performing a power-on reset (see the *Power-On Reset* section):

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB2	DB1-DB0
0	0	0	0	0	0	0	1	0	0	0	0	Х	Х

 2nd: Write sequence to power-down all DACs to high-impedance (after this sequence, the DAC8164 internal reference powers down automatically):

0B23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB2	DB1-DB0
0	0	1	1	0	1	0	1	1	1	Х	Х	Х	Х

 3rd: Write sequence to power-up DAC A to a specified value (after this sequence, the DAC8164 internal reference powers up automatically):

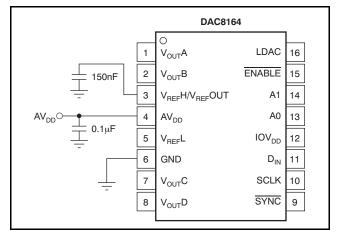
DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB2	DB1-DB0
0	0	0	1	0	0	0	0	D13	D12	D11	D10	D9–D0	Х

The DAC B, DAC C, and DAC D analog outputs simultaneously power-down to high-impedance, and DAC A settles to the specified value upon completion.

### **APPLICATION INFORMATION**

### INTERNAL REFERENCE

The internal reference of the DAC8164 does not require an external load capacitor for stability because it is stable with any capacitive load. However, for improved noise performance, an external load capacitor of 150nF or larger connected to the  $V_{REF}H/V_{REF}OUT$  output is recommended. Figure 97 shows the typical connections required for operation of the DAC8164 internal reference. A supply bypass capacitor at the AV<sub>DD</sub> input is also recommended.



# Figure 97. Typical Connections for Operating the DAC8164 Internal Reference

### Supply Voltage

The internal reference features an extremely low dropout voltage. It can be operated with a supply of only 5mV above the reference output voltage in an unloaded condition. For loaded conditions, refer to the *Load Regulation* section. The stability of the internal reference with variations in supply voltage (line regulation, dc PSRR) is also exceptional. Within the specified supply voltage range of 2.7V to 5.5V, the variation at  $V_{REF}H/V_{REF}OUT$  is less than 10µV/V; see the Typical Characteristics.

### **Temperature Drift**

The internal reference is designed to exhibit minimal drift error, defined as the change in reference output voltage over varying temperature. The drift is calculated using the *box* method described by Equation 2:

Drift Error = 
$$\left(\frac{V_{\text{REF}\_MAX} - V_{\text{REF}\_MIN}}{V_{\text{REF}} \times T_{\text{RANGE}}}\right) \times 10^{6} \text{ (ppm/°C)}$$
(2)

Where:

 $V_{\text{REF}_MAX}$  = maximum reference voltage observed within temperature range  $T_{\text{RANGE}}$ .

 $V_{\text{REF}_{MIN}}$  = minimum reference voltage observed within temperature range  $T_{\text{RANGE}}$ .

 $V_{\text{REF}}$  = 2.5V, target value for reference output voltage.

The internal reference (grades C and D) features an exceptional typical drift coefficient of 2ppm/°C from -40°C to +120°C. Characterizing a large number of units, a maximum drift coefficient of 5ppm/°C (grades C and D) is observed. Temperature drift results are summarized in the Typical Characteristics.

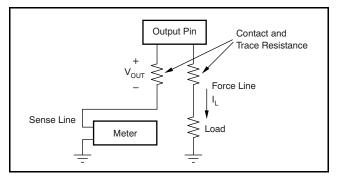
### Noise Performance

Typical 0.1Hz to 10Hz voltage noise can be seen in Figure 8, Internal Reference Noise. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade the ac performance. The output noise spectrum at  $V_{REF}H/V_{REF}OUT$  without any external components is depicted in Figure 7, Internal Reference Noise Density vs Frequency. Another noise density spectrum is also shown in Figure 7. This spectrum was obtained using a 4.8µF load capacitor at  $V_{REF}H/V_{REF}OUT$  for noise filtering. Internal reference noise impacts the DAC output noise; see the DAC Noise Performance section for more details.



### Load Regulation

Load regulation is defined as the change in reference output voltage as a result of changes in load current. The load regulation of the internal reference is measured using force and sense contacts as shown in Figure 98. The force and sense lines reduce the impact of contact and trace resistance, resulting in accurate measurement of the load regulation contributed solely by the internal reference. Measurement results are summarized in the Typical Characteristics. Force and sense lines should be used for applications that require improved load regulation.



# Figure 98. Accurate Load Regulation of the DAC8164 Internal Reference

# Long-Term Stability

Long-term stability/aging refers to the change of the output voltage of a reference over a period of months or years. This effect lessens as time progresses (see Figure 6, the typical long-term stability curve). The typical drift value for the internal reference is 50ppm from 0 hours to 1900 hours. This parameter is characterized by powering-up and measuring 20 units at regular intervals for a period of 1900 hours.

### Thermal Hysteresis

Thermal hysteresis for a reference is defined as the change in output voltage after operating the device at  $+25^{\circ}$ C, cycling the device through the operating temperature range, and returning to  $+25^{\circ}$ C. Hysteresis is expressed by Equation 3:

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$$V_{\text{HYST}} = \left(\frac{|V_{\text{REF}_{PRE}} - V_{\text{REF}_{POST}}|}{V_{\text{REF}_{NOM}}}\right) \times 10^{6} \text{ (ppm/°C)}$$
(3)

Where:

V<sub>HYST</sub> = thermal hysteresis.

 $V_{\text{REF}_{PRE}}$  = output voltage measured at +25°C pre-temperature cycling.

 $V_{\text{REF}_{POST}}$  = output voltage measured after the device cycles through the temperature range of -40°C to +120°C, and returns to +25°C.

# DAC NOISE PERFORMANCE

Typical noise performance for the DAC8164 with the internal reference enabled is shown in Figure 54 to Figure 56. Output noise spectral density at the V<sub>OUT</sub> pin versus frequency is depicted in Figure 54 for full-scale, midscale, and zero-scale input codes. The typical noise density for midscale code is 120nV/ $\sqrt{\text{Hz}}$  at 1kHz and 100nV/ $\sqrt{\text{Hz}}$  at 1MHz. High-frequency noise can be improved by filtering the reference noise as shown in Figure 55, where a 4.8µF load capacitor is connected to the V<sub>REF</sub>H/V<sub>REF</sub>OUT pin and compared to the no-load condition. Integrated output noise between 0.1Hz and 10Hz is close to 6µV<sub>PP</sub> (midscale), as shown in Figure 56.



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### **BIPOLAR OPERATION USING THE DAC8164**

The DAC8164 is designed for single-supply operation, but a bipolar output range is also possible using the circuit in either Figure 99 or Figure 100. The circuit shown gives an output voltage range of  $\pm V_{REF}$ . Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

The output voltage for any input code can be calculated with Equation 4:

$$V_{O} = \left[ V_{REF} \times \left[ \frac{D}{16384} \right] \times \left[ \frac{R_{1} + R_{2}}{R_{1}} \right] - V_{REF} \times \left[ \frac{R_{2}}{R_{1}} \right] \right]$$
(4)

where D represents the input code in decimal (0-16383).

With 
$$V_{\text{REF}}H = 5V$$
,  $R_1 = R_2 = 10k\Omega$ .  
 $V_O = \left(\frac{10 \times D}{16384}\right) - 5V$ 
(5)

This result has an output voltage range of  $\pm$ 5V with 0000h corresponding to a -5V output and 3FFFh corresponding to a +5V output, as shown in Figure 99. Similarly, using the internal reference, a  $\pm$ 2.5V output voltage range can be achieved, as Figure 100 shows.

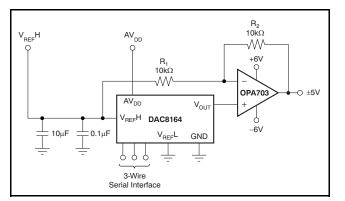


Figure 99. Bipolar Output Range Using External Reference at 5V

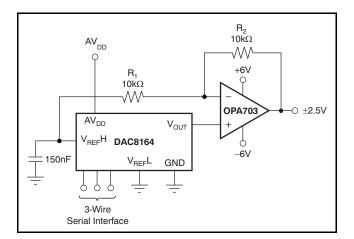


Figure 100. Bipolar Output Range Using Internal Reference



# MICROPROCESSOR INTERFACING

#### **DAC SPI Interfacing**

Care must be taken with the digital control signals that are applied directly to the DAC, especially with the SYNC pin. The SYNC pin must not be toggled without having a full SCLK pulse in between. If this condition is violated, the SPI interface locks up in an erroneous state, causing the DAC to behave incorrectly and have errors. The DAC can be recovered from this faulty state by writing a valid SPI command or using the SYNC pin correctly; communication will then be restored. Avoid glitches and transients on the SYNC line to ensure proper operation.

#### DAC8164 to an 8051 Interface

Figure 101 shows a serial interface between the DAC8164 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8164, while RXD drives the serial data line of the device. The SYNC signal is derived from a bit-programmable pin on the port of the 8051; in this case, port line P3.3 is used. When data are to be transmitted to the DAC8164, P3.3 is taken low. The 8051 transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted; then, a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of the third write cycle. The 8051 outputs the serial data in a format that has the LSB first. The DAC8164 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this requirement into account, and mirror the data as needed.

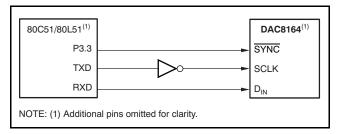


Figure 101. DAC8164 to 80C51/80L51 Interface

#### DAC8164 to Microwire Interface

Figure 102 shows an interface between the DAC8164 and any Microwire-compatible device. Serial data are shifted out on the falling edge of the serial clock and are clocked into the DAC8164 on the rising edge of the SK signal.

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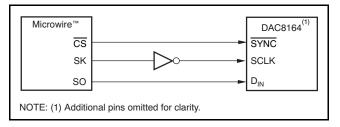


Figure 102. DAC8164 to Microwire Interface

#### DAC8164 to 68HC11 Interface

Figure 103 shows a serial interface between the DAC8164 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8164, while the MOSI output drives the serial data line of the DAC. The SYNC signal derives from a port line (PC7), similar to the 8051 diagram.

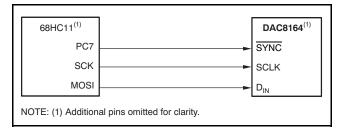


Figure 103. DAC8164 to 68HC11 Interface

The 68HC11 should be configured so that its CPOL bit is '0' and its CPHA bit is '1'. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data are being transmitted to the DAC, the SYNC line is held low (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data are transmitted MSB first.) In order to load data to the DAC8164, PC7 is left low after the first eight bits are transferred; then, a second and third serial write operation are performed to the DAC. PC7 is taken high at the end of this procedure.

TEXAS INSTRUMENTS

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# LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC8164 offers single-supply operation, and is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output.

As a result of the single ground pin of the DAC8164, all return currents (including digital and analog return currents for the DAC) must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system. The power applied to  $V_{DD}$  should be well-regulated and low noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection,  $V_{DD}$  should be connected to a power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1µF to 10µF capacitor and 0.1µF bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the supply and remove the high-frequency noise.



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# PARAMETER DEFINITIONS

With the increased complexity of many different specifications listed in product data sheets, this section summarizes selected specifications related to digital-to-analog converters.

# STATIC PERFORMANCE

Static performance parameters are specifications such as differential nonlinearity (DNL) or integral nonlinearity (INL). These are dc specifications and provide information on the accuracy of the DAC. They are most important in applications where the signal changes slowly and accuracy is required.

### Resolution

Generally, the DAC resolution can be expressed in different forms. Specifications such as IEC 60748-4 recognize the numerical, analog, and relative resolution. The numerical resolution is defined as the number of digits in the chosen numbering system necessary to express the total number of steps of the transfer characteristic, where a step represents both a digital input code and the corresponding discrete analogue output value. The most commonly-used definition of resolution provided in data sheets is the numerical resolution expressed in bits.

#### Least Significant Bit (LSB)

The least significant bit (LSB) is defined as the smallest value in a binary coded system. The value of the LSB can be calculated by dividing the full-scale output voltage by  $2^n$ , where *n* is the resolution of the converter.

#### Most Significant Bit (MSB)

The most significant bit (MSB) is defined as the largest value in a binary coded system. The value of the MSB can be calculated by dividing the full-scale output voltage by 2. Its value is one-half of full-scale.

#### **Relative Accuracy or Integral Nonlinearity (INL)**

Relative accuracy or integral nonlinearity (INL) is defined as the maximum deviation between the real transfer function and a straight line passing through the endpoints of the ideal DAC transfer function. DNL is measured in LSBs.

#### **Differential Nonlinearity (DNL)**

Differential nonlinearity (DNL) is defined as the maximum deviation of the real LSB step from the ideal 1LSB step. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. If the DNL is less than 1LSB, the DAC is said to be monotonic.

#### **Full-Scale Error**

Full-scale error is defined as the deviation of the real full-scale output voltage from the ideal output voltage while the DAC register is loaded with the full-scale code. Ideally, the output should be  $V_{DD} - 1$  LSB. The full-scale error is expressed in percent of full-scale range (%FSR).

#### Offset Error

The offset error is defined as the difference between actual output voltage and the ideal output voltage in the linear region of the transfer function. This difference is calculated by using a straight line defined by two codes. Since the offset error is defined by a straight line, it can have a negative or positve value. Offset error is measured in mV.

#### Zero-Code Error

The zero-code error is defined as the DAC output voltage, when all '0's are loaded into the DAC register. Zero-scale error is a measure of the difference between actual output voltage and ideal output voltage (0V). It is expressed in mV. It is primarily caused by offsets in the output amplifier.

#### Gain Error

Gain error is defined as the deviation in the slope of the real DAC transfer characteristic from the ideal transfer function. Gain error is expressed as a percentage of full-scale range (%FSR).

#### Full-Scale Error Drift

Full-scale error drift is defined as the change in full-scale error with a change in temperature. Full-scale error drift is expressed in units of %FSR/°C.

#### Offset Error Drift

Offset error drift is defined as the change in offset error with a change in temperature. Offset error drift is expressed in  $\mu$ V/°C.

#### Zero-Code Error Drift

Zero-code error drift is defined as the change in zero-code error with a change in temperature. Zero-code error drift is expressed in  $\mu$ V/°C.

#### **Gain Temperature Coefficient**

The gain temperature coefficient is defined as the change in gain error with changes in temperature. The gain temperature coefficient is expressed in ppm of FSR/°C.

# Power-Supply Rejection Ratio (PSRR)

Power-supply rejection ratio (PSRR) is defined as the ratio of change in output voltage to a change in supply voltage for a full-scale output of the DAC. The PSRR of a device indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is measured in decibels (dB).

# Monotonicity

Monotonicity is defined as a slope whose sign does not change. If a DAC is monotonic, the output changes in the same direction or remains at least constant for each step increase (or decrease) in the input code.

# DYNAMIC PERFORMANCE

Dynamic performance parameters are specifications such as settling time or slew rate, which are important in applications where the signal rapidly changes and/or high frequency signals are present.

# **Slew Rate**

The output slew rate (SR) of an amplifier or other electronic circuit is defined as the maximum rate of change of the output voltage for all possible input signals.

$$SR = \max\left[\left|\frac{\Delta V_{OUT}(t)}{\Delta t}\right|\right]$$

Where  $\Delta V_{OUT}(t)$  is the output produced by the amplifier as a function of time *t*.

# **Output Voltage Settling Time**

Settling time is the total time (including slew time) for the DAC output to settle within an error band around its final value after a change in input. Settling times are specified to within  $\pm 0.003\%$  (or whatever value is specified) of full-scale range (FSR).

# Code Change/Digital-to-Analog Glitch Energy

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nanovolts-second (nV-s), and is measured when the digital input code changes by 1LSB at the major carry transition.

# **Digital Feedthrough**

Digital feedthrough is defined as impulse seen at the output of the DAC from the digital inputs of the DAC. It is measured when the DAC output is not updated. It is specified in nV-s, and measured with a full-scale code change on the data bus; that is, from all '0's to all '1's and vice versa.

# Channel-to-Channel DC Crosstalk

Channel-to-channel dc crosstalk is defined as the dc change in the output level of one DAC channel in response to a change in the output of another DAC channel. It is measured with a full-scale output change on one DAC channel while monitoring another DAC channel remains at midscale; it is expressed in LSB.

# **Channel-to-Channel AC Crosstalk**

AC crosstalk in a multi-channel DAC is defined as the amount of ac interference experienced on the output of a channel at a frequency (f) (and its harmonics), when the output of an adjacent channel changes its value at the rate of frequency (f). It is measured with one channel output oscillating with a sine wave frequency of 1kHz, while monitoring the amplitude of 1kHz harmonics on an adjacent DAC channel output (kept at zero scale); it is expressed in dB.

# Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio (SNR) is defined as the ratio of the root mean-squared (RMS) value of the output signal divided by the RMS values of the sum of all other spectral components below one-half the output frequency, not including harmonics or dc. SNR is measured in dB.

# **Total Harmonic Distortion (THD)**

Total harmonic distortion + noise is defined as the ratio of the RMS values of the harmonics and noise to the value of the fundamental frequency. It is expressed in a percentage of the fundamental frequency amplitude at sampling rate  $f_{S}$ .

# Spurious-Free Dynamic Range (SFDR)

Spurious-free dynamic range (SFDR) is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. SFDR is the measure of the difference in amplitude between the fundamental and the largest harmonically or non-harmonically related spur from dc to the full Nyquist bandwidth (half the DAC sampling rate, or  $f_S/2$ ). A spur is any frequency bin on a spectrum analyzer, or from a Fourier transform, of the analog output of the DAC. SFDR is specified in decibels relative to the carrier (dBc).

# Signal-to-Noise plus Distortion (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing any internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate,  $f_S$ .





#### **DAC Output Noise Density**

Output noise density is defined as internally-generated random noise. Random noise is characterized as a spectral density  $(nV/\sqrt{Hz})$ . It is measured by loading the DAC to midscale and measuring noise at the output.

#### DAC Output Noise

DAC output noise is defined as any voltage deviation of DAC output from the desired value (within a particular frequency band). It is measured with a DAC channel kept at midscale while filtering the output voltage within a band of 0.1Hz to 10Hz and measuring its amplitude peaks. It is expressed in terms of peak-to-peak voltage ( $V_{pp}$ ).

#### Full-Scale Range (FSR)

Full-scale range (FSR) is the difference between the maximum and minimum analog output values that the DAC is specified to provide; typically, the maximum and minimum values are also specified. For an *n*-bit DAC, these values are usually given as the values matching with code 0 and  $2^n$ .

SBAS410B-FEBRUARY 2008-REVISED MAY 2011

# **REVISION HISTORY**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	Changes from Revision A (February 2008) to Revision B Page							
•	Changed Output Voltage parameter min/max values from 2.4995 and 2.5005 to 2.4975 and 2.5025, respectively							
•	Changed Initial Accuracy parameter min/max values from -0.02 and 0.02 to -0.1 and 0.1, respectively 4							
•	Changed values for SCLK High TIme parameter from 20 and 10 to 10 and 20							
•	Added DAC SPI Interfacing subsection to Microprocessor Interfacing section							



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6-May-2011

# **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
DAC8164IAPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164IAPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164IAPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164IAPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164IBPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164IBPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164IBPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164IBPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164ICPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164ICPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164ICPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164ICPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164IDPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164IDPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164IDPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8164IDPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

<sup>(1)</sup> The marketing status values are defined as follows:



6-May-2011

ACTIVE: Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# PACKAGE MATERIALS INFORMATION

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# TAPE AND REEL INFORMATION





# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8164IAPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC8164IBPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC8164ICPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC8164IDPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TEXAS INSTRUMENTS

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# PACKAGE MATERIALS INFORMATION

5-May-2011



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8164IAPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
DAC8164IBPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
DAC8164ICPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
DAC8164IDPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  $\beta$ . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



# LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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