SN54259, SN54LS259B, SN74259, SN74LS259B 8-BIT ADDRESSABLE LATCHES

SDLS086 – DECEMBER 1983 – REVISED MARCH 1988

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplified Expansion
- Expandable for N-Bit Applications
- Four District Functional Modes
- Package Options Include Ceramic Chip Carriers and Flat Packages in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{\text{CLR}}$) and enable ($\overline{\text{G}}$) inputs as enumerated in the function table. In the addressablelatch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable $\overline{\text{G}}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

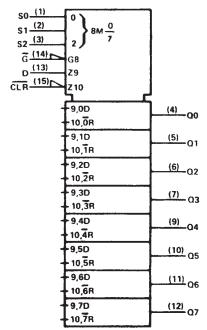
The SN54259 and SN54LS259B are characterized for operation over the full military temperature range of -55° C to 125°C. The SN74259 and SN74LS259B are characterized for operation from 0°C to 70°C.

SN54259, SN54LS259B J OR W PACKAGE SN74259 N PACKAGE SN74LS259B D OR N PACKAGE (TOP VIEW)									
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$									
SN54LS259B FK PACKAGE (TOP VIEW)									
$ \begin{array}{c} & 5 \\ & 7 \\ & 17 \\ & 10 \\ & 1$									
$\begin{array}{cccc} NC \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ $									

NC - No internal connection

B & S & B

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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FUNCTION TABLE

INPUT	s	OUTPUT OF	EACH OTHER	FUNCTION
CLR	G	LATCH	OUTPUT	FONCTION
н	L	D	Q _{i0}	Addressable Latch
н	н	Q _{i0}	Q _{iO}	Memory
L	L,	D	L	8-Line Demultiplexer
L	н	L	L	Clear

 $H \equiv high level, L \equiv low level$

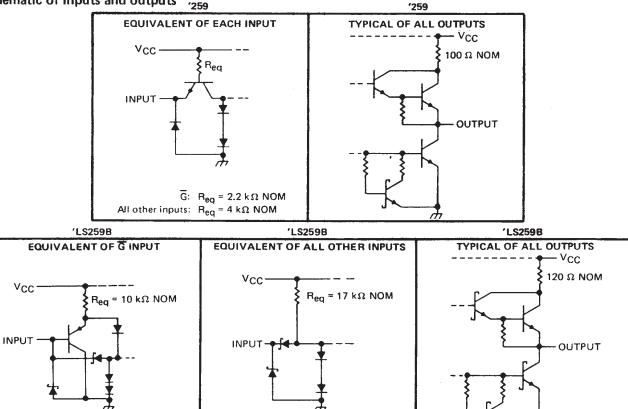
D = the level at the data input

 $\Omega_{i0} \equiv$ the level of Ω_i (i = 0, 1, ... 7, as appropriate) before the indicated steady-state input conditions were established.

schematic of inputs and outputs /259

LATCH SELECTION TABLE

SEL		IPUTS	LATCH
S2	S1	SO	ADDRESSED
L	L	L	0
L	Ł	Н	1
L	н	L	2
Ł	Н	H	3
н	L	L	4
н	L	н	5
н	н	L	6
н	н	н	7



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)		
Input voltage: SN54259, SN74259.		 5.5 V
Operating free-air temperature range:	SN54259, SN54LS259B	 -55° C to 125° C
	SN74259, SN74LS259B	 0°C to 70°C
Storage temperature range		 $-65^{\circ}C$ to $150^{\circ}C$

NOTE 1: Voltage values are with respect to network ground terminal.



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recommended operating conditions

		SN	SN54259			SN74259			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	V	
High-level output current, IOH				800			800	μA	
Low-level output current, IOL			16			16	mA		
Width of clear or enable pulse, t_W	-	15			15			ns	
Contra dima d	Data	151			151	•	-		
Setup time, t _{su}	Address	51			51	•		ns	
Hatdatara A	Data	0↑			01				
Hold time, th Address		20†			201			ns	
Operating free-air temperature, TA		55		125	0		70	°C	

The arrow indicates that the rising edge of the enable pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED		7507.00	NDITIONS [†]	S	N5425	•	SN74259			UNIT
	PARAMETER		TEST CU	NDITIONS'	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
VIH	High-level input volta	ge			2			2			V
VIL	Low-level input voltage	98					0.8			0.8	V
VIK	Input clamp voltage		V _{CC} = MIN,	I _I = 12 mA			-1.5			-1.5	V
∨он	High-level output volt	age	$V_{CC} = MIN,$ $V_{1L} = 0.8 V,$	V _{IH} = 2 V, I _{OH} =800 μA	2.4	3.4		2.4	3.4		v
VOL	Low-level output voltage		V _{CC} = MIN, V _{1L} = 0.8 V,	V _{IH} = 2 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	v
4	Input current at maxi	mum input voltage	V _{CC} = MAX,	V _I = 5.5 V			1			1	mA
Чн	High-level input current	G Other inputs	V _{CC} ≃ MAX,	∨ ₁ = 2.4 ∨			80 40			80 40	μΑ
ΊL	Low-level input current	G Other inputs	V _{CC} = MAX,	V _I = 0.4 V			3.2 1.6			-3.2 -1.6	mA
los	Short-circuit output c	urrent§	V _{CC} = MAX		-18		-57	-18		-57	mA
ICC	Supply current		V _{CC} = MAX,	See Note 2	1	60	90		60	90	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time,

NOTE 2: ICC is measured with the inputs grounded and the outputs open.

FROM TO UNIT PARAMETER **TEST CONDITIONS** MIN TYP MAX (INPUT) (OUTPUT) Any Q 16 25 ns CLR ^tPHL 14 24 **TPLH** ns Data Any Q $C_L \approx 15 \, pF$, 11 20 ^tPHL 15 28 $R_L = 400 \Omega$, ^tPLH ns Address Any Q 17 28 TPHL See Note 3 12 20 **TPLH** ns Ğ Any Q 11 20 TPHL

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$

tPLH = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



SN54LS259B, SN74LS259B 8-BIT ADDRESSABLE LATCHES

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recommended operating conditions

			SN	154LS2	59B	SN74LS259B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
юн	High-level output current			- 0.4			- 0.4	mA	
IOL	Low-level output current			4			8	mA	
	t _w Pulse duration CLR low	G low	17			17			
ťw		CLR low	10			10			្ពាន
		Data before G t	_ 20			20			
t _{su}	Set up time	Address before Gt	17			17			ns
		Address before GI	0			0			
		Data after G t	0			0			
th	Hold time	Address after G t	0			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]			SN54LS259B			SN	UNIT		
FANAMETEN				MIN	ТҮР	MAX	MIN	TYP	MAX	UNIT
Vik	$V_{CC} = MIN$, $I_{I} = -18 m/$	4				1,5			- 1.5	V
V _{OH}	$V_{CC} = MIN, V_{IH} = 2 V,$ $I_{OH} = -0.4 \text{ mA}$	VIL = MAX,		2,5	3.4		2.7	3.4		v
Ve	$V_{CC} = MIN, V_{IH} = 2 V,$		10L = 4 mA	<u> </u>	0.25	0.4		0.25	0.4	
VOL	VIL = MAX		IOL = 8 mA	1	-			0.35	0.5	1
II.	V _{CC} = MAX, V _I = 7 V					0.1			0.1	mA
Чн	V _{CC} = MAX, V ₁ = 2.7 V			1		20			20	μA
ΙL	V _{CC} = MAX, V _I = 0.4 V			I		- 0.4			- 0.4	mA
IOS§	V _{CC} = MAX			- 20		- 100	- 20		- 100	mA
Icc	V _{CC} = MAX, See Note 2			1	27	36		22	36	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions [‡]All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time, and duration short-circuit should not exceed one second.

NOTE 2: $\ensuremath{\mathsf{I_{CC}}}$ is measured with the inputs grounded and the outputs open.

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN TYP	мах	UNIT
^t PHL	CLR	Any Q		12	18	ns
^t PLH	Data	Any Q		19	30	ns
tPHL.	Udla	Any C	$C_{1} = 15 pF$, $R_{1} = 2 k\Omega$,	13	20	115
^t PLH	Address	Any Q	CL = 15 pF, RL = 2 kΩ, See Note 3	17	27	
^t PHL	Address	Any Q	See Note 5	14	20	ns
^t PLH	Ğ	Any Q		15	24	ns
^t PHL	3	Aug Q		15	24	115

tpLH = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

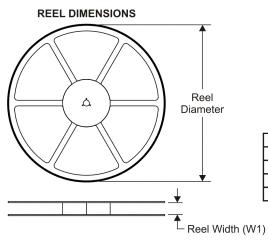


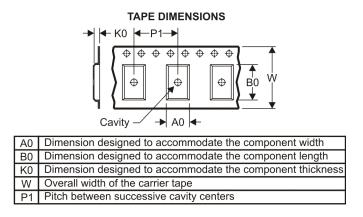
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS259BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

23-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS259BDR	SOIC	D	16	2500	333.2	345.9	28.6

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