



FEATURES

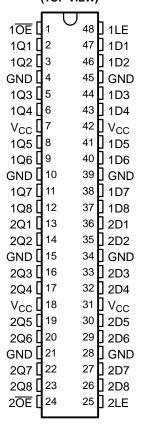
- Member of the Texas Instruments Widebus™
 Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.2 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Partial-Power-Down Mode Operation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 16-bit transparent D-type latch is designed for 1.65-V to 3.6-V $V_{\rm CC}$ operation.

The SN74LVC16373A is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



ORDERING INFORMATION

T _A	PACKAGE ⁽¹	1)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	FBGA – GRD	Tape and reel	SN74LVC16373AGRDR	LD373A
	FBGA – ZRD (Pb-free)	rape and reer	SN74LVC16373AZRDR	LD3/3A
	SSOP – DL	Tube	SN74LVC16373ADL	LVC16373A
	330P - DL	Tape and reel	SN74LVC16373ADLR	LVC10373A
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74LVC16373ADGGR	LVC16373A
-40 C to 65 C		Tape and reel	74LVC16373ADGGRG4	LVC10373A
	TVSOP – DGV	Tone and real	SN74LVC16373ADGVR	LD373A
	TVSOP - DGV	Tape and reel	74LVC16373ADGVRE4	LD3/3A
	VFBGA – GQL	Topo and real	SN74LVC16373AGQLR	LD373A
	VFBGA – ZQL (Pb-free)	Tape and reel	SN74LVC16373AZQLR	LDSISA

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SCAS755A-DECEMBER 2003-REVISED SEPTEMBER 2005



DESCRIPTION/ORDERING INFORMATION (CONTINUED)

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

GQL OR ZQL PACKAGE (TOP VIEW)

	_	1	2	3	4	5	6	
Α		$\overline{}$		()			$\overline{\circ}$	Ì
В		()	()	()	()	()	()	ı
С		()	()	()	()	()	()	ı
D		()	()	()	()	()	()	ı
Е		()	()			()	()	ı
F		()	()			()	()	ı
G		()	()	()	()	()	()	ı
Н		()	()	()	()	()	()	ı
J		()	()	()	()	()	()	ı
K		()	()	()	()	()	\circ	J

TERMINAL ASSIGNMENTS⁽¹⁾ (56-Ball GQL/ZQL Package)

	1	2	3	4	5	6			
Α	1 OE	NC	NC	NC	NC	1LE			
В	1Q2	1Q1	GND GND		1D1	1D2			
С	1Q4	1Q3	V _{CC}	V _{CC}	1D3	1D4			
D	1Q6	1Q5	GND	GND	1D5	1D6			
Е	1Q8	1Q7			1D7	1D8			
F	2Q1	2Q2			2D2	2D1			
G	2Q3	2Q4	GND	GND	2D4	2D3			
Н	2Q5	2Q6	V _{CC}	V _{CC}	2D6	2D5			
J	2Q7	2Q8	GND	GND	2D8	2D7			
K	2 OE	NC	NC	NC	NC	2LE			

(1) NC - No internal connection

GRD OR ZRD PACKAGE (TOP VIEW)

	_	1	2	3	4	[′] 5	6	_
Α		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	_
В		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	
С		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	
D		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	
E		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	
F		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	
G		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	
н		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	
J		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	
	\							_

TERMINAL ASSIGNMENTS⁽¹⁾ (54-Ball GRD/ZRD Package)

	1	2	3	4	5	6		
Α	1Q1	NC	1 OE	1LE	NC	1D1		
В	1Q3	1Q2	NC	NC	1D2	1D3		
С	1Q5	1Q4	V _{CC}	V _{CC}	1D4	1D5		
D	1Q7	1Q6	GND	GND	1D6	1D7		
E	2Q1	1Q8	GND	GND	1D8	2D1		
F	2Q3	2Q2	GND	GND	2D2	2D3		
G	2Q5	2Q4	V _{CC}	V _{CC}	2D4	2D5		
Н	2Q7	2Q6	NC	NC	2D6	2D7		
J	2Q8	NC	2 OE	2LE	NC	2D8		

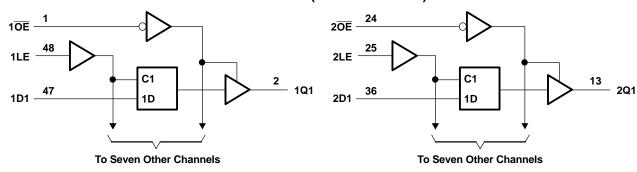
(1) NC - No internal connection



FUNCTION TABLE

I	NPUTS	NPUTS OUTPUT			
ŌĒ	LE	D	Q		
L	Н	Н	Н		
L	Н	L	L		
L	L	X	Q_0		
Н	Χ	Χ	Z		

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DGV, and DL packages.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range ⁽²⁾		-0.5	6.5	V
Vo	Voltage range applied to any output in the h	nigh-impedance or power-off state (2)	-0.5	6.5	V
Vo	Voltage range applied to any output in the h	high or low state ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current				
	Continuous current through each V _{CC} or GN	ND		±100	mA
		DGG package		70	
		DGV package		58	
θ_{JA}	Package thermal impedance (4)	DL package		63	°C/W
	-	GQL/ZQL package		42	
		GRD/ZRD package		36	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC16373A 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS755A-DECEMBER 2003-REVISED SEPTEMBER 2005

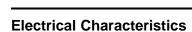


Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V	Cupply voltage	Operating	1.65	3.6	V
V_{CC}	Supply voltage	Data retention only	1.5		V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
VI	Input voltage		0	5.5	V
\ /	Output voltage	High or low state	0	V _{CC}	V
V_O		High-impedance state	0	5.5	V
		V _{CC} = 1.65 V		-4	
	High lovel output ourrent	V _{CC} = 2.3 V		-8	A
I _{OH}	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
	Low lovel output ourrent	V _{CC} = 2.3 V		8	A
I _{OL}	Low-level output current	V _{CC} = 2.7 V	V _{CC} = 2.7 V		mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SCAS755A-DECEMBER 2003-REVISED SEPTEMBER 2005



TRUMENTS

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over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{cc}	MIN	TYP ⁽¹⁾ MAX	UNIT
	$I_{OH} = -100 \mu A$		1.65 V to 3.6 V	$V_{CC} - 0.2$		
	$I_{OH} = -4 \text{ mA}$		1.65 V	1.2		
\/	$I_{OH} = -8 \text{ mA}$		2.3 V	1.7		V
V _{OH}	I - 12 mA	$I_{OH} = -12 \text{ mA}$				V
	1 _{OH} = -12 IIIA					
	$I_{OH} = -24 \text{ mA}$	$I_{OH} = -24 \text{ mA}$				
	_L = 100 μA		1.65 V to 3.6 V		0.2	
	I _{OL} = 4 mA		1.65 V		0.45	
V _{OL}	I _{OL} = 8 mA	2.3 V		0.7	V	
	I _{OL} = 12 mA	2.7 V		0.4		
	I _{OL} = 24 mA	3 V		0.55		
I _I	V _I = 0 to 5.5 V		3.6 V		±5	μΑ
I _{off}	V_I or $V_O = 5.5 \text{ V}$		0		±10	μΑ
I _{OZ}	V _O = 0 to 5.5 V		3.6 V		±10	μΑ
1	V _I = V _{CC} or GND	1 - 0	3.6 V		20	^
I _{cc}	$3.6 \text{ V} \le \text{V}_1 \le 5.5 \text{ V}^{(2)}$	I _O = 0	3.6 V	20		μΑ
Δl _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500		μΑ
C _i	$V_I = V_{CC}$ or GND		3.3 V		5	pF
Co	V _O = V _{CC} or GND		3.3 V		6.5	pF

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. (2) This applies in the disabled state only.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V_{CC} = 3.3 V \pm 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	1.6		1.2		1.7		1.7		ns
t _h	Hold time, data after LE↓	1		1.1		1.2		1.2		ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V_{CC} = 1.8 V \pm 0.15 V		V_{CC} = 2.5 V \pm 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	D	Q	1.5	6.4	1	4.2	1	4.9	1.6	4.2	
t _{pd}	LE		1.5	7.1	1	4.8	1	5.3	2.1	4.6	ns
t _{en}	ŌĒ	Q	1.5	6.7	1	4.7	1	5.7	1.3	4.7	ns
t _{dis}	ŌĒ	Q	1.5	8.4	1	5	1	6.3	2.5	5.9	ns

SN74LVC16373A 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS755A-DECEMBER 2003-REVISED SEPTEMBER 2005



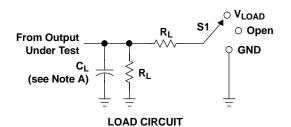
Operating Characteristics

 $T_A = 25^{\circ}C$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
Power dissipation capacitance		Outputs enabled	f = 10 MHz	32	35	39	pF	
C _{pd}	per latch	Outputs disabled	1 = 10 101112	4	4	6	þΓ	

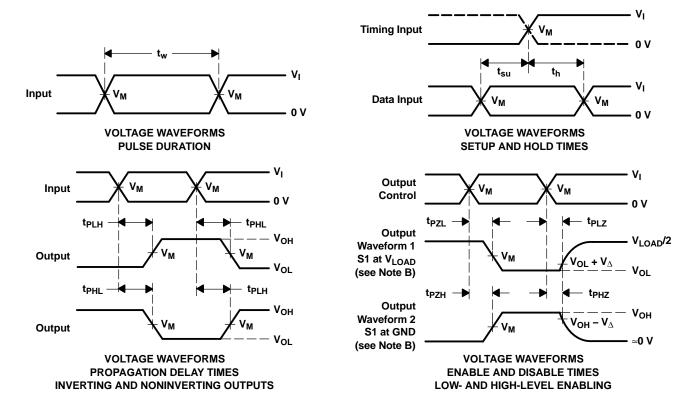


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

INPUTS		.,	V	_		V	
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R_L	$oldsymbol{V}_{\Delta}$
1.8 V \pm 0.15 V	v _{cc}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \ \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



3-May-2012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74LVC16373ADGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC16373ADGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC16373ADGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC16373ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC16373ADGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC16373ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC16373ADLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC16373ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC16373ADLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC16373AGQLR	LIFEBUY	BGA MICROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM	
SN74LVC16373AZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
SN74LVC16373AZRDR	ACTIVE	BGA MICROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



PACKAGE OPTION ADDENDUM

3-May-2012

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC16373A:

Enhanced Product: SN74LVC16373A-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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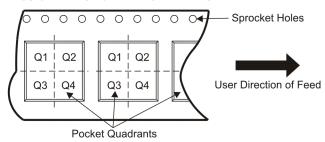
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	_	Package		SPQ	Reel	Reel	A0	B0	K0	P1	W (mm)	Pin1
	Туре	Drawing			Diameter (mm)	Width W1 (mm)	(mm)	(mm)	(mm)	(mm)	(mm)	Quadrant
SN74LVC16373ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74LVC16373ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVC16373ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVC16373AGQLR	BGA MI CROSTA R JUNI OR	GQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1
SN74LVC16373AZQLR	BGA MI CROSTA R JUNI OR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1
SN74LVC16373AZRDR	BGA MI CROSTA R JUNI OR	ZRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1

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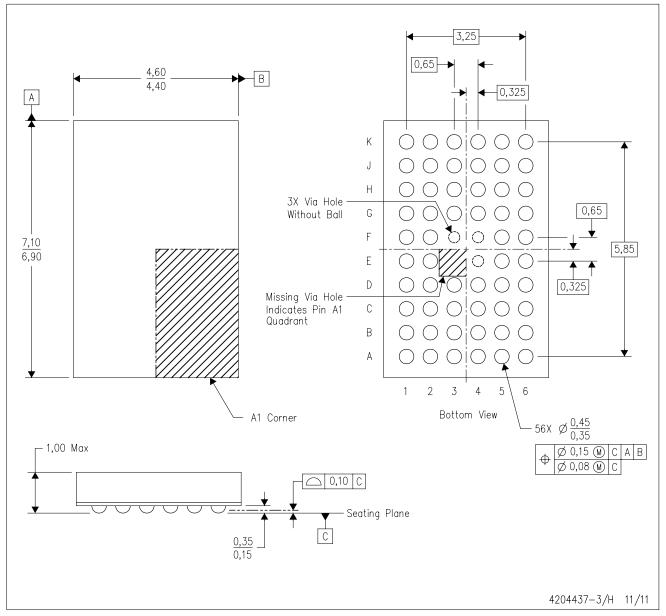


*All dimensions are nominal

7 til dimensions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC16373ADGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74LVC16373ADGVR	TVSOP	DGV	48	2000	346.0	346.0	33.0
SN74LVC16373ADLR	SSOP	DL	48	1000	346.0	346.0	49.0
SN74LVC16373AGQLR	BGA MICROSTAR JUNIOR	GQL	56	1000	333.2	345.9	28.6
SN74LVC16373AZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6
SN74LVC16373AZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	333.2	345.9	28.6

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

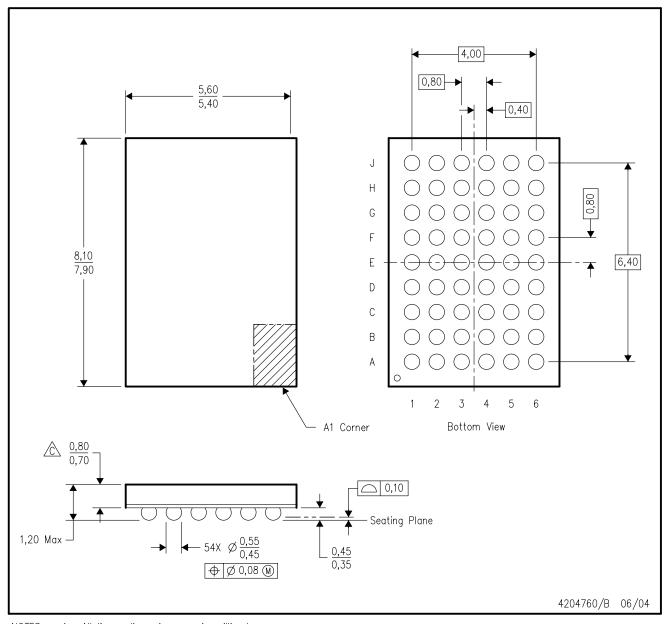
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

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ZRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY



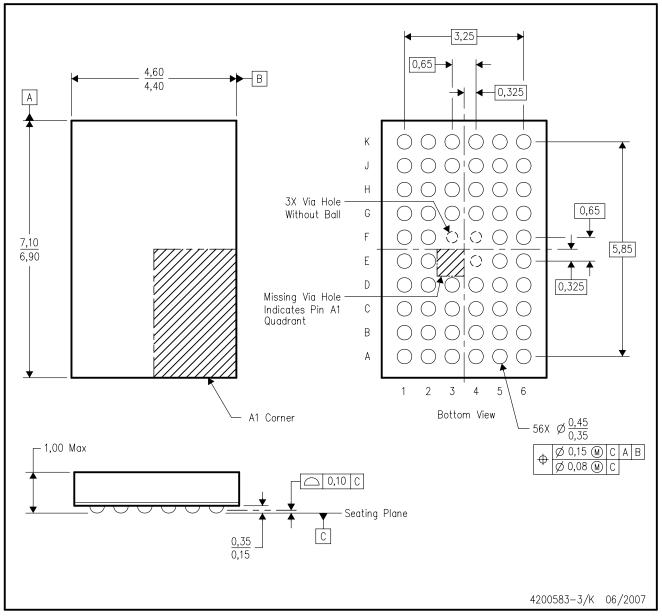
 $\hbox{NOTES:} \quad \hbox{A. All linear dimensions are in millimeters.}$

- B. This drawing is subject to change without notice.
- Falls within JEDEC MO-205 variation DD.
- D. This package is lead—free. Refer to the 54 GRD package (drawing 4204759) for tin—lead (SnPb).



GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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