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- Low $r_{DS(on)} \dots 5 \Omega$ Typical
- Avalanche Energy . . . 30 mJ
- Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current
- 500-mA Typical Current-Limiting Capability
- Output Clamp Voltage . . . 50 V
- Four Distinct Function Modes
- Low Power Consumption

description

This power logic 8-bit addressable latch controls open-drain DMOS-transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multifunctional device capable of storing single-line data in eight addressable latches and 3-to-8 decoder or demultiplexer with active-low DMOS outputs.

Four distinct modes of operation are selectable by controlling the clear (\overline{CLR}) and enable (\overline{G}) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable \overline{G} should be held high (inactive) while the address lines are changing. In the 3-to-8 decoding or demultiplexing mode, the addressed output is inverted with respect to the D input and all other

DW OR N PACKAGE (TOP VIEW)							
NC [1	20] NC				
V _{CC} [2	19] CLR				
S0 [3	18] D				
DRAIN0 [4	17] DRAIN7				
DRAIN1 [5	16] DRAIN6				
DRAIN2 [6	15] DRAIN5				
DRAIN3 [7	14] DRAIN4				
S1 [8	13] G				
GND]	9	12] S2				
GND [9	12	S2				
GND [10	11	GND				

NC - No internal connection

FUNCTION TABLE

INF	PUT	s	OUTPUT OF ADDRESSED	EACH OTHER	FUNCTION				
CLR	G	D	DRAIN	DRAIN	FUNCTION				
H H	L L	H L	L H	Q _{io} Q _{io}	Addressable Latch				
н	Н	Х	Q _{io}	Q _{io}	Memory				
L	L L	H L	L H	H H	8-Line Demultiplexer				
L	Н	Х	Н	Н	Clear				

LATCH SELECTION TABLE

SELE		DRAIN	
S2	S 1	S0	ADDRESSED
L	L	L	0
L	L	Н	1
L	Н	L	2
L	Н	н	3
Н	L	L	4
Н	L	Н	5
Н	Н	L	6
Н	Н	Н	7

H = high level, L = low level

outputs are off. In the clear mode, all outputs are off and unaffected by the address and data inputs. When data is low for a given output, the DMOS-transistor output is off. When data is high, the DMOS-transistor output has sink-current capability.

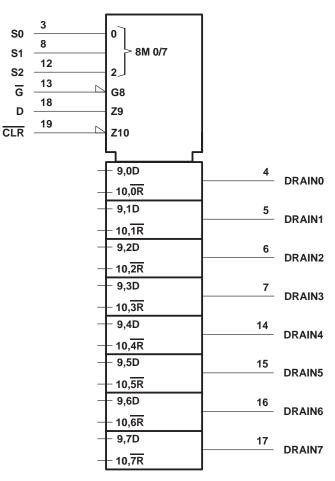
Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at $T_C = 25$ °C. The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B259 is characterized for operation over the operating case temperature range of -40°C to 125°C.



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logic symbol[†]

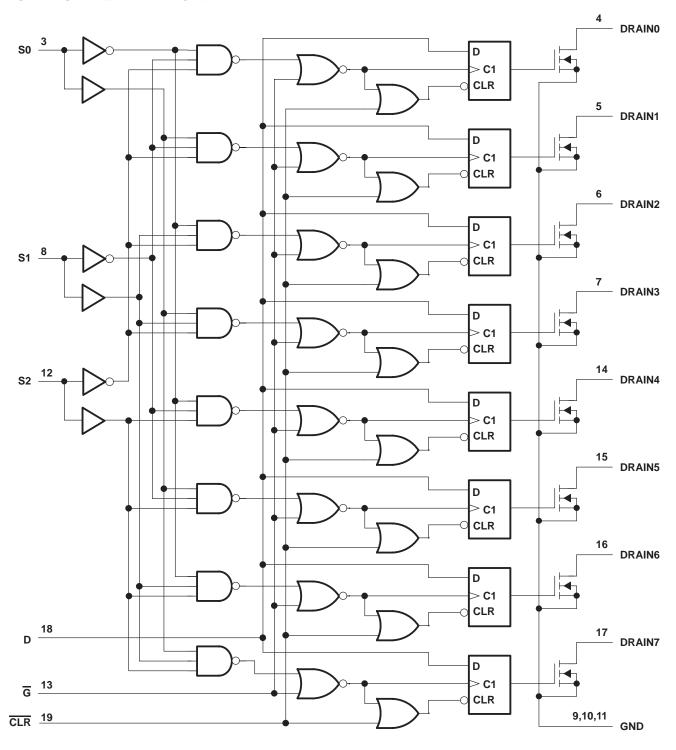


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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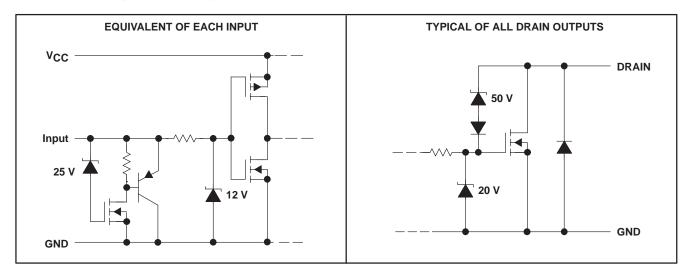
logic diagram (positive logic)





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schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted) $\!\!\!\!^\dagger$

Logic supply voltage, V_{CC} (see Note 1) Logic input voltage range, V_1 Power DMOS drain-to-source voltage, V_{DS} (see Note 2) Continuous source-to-drain diode anode current Pulsed source-to-drain diode anode current (see Note 3) Pulsed drain current, each output, all outputs on, I_D , $T_C = 25^{\circ}C$ (see Note 3) Continuous drain current, each output, all outputs on, I_D , $T_C = 25^{\circ}C$ (see Note 3) Continuous drain current, each output, all outputs on, I_D , $T_C = 25^{\circ}C$ Peak drain current single output, I_{DM} , $T_C = 25^{\circ}C$ (see Note 3) Single-pulse avalanche energy, E_{AS} (see Figure 4) Avalanche current, I_{AS} (see Note 4) Continuous total dissipation Operating virtual junction temperature range, T_J Operating case temperature range, T_C Storage temperature range	-0.3 V to 7 V
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

2. Each power DMOS source is internally connected to GND.

3. Pulse duration \leq 100 µs and duty cycle \leq 2%.

4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 200 mH, I_{AS} = 0.5 A (see Figure 4).

	DISSIPATION RATING TABLE								
PACKAGE	T _C ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _C = 25°C	T _C = 125°C POWER RATING						
DW	1389 mW	11.1 mW/°C	278 mW						
N	1050 mW	10.5 mW/°C	263 mW						



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recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V _{CC}	4.5	5.5	V
High-level input voltage, VIH	0.85 V _{CC}		V
Low-level input voltage, VIL		0.15 V _{CC}	V
Pulsed drain output current, $T_C = 25^{\circ}C$, $V_{CC} = 5 V$ (see Notes 3 and 5)	-500	500	mA
Setup time, D high before \overline{G} , t _{SU} (see Figure 2)	20		ns
Hold time, D high after \overline{G} , t _h (see Figure 2)	20		ns
Pulse duration, t _W (see Figure 2)	40		ns
Operating case temperature, T _C	-40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

	PARAMETER		TEST CONDITIO	DNS	MIN	TYP	MAX	UNIT
V _{(BR)DSX}	Drain-to-source breakdown voltage	I _D = 1 mA			50			V
V _{SD}	Source-to-drain diode forward voltage	I _F = 100 mA				0.85	1	V
IIН	High-level input current	V _{CC} = 5.5 V,	$V_I = V_{CC}$				1	μA
۱ _{IL}	Low-level input current	V _{CC} = 5.5 V,	$V_{I} = 0$				-1	μA
laa			All outputs off			20	100	μA
lcc	Logic supply current	V _{CC} = 5.5 V	All outputs on		150	300	μη	
IN	Nominal current	V _{DS(on)} = 0.5 V, See Notes 5, 6, a		T _C = 85°C,		90		mA
1	Off-state drain current	V _{DS} = 40 V,	V _{CC} = 5.5 V			0.1	5	۵
DSX	On-state drain current	V _{DS} = 40 V,	V _{CC} = 5.5 V,	T _C = 125°C		0.15	8	μA
		I _D = 100 mA,	V _{CC} = 4.5 V			4.2	5.7	
^r DS(on)	Static drain-to-source on-state resistance	I _D = 100 mA, T _C = 125°C	V _{CC} = 4.5 V,	See Notes 5 and 6 and Figures 6 and 7		6.8	9.5	Ω
		I _D = 350 mA,	V _{CC} = 4.5 V	1		5.5	8	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output from D	150				ns
^t PHL	Propagation delay time, high-to-low-level output from D	C _L = 30 pF, I _D = 100 mA,		90		ns
tr	Rise time, drain output	See Figures 1, 2, and 8		200		ns
tf	Fall time, drain output			200		ns
ta	Reverse-recovery-current rise time	I _F = 100 mA, di/dt = 20 A/μs,		100		
t _{rr}	Reverse-recovery time	See Notes 5 and 6 and Figure 3		300		ns

NOTES: 3. Pulse duration \leq 100 μ s and duty cycle \leq 2%.

5. Technique should limit $T_J - T_C$ to 10°C maximum.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

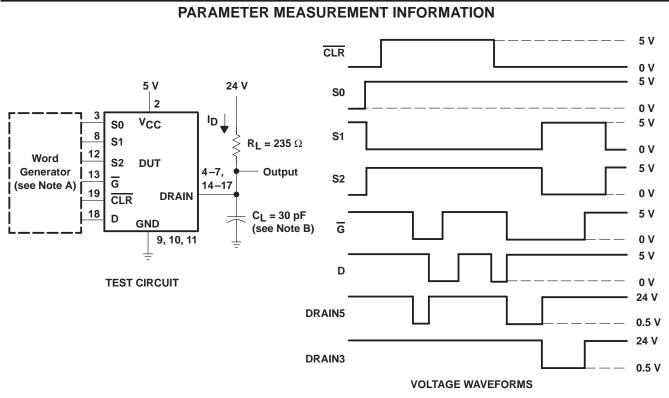
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at $T_C = 85^{\circ}C$.



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thermal resistance

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT	
B	R _{0JA} Thermal resistance junction-to-ambient	DW package	All 9 outputs with aqual power		90	0CAN
R _{0JA}		N package	All 8 outputs with equal power		95	°C/W

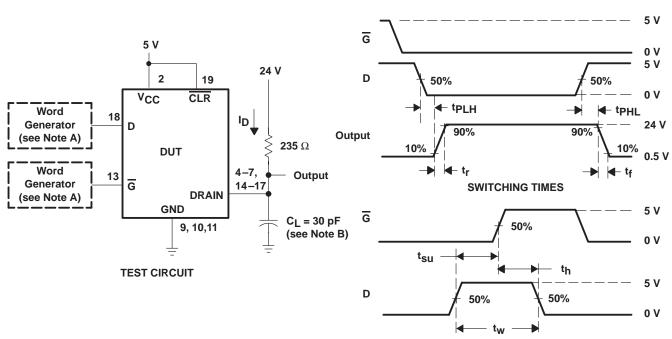


- NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50 \ \Omega$.
 - B. C_{L} includes probe and jig capacitance.

Figure 1. Resistive-Load Test Circuit and Voltage Waveforms



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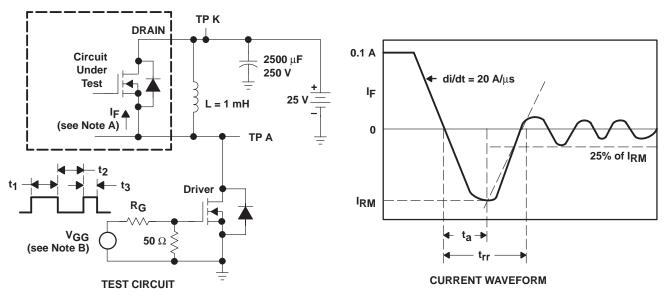


PARAMETER MEASUREMENT INFORMATION

INPUT SETUP AND HOLD WAVEFORMS

- NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50 \ \Omega$.
 - B. $\tilde{C_L}$ includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

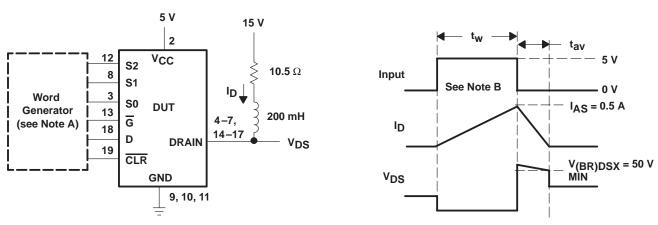


- NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
 - B. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/ μ s. A V_{GG} double-pulse train is used to set I_F = 0.1 A, where t₁ = 10 μ s, t₂ = 7 μ s, and t₃ = 3 μ s.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode



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PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_f \le 10 \text{ ns}, t_f \le 10 \text{ ns}, Z_O = 50 \Omega$. B. Input pulse duration, t_W , is increased until peak current $I_{AS} = 0.5 \text{ A}$. Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30 \text{ mJ}$.



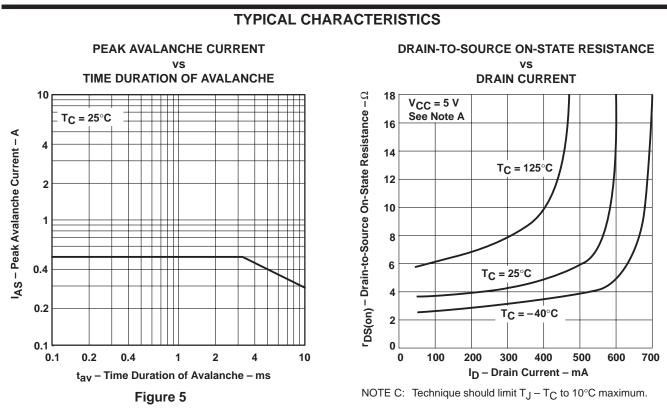
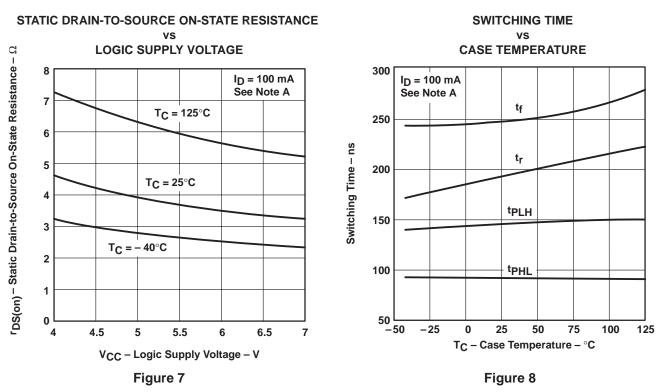


Figure 6



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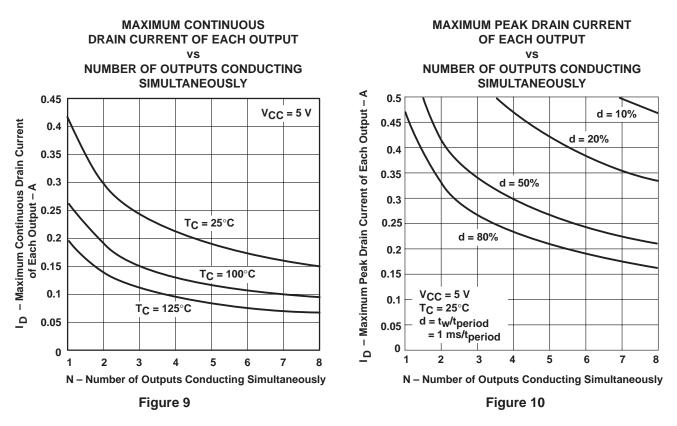


TYPICAL CHARACTERISTICS

NOTE D: Technique should limit $T_J - T_C$ to 10°C maximum.



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THERMAL INFORMATION





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TPIC6B259DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPIC6B259DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPIC6B259DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPIC6B259DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPIC6B259N	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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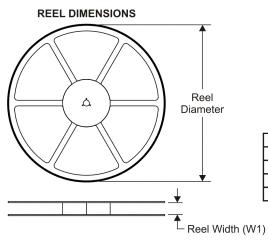
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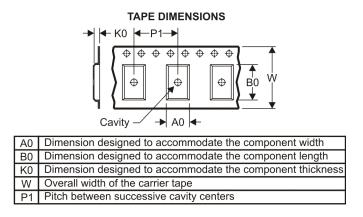
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6B259DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

9-Dec-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6B259DWR	SOIC	DW	20	2000	346.0	346.0	41.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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