- Low  $r_{DS(on)} \dots 1.3 \Omega$  Typ
- Avalanche Energy . . . 75 mJ
- Eight Power DMOS Transistor Outputs of 250-mA Continuous Current
- 1.5-A Pulsed Current Per Output
- Output Clamp Voltage up to 45 V
- Low Power Consumption

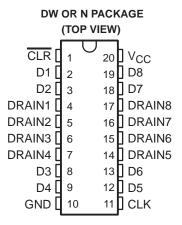
### description

The TPIC6273 is a monolithic high-voltage high-current power logic octal D-type latch with DMOS transistor outputs designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

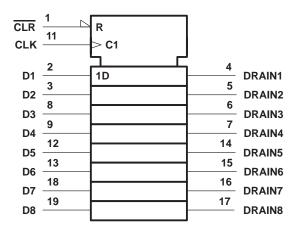
The TPIC6273 contains eight positive-edgetriggered D-type flip-flops with a direct clear input. Each flip-flop features an open-drain power DMOS transistor output.

When clear (CLR) is high, information at the D inputs meeting the setup time requirements is transferred to the DRAIN outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input (CLK) is at either the high or low level, the D input signal has no effect at the output. An asynchronous CLR is provided to turn all eight DMOS-transistor outputs off.

The TPIC6273 is characterized for operation over the operating case temperature range of  $-40^{\circ}$ C to 125°C.



## logic symbol†



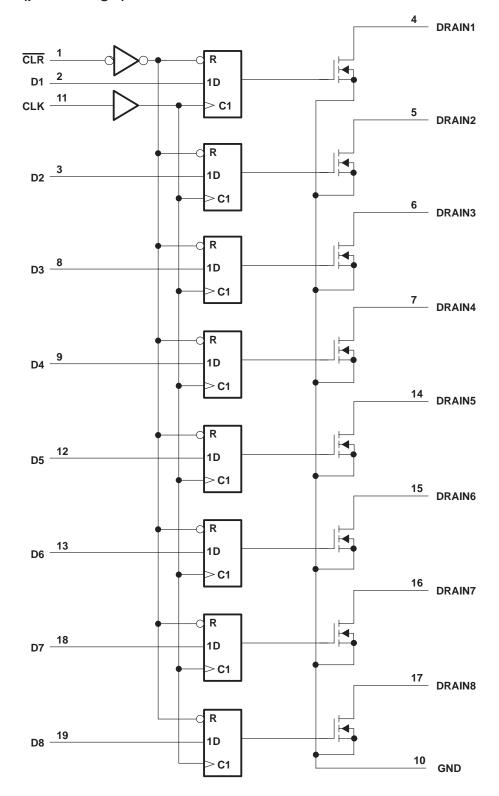
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

# FUNCTION TABLE (each channel)

	INPUTS		OUTPUT
CLR	CLK	D	DRAIN
L	Χ	X	Н
Н	$\uparrow$	Н	L
Н	$\uparrow$	L	Н
Н	L	X	Latched

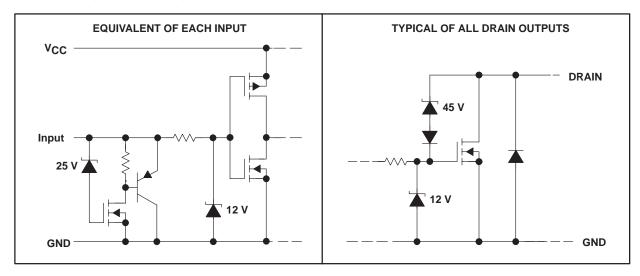
H = high level, L = low level, X = irrelevant

# logic diagram (positive logic)





### schematic of inputs and outputs



# absolute maximum ratings over recommended operating case temperature range (unless otherwise noted) $\!\!\!\!^{\dagger}$

Logic supply voltage, V <sub>CC</sub> (see Note 1)	7 V
Logic input voltage range, V <sub>I</sub>	0.3 V to 7 V
Power DMOS drain-to-source voltage, V <sub>DS</sub> (see Note 2)	45 V
Continuous source-drain diode anode current	
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, $I_{Dn}$ , $T_A = 25$ °C (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, $I_{Dn}$ , $T_A = 25$ °C	
Peak drain current single output, I <sub>DM</sub> , T <sub>A</sub> = 25°C (see Note 3)	
Single-pulse avalanche energy, E <sub>AS</sub> (see Figure 4)	
Avalanche current, I <sub>AS</sub> (see Note 4)	1 A
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T <sub>J</sub>	
Storage temperature range, T <sub>stq</sub>	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

- 2. Each power DMOS source is internally connected to GND.
- 3. Pulse duration  $\leq$  100  $\mu$ s, duty cycle  $\leq$  2%
- 4. DRAIN supply voltage = 15 V, starting junction temperature ( $T_{JS}$ ) = 25°C, L = 100 mH,  $I_{AS}$  = 1 A (see Figure 4).

### **DISSIPATION RATING TABLE**

PACKAGE	$T_{\mbox{\scriptsize A}} \le 25^{\circ}\mbox{\scriptsize C}$ POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW



SLIS011A - APRIL 1992 - REVISED OCTOBER 1995

### recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V <sub>CC</sub>	4.5	5.5	V
High-level input voltage, VIH	0.85 V <sub>CC</sub>		V
Low-level input voltage, V <sub>IL</sub>		0.15 V <sub>CC</sub>	V
Pulsed drain output current, T <sub>C</sub> = 25°C, V <sub>CC</sub> = 5 V (see Notes 3 and 5)	-1.8	1.5	Α
Setup time, D high before CLK↑, t <sub>SU</sub> (see Figure 2)	10		ns
Hold time, D high after CLK↑, th (see Figure 2)	15		ns
Pulse duration, t <sub>W</sub> (see Figure 2)	25		ns
Operating case temperature, T <sub>C</sub>	-40	125	°C

# electrical characteristics, $V_{CC}$ = 5 V, $T_{C}$ = 25°C (unless otherwise noted)

	PARAMETER		TEST COND	ITIONS	MIN	TYP	MAX	UNIT
V(BR)DSX	Drain-source breakdown voltage	$I_D = 1 \text{ mA}$			45			V
$V_{SD}$	Source-drain diode forward voltage	$I_F = 250 \text{ mA},$	See Note 3			0.85	1	V
lн	High-level input current	$V_{CC} = 5.5 \text{ V},$	$V_I = V_{CC}$				1	μΑ
I <sub>IL</sub>	Low-level input current	$V_{CC} = 5.5 V$ ,	V <sub>I</sub> = 0				-1	μΑ
Icc	Logic supply current	I <sub>O</sub> = 0,	All inputs low			15	100	μΑ
IN	Nominal current	$V_{DS(on)} = 0.5$ $I_{N} = I_{D}$	5 V, T <sub>C</sub> = 85°C	See Notes 5, 6, and 7		250		mA
la av	Off state drain surrent	V <sub>DS</sub> = 40 V				0.05	1	^
IDSX	Off-state drain current	$V_{DS} = 40 \text{ V},$	T <sub>C</sub> = 125°C			0.15	5	μΑ
		$I_D = 250 \text{ mA},$	V <sub>CC</sub> = 4.5 V			1.3	2	
rDS(on)	Static drain-source on-state resistance	I <sub>D</sub> = 250 mA, V <sub>CC</sub> = 4.5 V	T <sub>C</sub> = 125°C,	See Notes 5 and 6 and Figures 8 and 9		2	3.2	Ω
		$I_D = 500 \text{ mA},$	V <sub>CC</sub> = 4.5 V	]		1.3	2	

# switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_{C} = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output from CLK			625		ns
tPHL	Propagation delay time, high-to-low-level output from CLK	$C_L = 30 \text{ pF}, \qquad I_D = 250 \text{ mA},$		150		ns
t <sub>r</sub>	Rise time, drain output	See Figures 1, 2, and 10		675		ns
tf	Fall time, drain output			400		ns
ta	Reverse-recovery-current rise time	I <sub>F</sub> = 250 mA, di/dt = 20 A/μs,		100		no
t <sub>rr</sub>	Reverse-recovery time	See Notes 5 and 6 and Figure 3		300		ns

NOTES: 3. Pulse duration  $\leq$  100  $\mu$ s, duty cycle  $\leq$  2%

- 5. Technique should limit  $T_J T_C$  to 10°C maximum.
- 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
- 7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at  $T_C = 85^{\circ}C$ .

#### thermal resistance

	PARAMETER	TEST CONDITIONS	MIN M	AX	UNIT	
D	Thermal resistance, junction-to-ambient	DW package  All 8 outputs with equal power			111	°C/W
$R_{\theta JA}$	merma resistance, junction-to-ambient	N package	All 6 outputs with equal power		108	C/VV



#### PARAMETER MEASUREMENT INFORMATION

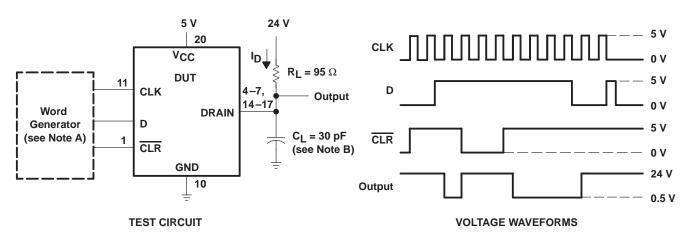


Figure 1. Resistive Load Normal Operation

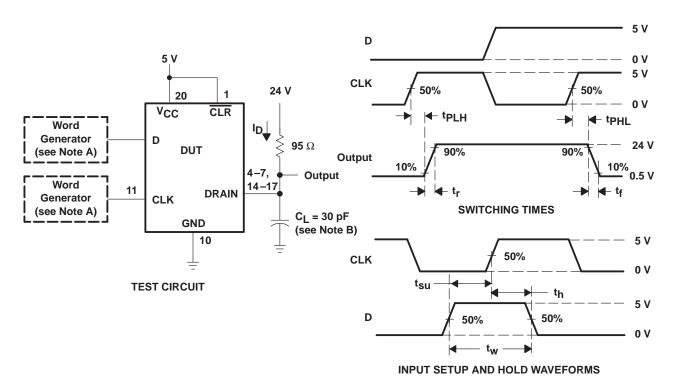
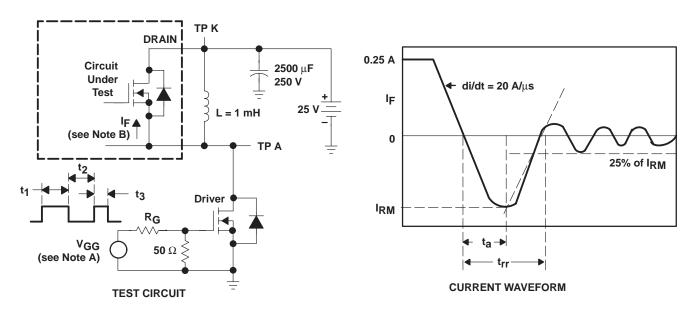


Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. The word generator has the following characteristics:  $t_{\Gamma} \le 10$  ns,  $t_{\phi} = 10$  ns,  $t_{\phi} =$ 

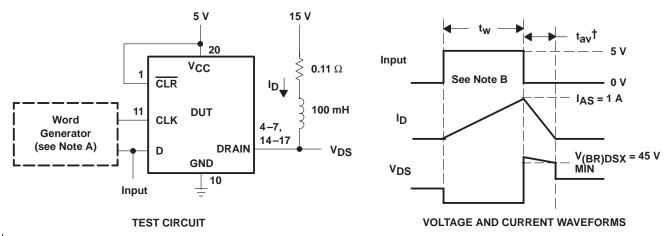
B. C<sub>L</sub> includes probe and jig capacitance.

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The V<sub>GG</sub> amplitude and R<sub>G</sub> are adjusted for di/dt = 20 A/ $\mu$ s. A V<sub>GG</sub> double-pulse train is used to set I<sub>F</sub> = 0.25 A, where t<sub>1</sub> = 10  $\mu$ s, t<sub>2</sub> = 7  $\mu$ s, and t<sub>3</sub> = 3  $\mu$ s.
  - B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



† Non-JEDEC symbol for avalanche ftime.

NOTES: A. The word generator A has the following characteristics:  $t_{\Gamma} \leq$  10 ns,  $t_{f} \leq$  10 ns,  $Z_{O}$  = 50  $\Omega$ .

B. Input pulse duration,  $t_W$ , is increased until peak current  $I_{AS} = 1$  A. Energy test is defined as  $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 75$  mJ, where  $t_{av}$  = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms



### **TYPICAL CHARACTERISTICS**

# **PEAK AVALANCHE CURRENT** TIME DURATION OF AVALANCHE 10 $T_{JS} = 25^{\circ}C$ IAS - Peak Avalanche Current - A 2 1 0.4 0.2 0.1 0.1 0.2 1 2 4 10 tav - Time Duration of Avalanche - ms

Figure 5

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING

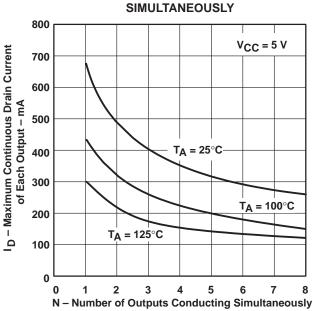


Figure 6

# MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT

# NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

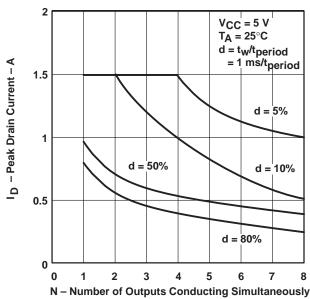
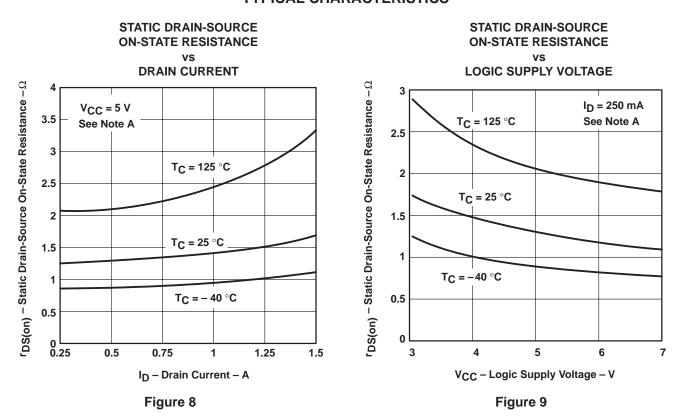
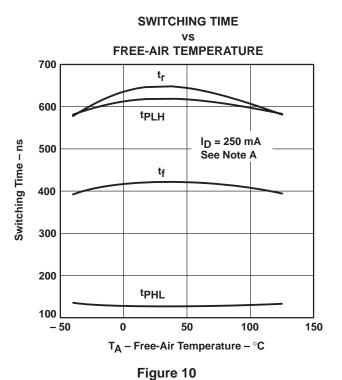


Figure 7



### **TYPICAL CHARACTERISTICS**





NOTE A: Technique should limit  $T_J - T_C$  to 10°C maximum.







30-Apr-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPIC6273DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPIC6273DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPIC6273DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPIC6273DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPIC6273N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

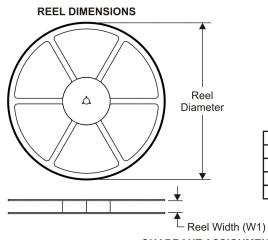
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# **PACKAGE MATERIALS INFORMATION**

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1

www.ti.com 9-Dec-2010



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6273DWR	SOIC	DW	20	2000	346.0	346.0	41.0

# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

### PLASTIC SMALL OUTLINE



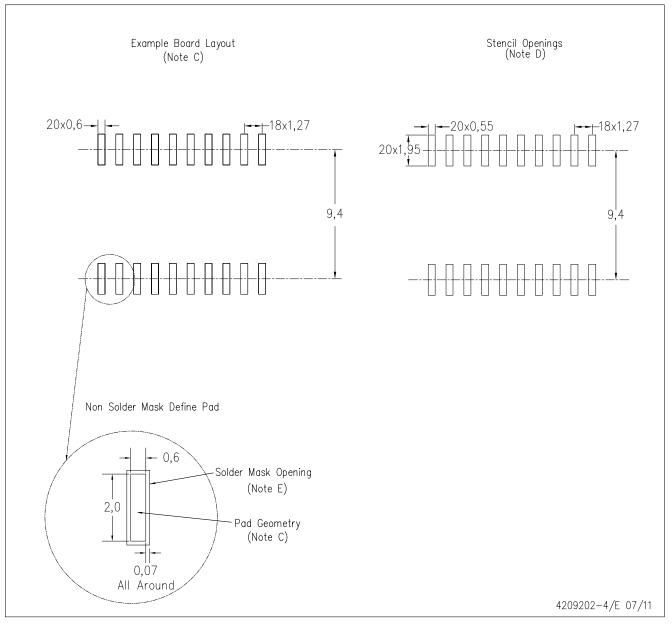
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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