#### The SN54165 and SN74165 devices are obsolete and are no longer supplied.

- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- Parallel-to-Serial Data Conversion

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'165	26 MHz	210 mW
'LS165A	35 MHz	90 mW

#### description

The '165 and 'LS165A are 8-bit serial shift registers that shift the data in the direction of QA toward Q<sub>H</sub> when clocked. Parallel-in access to each stage is made available by eight individual, direct data inputs that are enabled by a low level at the shift/load (SH/LD) input. These registers also feature gated clock (CLK) inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a two-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with SH/LD high enables the other clock input. Clock inhibit (CLK INH) should be changed to the high level only while CLK is high. Parallel loading is inhibited as long as SH/LD is high. Data at the parallel inputs are loaded directly into the register while SH/LD is low, independently of the levels of CLK, CLK INH, or serial (SER) inputs.

### SN54165, SN54LS165A, SN74165, SN74LS165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

SDLS062D - OCTOBER 1976 - REVISED FEBRUARY 2002



NC - No internal connection

ð ž



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



Copyright © 2002, Texas Instruments Incorporated On products compliant to MIL-PRF-38535, all parameters are tested less otherwise noted. On all other products. production processing does not necessarily include testing of all part

#### SDLS062D - OCTOBER 1976 - REVISED FEBRUARY 2002

## The SN54165 and SN74165 devices are obsolete and are no longer supplied.

TA	PAC	KAGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74LS165AN	SN74LS165AN
0°C to 70°C		Tube	SN74LS165AD	
0010700	3010 - 0	Tape and reel	SN74LS165ADR	LSTOSA
	SOP – NS	Tape and reel	SN74LS165ANSR	74LS165A
		Tube	SN54LS165AJ	SN54LS165AJ
55°C to 125°C	CDIP – J	Tube	SNJ54LS165AJ	SNJ54LS165AJ
	CFP – W	Tube	SNJ54LS165AW	SNJ54LS165AW
	LCCC – FK	Tube	SNJ54LS165AFK	SNJ54LS165AFK

#### **ORDERING INFORMATION**

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

			1 0110		_		
		INPUT	6	-	INTE OUT	RNAL PUTS	OUTPUT
SH/LD	CLK INH	CLK	SER	PARALLEL A H	$\overline{Q}_{A}$	$\overline{Q}_{B}$	QH
L	Х	Х	Х	ah	а	b	h
Н	L	L	Х	Х	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>
Н	L	$\uparrow$	Н	х	н	Q <sub>An</sub>	Q <sub>Gn</sub>
Н	L	$\uparrow$	L	Х	L	Q <sub>An</sub>	Q <sub>Gn</sub>
н	н	Х	Х	х	QAO	QBU	Quo

#### FUNCTION TABLE



# The SN54165 and SN74165 devices are obsolete and are no longer supplied.

## SN54165, SN54LS165A, SN74165, SN74LS165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

SDLS062D - OCTOBER 1976 - REVISED FEBRUARY 2002

#### schematics of inputs and outputs









SDLS062D - OCTOBER 1976 - REVISED FEBRUARY 2002

#### logic diagram (positive logic)



Pin numbers shown are for D, J, N, NS, and W packages.







SDLS062D - OCTOBER 1976 - REVISED FEBRUARY 2002

#### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage, V	CC (see Note 1)		 
Input voltage, VI:	SN54165, SN74165		 5.5 V
	SN54LS165A, SN74LS165/	Α	 
Interemitter voltag	e (see Note 2)		 5.5 V
Package thermal i	mpedance $\theta_{JA}$ (see Note 3):	D package	 
		N package	 67°C/W
		NS package	 64°C/W
Storage temperate	ure range, T <sub>stg</sub>		 –65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '165 to the SH/LD input in conjunction with the CLK INH input.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions

			SN54165		w,	SN74165		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
ЮН	High-level output current			-800			-800	μΑ
IOL	Low-level output current			16			16	mA
fclock	Clock frequency	0		20	0		20	MHz
<sup>t</sup> w(clock)	Width of clock input pulse	25			25			ns
<sup>t</sup> w(load)	Width of load input pulse	15			15			ns
t <sub>su</sub>	Clock-enable setup time (see Figure 1)	30			30			ns
t <sub>su</sub>	Parallel input setup time (see Figure 1)	10			10			ns
t <sub>su</sub>	Serial input setup time (see Figure 1)	20			20			ns
t <sub>su</sub>	Shift setup time (see Figure 1)	45			45			ns
th	Hold time at any input	0			0			ns
TA	Operating free-air temperature	-55		125	0		70	°C



SDLS062D - OCTOBER 1976 - REVISED FEBRUARY 2002

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				No.	:	SN54165		5	SN74165	5	
	PARAMETER		TEST CO	INDITIONS	MIN	TYP‡	MAX	MIN	түр‡	MAX	UNIT
VIH	High-level input voltage				2			2			V
VIL	Low-level input voltage						0.8			0.8	V
٧IK	Input clamp voltage		$V_{CC} = MIN,$	I <sub>I</sub> = -12 mA			-1.5			-1.5	V
V <sub>ОН</sub>	High-level output voltage		$V_{CC} = MIN,$ $V_{IL} = 0.8 V,$	V <sub>IH</sub> = 2 V, I <sub>OH</sub> = -800 μA	2.4	3.4		2.4	3.4		V
VOL	Low-level output voltage		$V_{CC} = MIN,$ $V_{IL} = 0.8 V,$	V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA		0.2	0.4		0.2	0.4	V
Ц	Input current at maximum	input voltage	$V_{CC} = MAX,$	V <sub>I</sub> = 5.5 V			1			1	mA
i	High lovel input ourrept	SH/LD		$\lambda = 2.4 \lambda$			80			80	
ЧΗ	Fligh-level input current	Other inputs	VCC = WAX,	v] = 2.4 v			40			40	μΑ
1	l ow lovel input current	SH/LD		$V_{\rm r} = 0.4 V_{\rm r}$			-3.2			-3.2	m۸
١Ľ	Low-level input current	Other inputs	VCC = WAX,	v] = 0.4 v			-1.6			-1.6	IIIA
los	Short-circuit output current	nt§	$V_{CC} = MAX$		-20		-55	-18		-55	mA
ICC	Supply current		V <sub>CC</sub> = MAX,	See Note 4		42	63		42	63	mA

NOTE 4: With the outputs open, CLK INH and CLK at 4.5 V, and a clock pulse applied to SH/LD, I<sub>CC</sub> is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ}C$ .

§ Not more than one output should be shorted at a time.

#### SN54165 and SN74165 switching characteristics, $V_{CC} = 5 V$ , $T_A = 25^{\circ}C$ (see Figure 1)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	ТҮР	МАХ	UNIT
fmax				20	26		MHz
<sup>t</sup> PLH		Anv	$C_1 = 15 \text{ pE } P_1 = 400 \text{ O}$		21	31	20
<sup>t</sup> PHL	LD	Апу	$C_{L} = 13 \text{ pr}, \text{ K}_{L} = 400 \text{ sz}$		27	40	115
<sup>t</sup> PLH	CLK	Δον	$C_{1} = 15 \text{ pE P}_{1} = 400 \text{ O}_{1}$		16	24	200
<sup>t</sup> PHL	ULK	Апу	$C_{L} = 15  \text{pr},  \text{K}_{L} = 400  \text{s}_{2}$		21	31	115
<sup>t</sup> PLH		0	$C_{1} = 15 \text{ pc} = 0.000$		11	17	20
<sup>t</sup> PHL		QH I	$C_{L} = 15  \text{pr},  \text{KL} = 400  \text{sz}$		24	36	115
<sup>t</sup> PLH		<u>.</u>	$C_{1} = 15 \text{ pE } P_{1} = 400 \text{ O}$		18	27	20
<sup>t</sup> PHL		QH	$C_{L} = 15  \text{pr},  \text{RL} = 400  \Omega$		18	27	IIS

fmax = maximum clock frequency, tpLH = propagation delay time, low-to-high-level output, tpHL = propagation delay time, high-to-low-level output



## The SN54165 and SN74165 devices are obsolete and are no longer supplied.

## SN54165, SN54LS165A, SN74165, SN74LS165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

SDLS062D - OCTOBER 1976 - REVISED FEBRUARY 2002

#### recommended operating conditions

			SN	54LS16	5A	SN	74LS16	5A	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current				-0.4			-0.4	mA
I <sub>OL</sub>	Low-level output current				4			8	mA
fclock	Clock frequency	-	0		25	0		25	MHz
+ /	Width of clock input pulse (see Figure 2)	Clock high	15			15			20
w(clock)	width of clock input pulse (see Figure 2)	Clock low	25			25			115
<b>•</b> " "	Width of load input pulse	Clock high	25			25			20
<sup>t</sup> w(load)	width of load input pulse	Clock low	17			17			115
t <sub>su</sub>	Clock-enable setup time (see Figure 2)		30			30			ns
t <sub>su</sub>	Parallel input setup time (see Figure 2)		10			10			ns
t <sub>su</sub>	Serial input setup time (see Figure 2)		20			20			ns
t <sub>su</sub>	Shift setup time (see Figure 2)		45			45			ns
t <sub>h</sub>	Hold time at any input		0			0			ns
TA	Operating free-air temperature		-55		125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEOTO			SN	154LS16	5A	SN	74LS16	5A	
PARAMETER		TESTC	ONDITIONS		MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIK	$V_{CC} = MIN,$	lı = –18 mA					-1.5			-1.5	V
VOH	$V_{CC} = MIN,$	V <sub>IH</sub> = 2 V,	$V_{IL} = MAX,$	I <sub>OH</sub> = -0.4 mA	2.5	3.5		2.7	3.5		V
Vei		$\lambda = 2 \lambda$	V MAX	I <sub>OL</sub> = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$v_{CC} = ivilla,$	VIH = 2 ∨,		I <sub>OL</sub> = 8 mA					0.35	0.5	v
Ц	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 7 V					0.1			0.1	mA
Чн	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V					20			20	μA
Ι <sub>ΙL</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.4 V					-0.4			-0.4	mA
IOS§	$V_{CC} = MAX$				-20		-100	-20		-100	mA
lcc	V <sub>CC</sub> = MAX,	See Note 4				18	30		18	30	mA

NOTE 4. With the outputs open, CLK INH and CLK at 4.5 V, and a clock pulse applied to SH/LD, I<sub>CC</sub> is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ}C$ .

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.



## The SN54165 and SN74165 devices are obsolete and are no longer supplied.

SDLS062D - OCTOBER 1976 - REVISED FEBRUARY 2002

## SN54LS165A and SN74LS165A switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see Figure 2)

PARAMETER <sup>†</sup>	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	МАХ	UNIT
fmax				25	35		MHz
<sup>t</sup> PLH		<b>A</b> py(	$P_1 = 2k\Omega C_1 = 15 pE$		21	35	200
<sup>t</sup> PHL	LD	Any	$R_{L} = 2 R_{22}, C_{L} = 15 pr$		26	35	115
<sup>t</sup> PLH	CLK	Any	$B_1 = 2k\Omega C_1 = 15 pE$		14	25	ne
<sup>t</sup> PHL	OER	Ану	NL = 2 NS2, OL = 10 pl		16	25	115
<sup>t</sup> PLH	u	0	$P_{1} = 2kO_{1}C_{2} = 15 pE$		13	25	200
<sup>t</sup> PHL		ЧН	$R_{L} = 2 R_{22}, O_{L} = 15 pr$		24	30	115
<sup>t</sup> PLH		<u>.</u>			19	30	
<sup>t</sup> PHL		⊂H ⊂	$R_{L} = 2 \text{ Ks2}, C_{L} = 15 \text{ pr}$		17	25	ns

† fmax = maximum clock frequency, tPLH = propagation delay time, low-to-high-level output, tPHL = propagation delay time, high-to-low-level output



# The SN54165 and SN74165 devices are obsolete and are no longer supplied.

### SN54165, SN54LS165A, SN74165, SN74LS165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

SDLS062D - OCTOBER 1976 - REVISED FEBRUARY 2002



- B. All diodes are 1N3064 or equivalent.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. S1 and S2 are closed for tPLH, tPHL, tPHZ, and tPLZ; S1 is open and S2 is closed for tPZH; S1 is closed and S2 is open for tPZL.
- E. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub>  $\approx$  50  $\Omega$ ; t<sub>r</sub> and t<sub>f</sub>  $\leq$  7 ns for Series 54/74 devices and t<sub>r</sub> and t<sub>f</sub>  $\leq$  2.5 ns for Series 54S/74S devices.
- F. The outputs are measured one at a time with one input transition per measurement.

#### Figure 1. Load Circuits and Voltage Waveforms



## The SN54165 and SN74165 devices are obsolete and are no longer supplied.

SDLS062D - OCTOBER 1976 - REVISED FEBRUARY 2002





- B. All diodes are 1N3064 or equivalent.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ . E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
- F. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub>  $\approx$  50  $\Omega$ , t<sub>r</sub>  $\leq$  1.5 ns, t<sub>f</sub>  $\leq$  2.6 ns.
- G. The outputs are measured one at a time with one input transition per measurement.

#### Figure 2. Load Circuits and Voltage Waveforms





www.ti.com

23-Mar-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-7700601VEA	ACTIVE	CDIP	J	16	25	TBD	A42	N / A for Pkg Type	
5962-7700601VFA	ACTIVE	CFP	W	16	25	TBD	A42	N / A for Pkg Type	
7700601EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
7700601FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
JM38510/30608B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/30608BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
JM38510/30608BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
M38510/30608B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/30608BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
M38510/30608BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SN54LS165AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN74165N	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI	
SN74LS165AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS165ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS165ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS165ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS165ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS165ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS165AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	
SN74LS165AN	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS165AN3	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI	
SN74LS165ANE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS165ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS165ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SNJ54LS165AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS165AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS165AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN54LS165A, SN54LS165A-SP, SN74LS165A :

• Catalog: SN74LS165A, SN54LS165A

Military: SN54LS165A

• Space: SN54LS165A-SP

## PACKAGE OPTION ADDENDUM



www.ti.com

23-Mar-2012

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

#### TAPE AND REEL INFORMATION





### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal													
	Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN	74LS165ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN	74LS165ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



## PACKAGE MATERIALS INFORMATION

19-Mar-2008



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS165ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS165ANSR	SO	NS	16	2000	346.0	346.0	33.0

#### **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		

**TI E2E Community Home Page** 

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2012, Texas Instruments Incorporated