PROGRAMMABLE OVERVOLTAGE PROTECTION FOR ERICSSON COMPONENTS SUBSCRIBER LINE INTERFACE CIRCUITS, SLICS

- **Overvoltage Protectors for listed SLICs:-**

SLIC †§	TISPPBL1	TISPPBL2
PBL 3762A/2	×	✓
PBL 3762A/4	×	✓
PBL 3764A/4	×	✓
PBL 3764A/6	×	✓
PBL 3766	✓	✓
PBL 3766/6	✓	✓
PBL 3767	✓	✓
PBL 3767/6	✓	✓
PBL 3860A/1	×	✓
PBL 3860A/6	×	✓
PBL 386 10/2	✓	✓
PBL 386 11/2	✓	✓
PBL 386 14/2	×	✓
PBL 386 15/2	×	✓
PBL 386 20/2	×	✓
PBL 386 21/2	×	✓
PBL 386 30/2	×	✓
PBL 386 40/2	×	✓
PBL 386 50/2	×	✓
PBL 386 61/2	< 55 mA‡	✓
PBL 386 65/2	< 55 mA‡	✓
PBL 387 10/1	×	✓

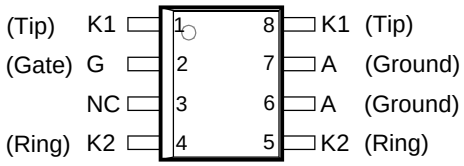
§ See Applications Information for earlier SLIC types.
‡ Use TISPPBL2 when programmed line current is above 55 mA

- **Rated for International Surge Wave Shapes**

WAVE SHAPE	STANDARD	I_{TSP} A
2/10 µs	GR-1089-CORE	100
1.2/50 µs	ITU-T K22	100
0.5/700 µs	I3124	40
10/700 µs	ITU-T K20, K21	40
10/1000 µs	GR-1089-CORE	30

- **Specified Impulse Limiting Voltage**
  - **Voltage-Time Envelope Guaranteed**
  - **Full -40 °C to 85 °C Temperature Range**
- **UL Recognized, E132482**

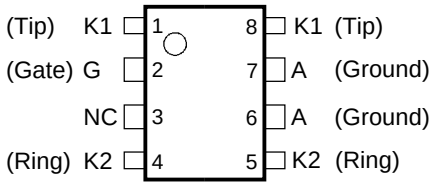
D PACKAGE
(TOP VIEW)



MD6XANA

NC - No internal connection
Terminal typical application names shown in parenthesis

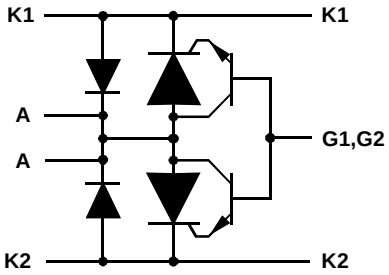
P PACKAGE
(TOP VIEW)



MD6XAV

NC - No internal connection
Terminal typical application names shown in parenthesis

device symbol



Terminals K1, K2 and A correspond to the alternative line designators of T, R and G or A, B and C. The negative protection voltage is controlled by the voltage, $V_{GG,}$ applied to the G terminal.

SD6XAEA

- **Feed-Through Package Connections**
  - **Minimises Inductive Wiring Voltages**
- **Surface Mount and Through-Hole Ordering Options**

DEVICE CODE	PACKAGE AND CARRIER TYPE
TISPPBLxD	8-pin Small-Outline in a Tube
TISPPBLxDR	8-pin Small-Outline on Tape and Reeled
TISPPBLxP	8-pin Plastic DIP in a Tube

† Customers are advised to obtain the latest version of the relevant Ericsson Components SLIC information to verify, before placing orders, that the information being relied on is current.

description

The TISPPBL1 and TISPPBL2 are dual forward-conducting buffered p-gate overvoltage protectors. They are designed to protect the Ericsson Components SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. The TISPPBLx limits voltages that exceed the SLIC supply rail levels.

The SLIC line driver section is typically powered by a negative voltage, V_{Bat}, in the region of -10 V to -85 V. The protector gate is connected to this negative supply. This references the protection (clipping) voltage to the negative supply voltage. As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimised. The TISPPBLx buffered gate design reduces the loading on the SLIC supply during overvoltages caused by power cross and induction.

Positive overvoltages are clipped to ground by diode forward conduction. Negative overvoltages are initially clipped close to the SLIC negative supply rail value. If sufficient current is available from the overvoltage, then the protector will crowbar into a low voltage ground referenced on-state condition. As the overvoltage subsides the high holding current of the crowbar prevents d.c. latchup. The difference between the TISPPBL1 and TISPPBL2 is the minimum value of holding current. The 105 mA TISPPBL1 can delatch SLIC programmed line currents up to 55 mA and the 150 mA TISPPBL2 can delatch all programmed line current values.

These monolithic protection devices are fabricated in ion-implanted planar vertical power structures for high reliability and in normal system operation they are virtually transparent. The TISPPBLx is available in 8-pin plastic small-outline surface mount package and 8-pin plastic dual-in-line package.

absolute maximum ratings, -40 °C ≤ T_A ≤ 85 °C (unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage, I_G = 0	V_{DRM}	-100	V
Repetitive peak gate-cathode voltage, V_{KA} = 0	V_{GKRM}	-90	V
Non-repetitive peak on-state pulse current (see Notes 1 and 2)	I_{TSP}		A
10/1000 µs (Bellcore GR-1089-CORE, Issue 2, December 1997, Section 4)		30	
0.2/310 µs (I3124, open-circuit voltage wave shape 0.5/700 µs)		40	
5/310 µs (ITU-T K20 & K21, open-circuit voltage wave shape 10/700 µs)		40	
1/20 µs (ITU-T K22, open-circuit voltage wave shape 1.2/50 µs)		100	
2/10 µs (Bellcore GR-1089-CORE, Issue 2, December 1997, Section 4)		100	
Non-repetitive peak on-state current, 50/60 Hz (see Notes 1 and 2)	I_{TSM}		A
100 ms		11	
1 s		4.5	
5 s		2.4	
300 s		0.95	
900 s		0.93	
Non-repetitive peak gate current, 1/2 µs pulse, cathodes commoned (see Note 1)	I_{GSM}	40	A
Operating free-air temperature range	T_A	-40 to +85	°C
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. Initially the protector must be in thermal equilibrium with -40 °C ≤ T_J ≤ 85 °C. The surge may be repeated after the device returns to its initial conditions.

2. These non-repetitive rated currents are peak values for either polarity. The rated current values may be applied either to the Ring to Ground or to the Tip to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of an individual terminal pair). Above 85 °C, derate linearly to zero at 150 °C lead temperature.

recommended operating conditions

SEE Figure 18		MIN	TYP	MAX	UNIT
C1	Gate decoupling capacitor	100	220		nF
R1a R1b	Series resistance for GR-1089-CORE first-level and second-level surge survival Series resistance for GR-1089-CORE first-level surge survival Series resistance for ITU-T recommendation K20/21	40 25 10			Ω

electrical characteristics, -40 °C ≤T_A ≤ 85 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_D	Off-state current	$V_D = V_{DRM}$, V_{GK} = 0	T_J = -40 °C			-5	µA
			T_J = 85 °C			-50	µA
$V_{(BO)}$	Breakover voltage	I_T = -20 A, 0.5/700 generator, Figure 3 test circuit (See Figure 2)				-70	V
$t_{(BR)}$	Breakdown time	I_T = -20 A, 0.5/700 generator, Figure 3 test circuit (See Figure 2)	$V_{(BR)}$ < -50 V			1	µs
V_F	Forward voltage	I_F = 5 A, t_w = 500 µs				3	V
V_{FRM}	Peak forward recovery voltage	I_F = 20 A, 0.5/700 generator, Figure 3 test circuit (See Figure 2)				8	V
t_{FR}	Forward recovery time	I_F = 20 A, 0.5/700 generator, Figure 3 test circuit (See Figure 2)	V_F > 5 V V_F > 1 V			1 10000	µs
I_H	Holding current	I_T = -1 A, di/dt = 1A/ms, V_{GG} = -50 V,	TISPPBL1 TISPPBL2	-105 -150			mA
I_{GAS}	Gate reverse current	$V_{GG} = V_{GKRM}$, V_{AK} = 0	T_J = -40 °C			-5	µA
			T_J = 85 °C			-50	µA
I_{GAT}	Gate reverse current, on state	I_T = -0.5 A, t_w = 500 µs, V_{GG} = -50 V, T_A = 25 °C				-1	mA
I_{GAF}	Gate reverse current, forward conducting state	I_F = 1 A, t_w = 500 µs, V_{GG} = -50 V, T_A = 25 °C			-10		mA
I_{GT}	Gate trigger current	I_T = -5 A, $t_{p(g)}$ ≥ 20 µs, V_{GG} = -50 V, T_A = 25 °C				5	mA
V_{GT}	Gate trigger voltage	I_T = -5 A, $t_{p(g)}$ ≥ 20 µs, V_{GG} = -50 V, T_A = 25 °C				2.5	V
C_{AK}	Anode-cathode off-state capacitance	f = 1 MHz, V_d = 1 V, I_G = 0, T_A = 25 °C (see Note 3)	V_D = -3 V			110	pF
			V_D = -50 V			60	pF

NOTE 3: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

thermal characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to free air thermal resistance	P_{tot} = 0.8 W, T_A = 25 °C 5 cm^2, FR4 PCB	D Package			160	°C/W
			P Package			100	

PARAMETER MEASUREMENT INFORMATION

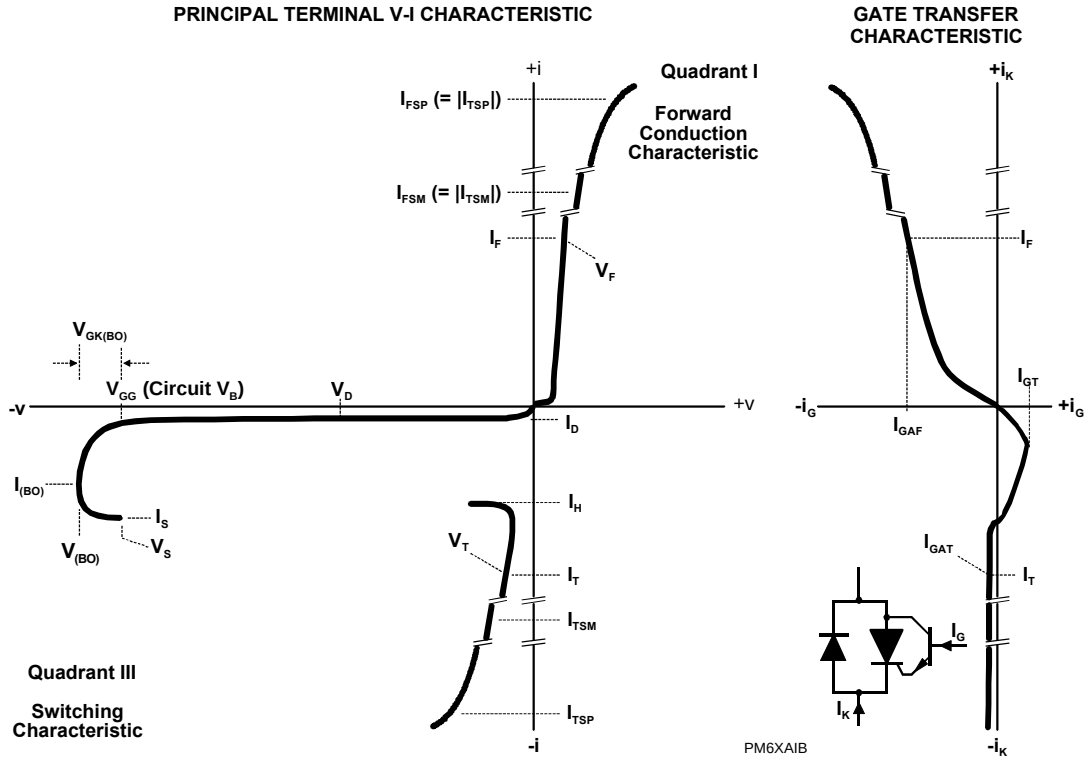


Figure 1 PRINCIPAL TERMINAL AND GATE TRANSFER CHARACTERISTICS

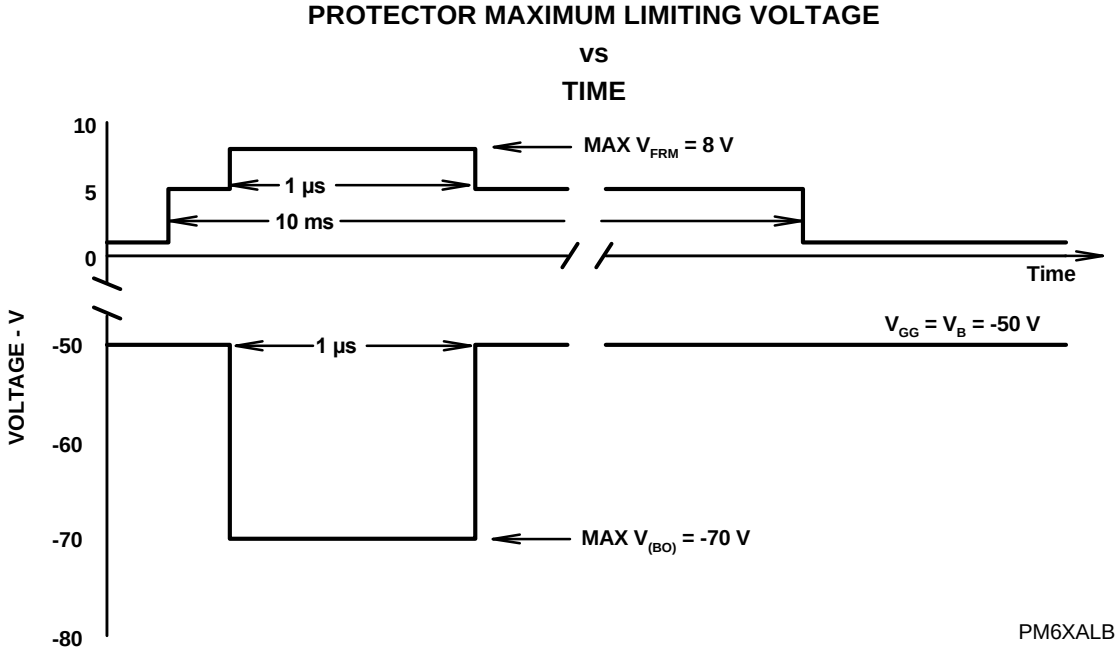


Figure 2 TRANSIENT LIMITS FOR TISPPBLx LIMITING VOLTAGE

PARAMETER MEASUREMENT INFORMATION

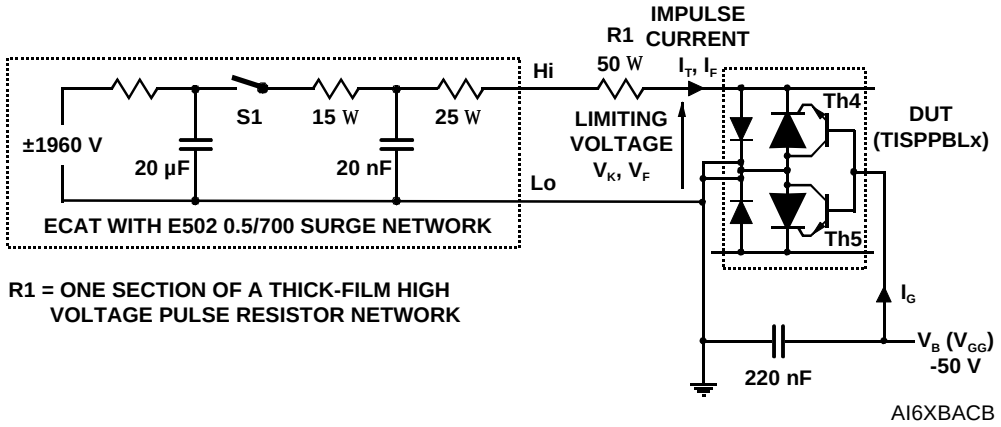


Figure 3 TEST CIRCUIT FOR MEASUREMENT OF LIMITING VOLTAGE

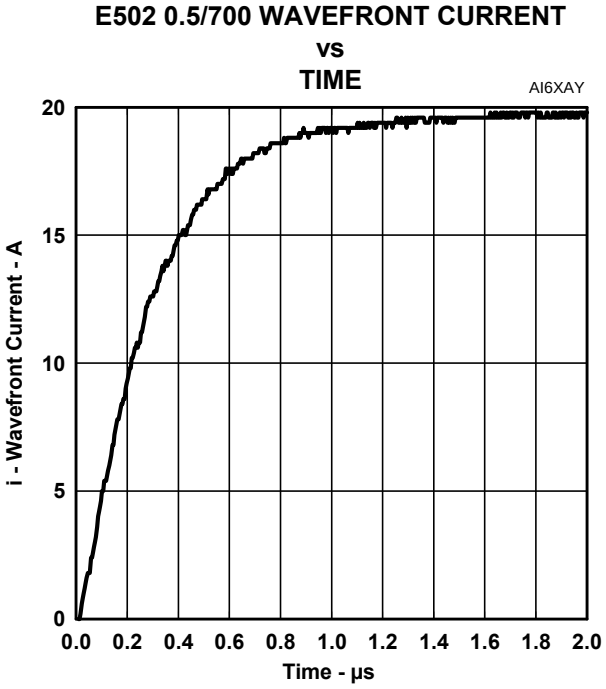


Figure 4 CURRENT WAVEFRONT

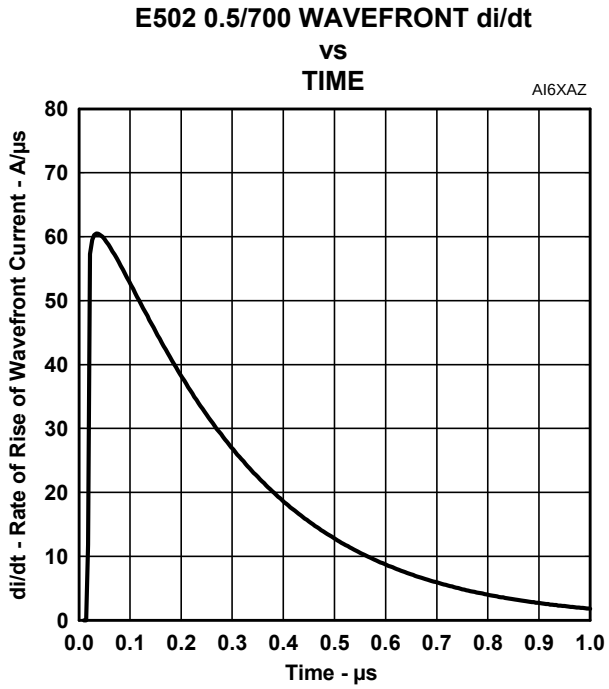


Figure 5 CURRENT WAVEFRONT di/dt

THERMAL INFORMATION

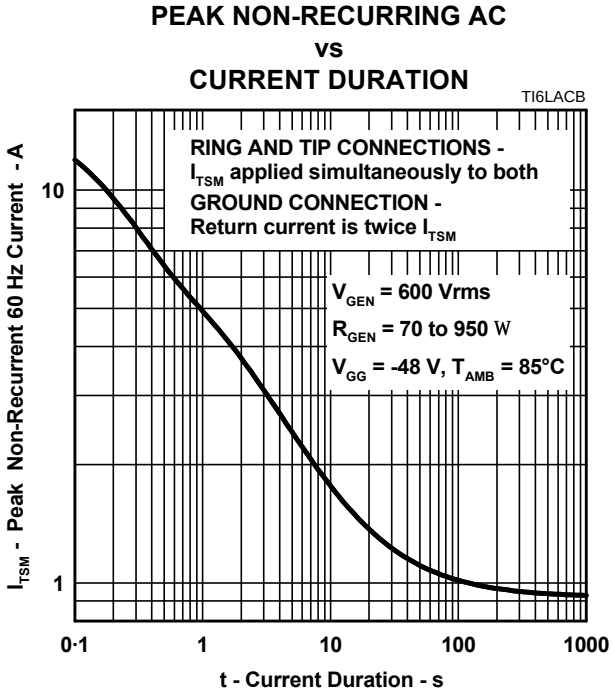


Figure 6

TYPICAL CHARACTERISTICS

DISTRIBUTION LIMITS OF THYRISTOR LIMITING VOLTAGE vs TIME

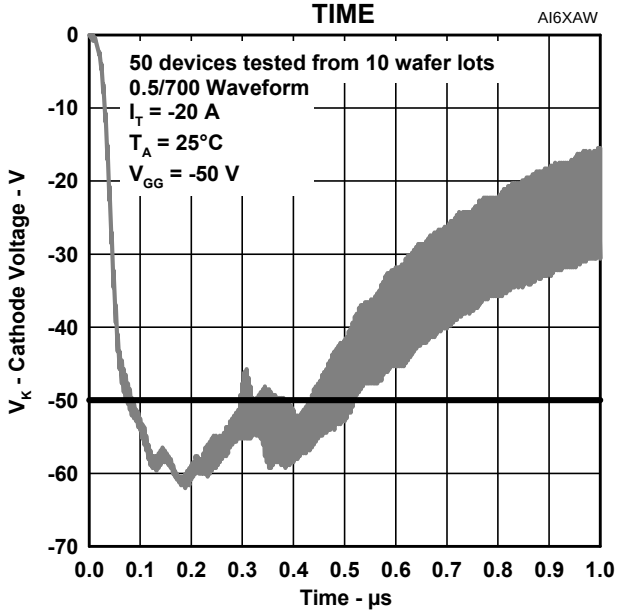


Figure 7

DISTRIBUTION LIMITS OF DIODE FORWARD VOLTAGE vs TIME

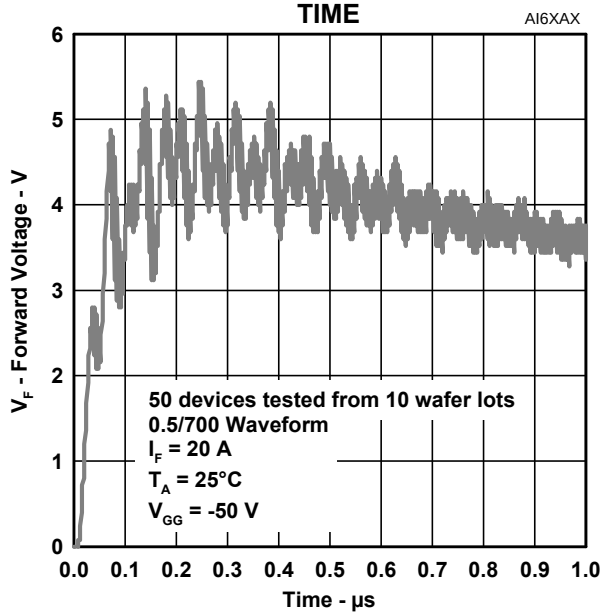


Figure 8

CUMULATIVE POPULATION % vs PEAK LIMITING VOLTAGE

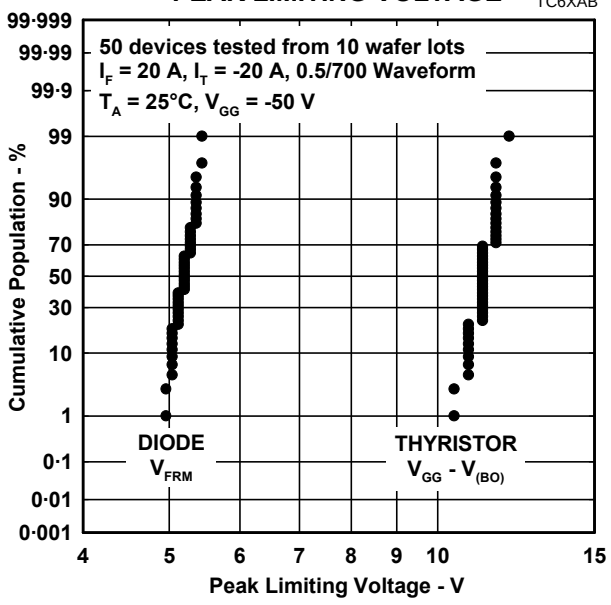


Figure 9

DIODE FORWARD CURRENT vs FORWARD VOLTAGE

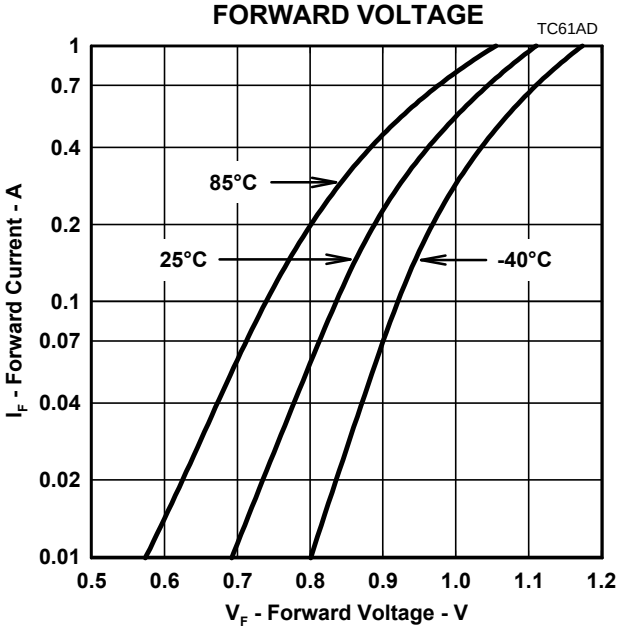


Figure 10

TYPICAL CHARACTERISTICS

**CUMULATIVE POPULATION %
vs
LIMITING TIME**

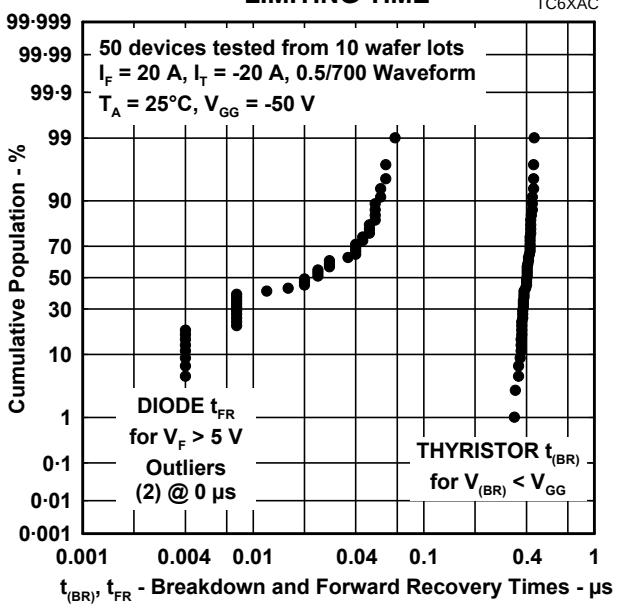


Figure 11

**NORMALISED PEAK LIMITING VOLTAGES
vs
JUNCTION TEMPERATURE**

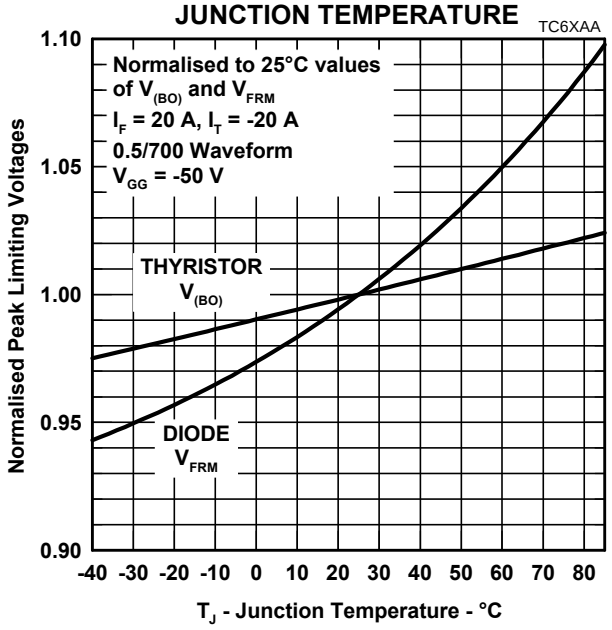


Figure 12

APPLICATIONS INFORMATION

operation of gated protectors

The following SLIC circuit definitions are used in this data sheet:

V_{BAT} — Package pin label for the battery supply voltage.
V_{Bat} — Voltage applied to the V_{BAT} pin.
V_B — Negative power supply voltage applied to the V_{BAT} pin via an isolation diode. This voltage is also the gate reference voltage, V_{GG}, of the TISPPBLx. When the isolation diode, D1, is conducting, then $V_{Bat} = V_B + 0.7$.

The isolation diode, D1 in Figure 13, is to prevent a damaging current flowing into the SLIC substrate (V_{BAT} pin) if the V_{Bat} voltage becomes more negative than the V_B supply during a negative overvoltage condition. Each SLIC needs an isolation diode from the V_B voltage supply.

Figure 13 and Figure 14 show how the TISPPBLx limits overvoltages. The TISPPBLx thyristor sections limit negative overvoltages and the diode sections limit positive overvoltages.

Negative overvoltages (Figure 13) are initially clipped close to the SLIC negative supply rail value (V_B) by the conduction of the transistor base-emitter and the thyristor gate-cathode junctions. If sufficient current is available from the overvoltage, then the thyristor will crowbar into a low voltage ground referenced on-state condition. As the overvoltage subsides the high holding current of the crowbar thyristor prevents d.c. latchup.

The negative protection voltage will be the sum of the gate supply (V_B) and the peak gate(terminal)-cathode voltage ($V_{GK(BO)}$). Under a.c. overvoltage conditions $V_{GK(BO)}$ will be less than 3 V. The integrated transistor buffer in the TISPPBLx greatly reduces the gate positive current (from about 50 mA to 1 mA) and introduces a negative gate current. Figure 1 shows that the TISPPBLx gate current depends on the current being

conducted by the principal terminals. The gate current is positive during clipping (charging the V_B supply) and negative when the thyristor is on or the diode is conducting (loading the V_B supply). Without the negative gate current and the reduced level of positive gate current the V_B supply could be charged with a current of nearly 100 mA. As the V_B supply is likely to be electronic it would not be designed to be charged like a battery. As a result, the SLIC could be destroyed by the voltage of V_B increasing to a level that exceeded the SLIC's capability on the V_{BAT} pin. The integrated transistor buffer removes this problem.

Fast rising impulses will cause short term overshoots in gate-cathode voltage. The negative protection voltage under impulse conditions will also be increased if there is a long connection between the gate decoupling capacitor, C1, and the gate terminal. During the initial rise of a fast impulse, the gate current (I_G) is the same as the cathode current (I_K). Rates of 60 A/µs can cause inductive voltages of 0.6 V in 2.5 cm of printed wiring track. To minimise this inductive voltage increase of protection voltage, the length of the capacitor to gate terminal tracking should be minimised. Inductive voltages in the protector cathode wiring can increase the protection voltage. These voltages can be minimised by routing the SLIC connection through the protector as shown in Figure 13 and Figure 14.

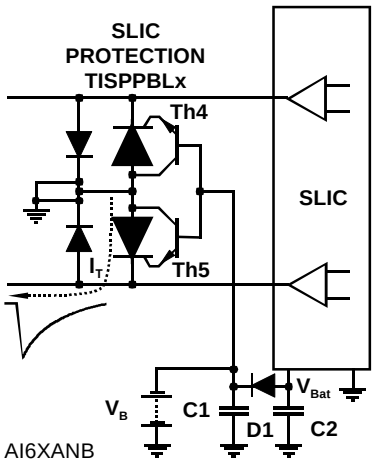


Figure 13 NEGATIVE OVERVOLTAGE CONDITION

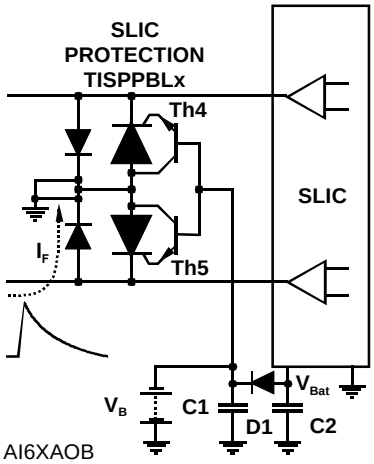


Figure 14 POSITIVE OVERVOLTAGE CONDITION

Positive overvoltages (Figure 14) are clipped to ground by forward conduction of the diode section in the TISPPBLx. Fast rising impulses will cause short term overshoots in forward voltage (V_{FRM}).

TISPPBLx limiting voltages

This clause details the TISPPBLx voltage limiting levels under impulse conditions.

test circuit

Figure 3 shows the basic test circuit used for the measurement of impulse limiting voltage. During the impulse, the high levels of electrical energy and rapid rates of change cause electrical noise to be induced or conducted into the measurement system. It is possible for the electrical noise voltage to be many times the wanted signal voltage. Elaborate wiring and measurement techniques where used to reduce the noise voltage to less than 2 V peak to peak.

impulse generator

A Keytek ECAT E-Class series 100 with an E502 surge network was used for testing. The E502 produces a 0.5/700 voltage impulse. This particular waveform was used as it has the fastest rate of current rise (di/dt) of the commonly used lightning surge waveforms. This maximises the measured limiting voltage. Figure 4 shows the current wavefront through the DUT. To produce a peak test current level of ±20 A, the E502 charging voltage was set to ±1960 V. Figure 5 shows the DUT current di/dt. Initially the wavefront current rises

at 60 A/µs, this rate then reduces as the peak current is approached. At the TISPPBLx $V_{(BO)}$ condition the di/dt is about 50 A/µs.

limiting voltage levels

Fifty devices were measured in the test circuit of Figure 3. The 50 devices were made up from groups of 5 devices taken from 10 separately processed device lots. Figure 7 shows the total waveform variation of the thyristor limiting voltage across the 50 devices. This shows that the largest peak limiting voltage (Breakover voltage, $V_{(BO)}$) is -62 V, a 12 V overshoot beyond the -50 V gate reference supply, V_B. The limiting voltage exceeds the gate reference supply voltage level for a period ($t_{(BR)}$) of about 0.4 µs.

Figure 9 and Figure 11 show these two waveform parameters in terms of device population. In Figure 9, the limiting voltage is shown in terms of the overshoot beyond the gate reference supply (V_B - $V_{(BO)}$). Removing the gate reference voltage level magnifies the thyristor limiting voltage variation and shows the data stratification caused by the oscilloscope digitisation. Extrapolating the data trend indicates that the overshoot is less than 14 V at the 99.997% level (equal to 30 ppm of the population exceeding 14 V, equivalent to +4 sigma point of a normal distribution). In Figure 11, extrapolating the thyristor data trend to the 99.997% level indicates a maximum breakdown time, $t_{(BR)}$, of 0.5 µs. Figure 12 shows that increasing the temperature up to 85 °C increases the thyristor peak limiting voltage by 2.4%, giving a maximum 85 °C peak limiting voltage of 1.024x(-50-14) = -65.5 V. Over the -40 °C to 85 °C temperature range the TISPPBLx is specified to have a maximum $V_{(BO)}$ value of -70 V and a breakdown time, $t_{(BR)}$, of 1 µs.

Figure 8 shows the total waveform variation of the diode limiting voltage across the 50 devices. The peak limiting voltage (Peak Forward Recovery Voltage V_{FRM}) is less than 6 V, and this value includes the 2 V of magnetically induced noise in the probe. Figure 9 shows that extrapolated 99.997% level is about 5.5 V. In Figure 11, extrapolating the diode data trend to the 99.997% level indicates a maximum forward recovery time, t_{FR}, of 0.1 µs. Figure 12 indicates that there is about a 10% uplift by increasing the temperature to 85 °C. This gives a maximum 85 °C peak limiting voltage of 1.1x(5.5) = 6.1 V. Over the -40 °C to 85 °C temperature range, the TISPPBLx is specified to have a maximum V_{FRM} value of 8 V and a maximum forward recovery time of 1 µs.

Diodes do not switch to a much lower voltage like thyristors, so the diode limiting voltage applies for the whole impulse duration. Forward voltages of 1 V or less are normally considered safe. Figure 10 shows that the lowest current 1 V condition occurs at -40 °C with a current of 0.3 A. When the TISPPBLx is tested with the rated 10/1000 impulse it would take about 8 ms for the current to decay from 30 A to 0.3 A. Over the -40 °C to 85 °C temperature range, the TISPPBLx is specified to have a V_F below 1 V within 10 ms.

SLIC protection requirements

This clause discusses the voltage withstand capabilities of the various Ericsson Components SLIC groups and compares these to the TISPPBLx protector parameters. The examples provided are intended to provide designers information on how the TISPPBLx protector and specific SLICs work together. Designers should always follow the circuit design recommendations contained in the latest edition of a SLIC data sheet.

temperature range

Some SLICs are rated for 0 °C to 70 °C operation, others for -40 °C to 85 °C operation. The TISPPBLx protector is specified for -40 °C to 85 °C operation and so covers both temperature ranges.

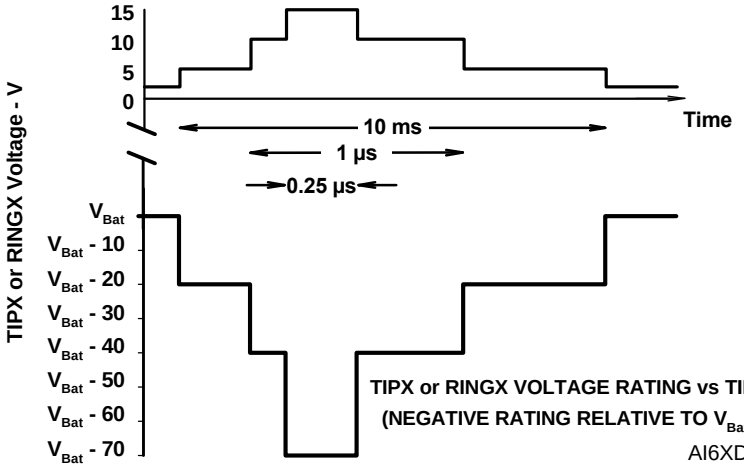
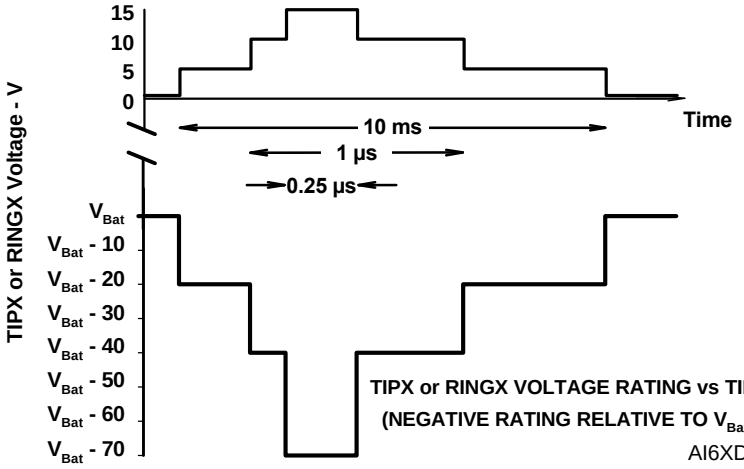
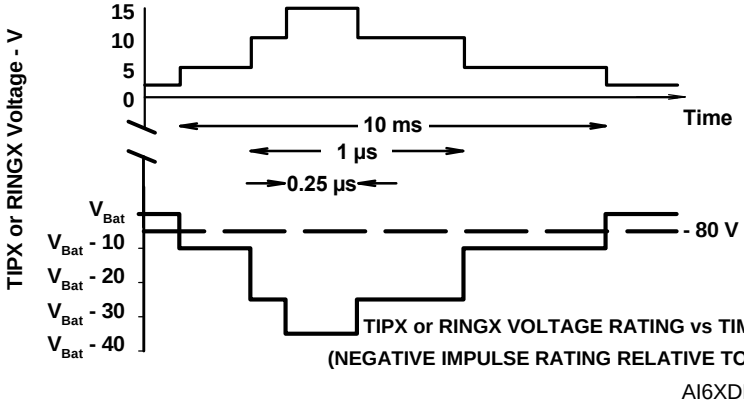
PART NUMBER	MAXIMUM VOLTAGE RATINGS
PBL 3762A/2 **PBL 3762A/4** **PBL 3764A/4** **PBL 3764A/6** **PBL 3860A/1** **PBL 3860A/6** **PBL 386 10/2** **PBL 386 11/2** **PBL 386 14/2** **PBL 386 15/2** **PBL 386 61/2** **PBL 386 65/2** **PBL 387 10/1**	d.c. V_{BAT} & +2 V, < 10 ms V_{BAT} -20 V & +5 V, < 1 µs V_{BAT} -40 V & +10 V, < 250 ns V_{BAT} -70 V & +15 V  **TIPX or RINGX VOLTAGE RATING vs TIME** **(NEGATIVE RATING RELATIVE TO V_{Bat})** AI6XDBAA
PBL 3766 **PBL 3766/6** **PBL 3767** **PBL 3767/6**	d.c. V_{BAT} & +0.5 V, < 10 ms V_{BAT} -20 V & +5 V, < 1 µs V_{BAT} -40 V & +10 V, < 250 ns V_{BAT} -70 V & +15 V  **TIPX or RINGX VOLTAGE RATING vs TIME** **(NEGATIVE RATING RELATIVE TO V_{Bat})** AI6XDBAB
PBL 386 20/2 **PBL 386 21/2** **PBL 386 30/2** **PBL 386 40/2** **PBL 386 50/2**	d.c. -80 V & +2 V, < 10 ms V_{BAT} -10 V & +5 V, < 1 µs V_{BAT} -25 V & +10 V, < 250 ns V_{BAT} -35 V & +15 V  **TIPX or RINGX VOLTAGE RATING vs TIME** **(NEGATIVE IMPULSE RATING RELATIVE TO V_{Bat})** AI6XDBAC

Figure 15 TIPX AND RINGX RATED VALUES

normal operation

Depending on the SLIC type, the maximum SLIC supply voltage rating (V_{Bat}) will be -70 V, -80 V or -85 V. The -90 V rating of the TISPPBLx gate-cathode (V_{GKRM}) exceeds the highest SLIC voltage rating. To restore normal operation after the TISPPBLx has switched on, the minimum switch-off current (holding current I_H) needed is equal to the maximum SLIC short circuit current to ground (d.c. line current together with the maximum longitudinal current). The first page of this data sheet has a list of the appropriate TISPPBLx protectors that can be used with each SLIC.

maximum TIPX and RINGX terminal ratings

The withstand levels of a SLIC line drive amplifier TIPX and RINGX can be expressed in terms of maximum voltage for certain time periods. The negative voltage rating can be specified in two ways; relative to ground or relative to the SLIC negative supply voltage (V_{Bat}).

The TIPX or RINGX voltage withstand levels for the current range of Ericsson SLICs falls into three groups, see Figure 15. The first group, headed by the PBL 3762A/2 SLIC, has a positive polarity d.c. withstand of +2 V. For 10 ms, the output can withstand a voltage of +5 V. For 1 µs, the output can withstand a voltage of +10 V. For 250 ns, the output is able to withstand a voltage of +15 V.

In the negative polarity, the output can withstand V_{Bat} continuously. For 10 ms, the output can withstand a voltage of V_{Bat} - 20 V. For 1 µs, the output can withstand a voltage of V_{Bat} - 40 V. For 250 ns, the output is able to withstand a voltage of V_{Bat} - 70 V.

The second group, headed by the PBL 3766 SLIC, has a positive polarity d.c. withstand of +0.5 V. For 10 ms, 1 µs and 250 ns the withstand voltage is the same as the PBL 3762A/2 group. In the negative polarity the withstand voltage of the PBL 3766 group is the same as the PBL 3762A/2 group.

The third group, headed by the PBL 386 20/2 SLIC, has the same positive polarity withstand as the PBL 3762A/2 group. In the negative polarity, the output can withstand -80 V continuously. For 10 ms, the output can withstand a voltage of V_{Bat} - 10 V. For 1 µs, the output can withstand a voltage of V_{Bat} - 25 V. For 250 ns, the output is able to withstand a voltage of V_{Bat} - 35 V.

protection requirements to cover all SLICs

To protect all SLICs, the TISPPBLx protector must limit the voltage to the lowest withstand levels of the three SLIC groups shown in Figure 15. Figure 16 shows that this will be the positive polarity rating of the PBL 3766 group and the negative rating of the PBL 386 20/2 group. .

TISPPBLx voltage limiting performance

Figure 17 shows how the TISPPBLx protection voltages compare to the minimum voltage withstands of Figure 16. The two shaded areas represent the positive and negative maximum limiting voltage levels of the TISPPBLx from Figure 2. The isolation diode voltage drop displaces the TISPPBLx negative limiting voltage 1 µs, -20 V pulse area by -0.7 V from V_{Bat}. So the actual negative limiting voltage is -20.7 V relative to V_{Bat}. This value does not exceed any part of the SLIC minimum negative voltage ratings. Any negative voltage disturbance in the V_B supply caused by TISPPBLx gate current will be tracked in V_{Bat} by conduction of the isolation diode D1. So a negative going change in V_B does not substantially increase the TIPX and RINGX voltage stress relative to V_{Bat}. However, the absolute value of V_{Bat} with respect to ground must be kept within the data sheet rating. In the positive polarity the TISPPBLx limits the maximum voltage to 8 V in a 1 µs period and between 1 V and 5 V for a 10 ms period. These values do not exceed any of the SLIC minimum positive voltage ratings.

application circuit

Figure 18 shows a typical TISPPBLx SLIC card protection circuit. The incoming line conductors, R and T, connect to the relay matrix via the series over-current protection. Fusible resistors, fuses and positive

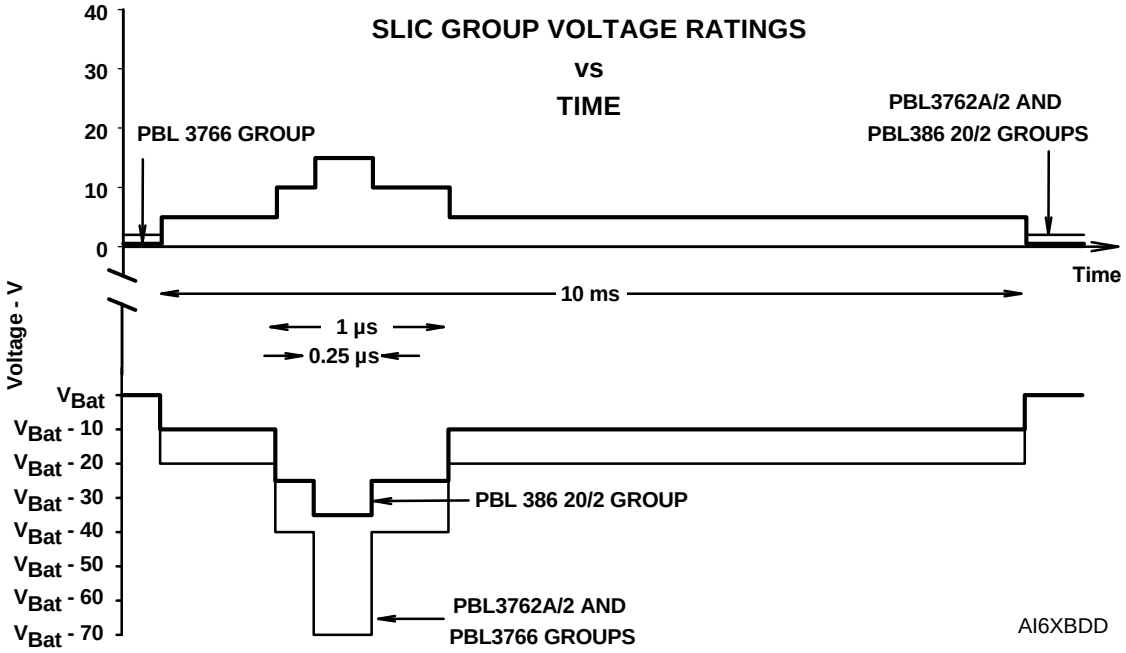


Figure 16 SLIC VOLTAGE RATINGS

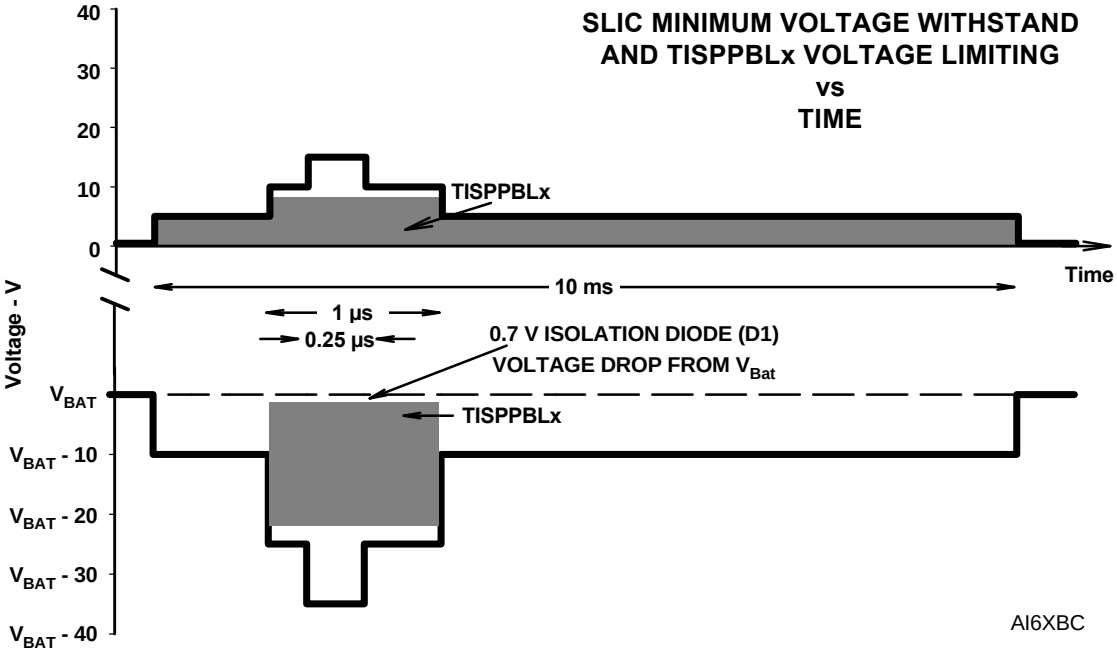


Figure 17 SLIC VOLTAGE RATINGS AND TISPPBLx PROTECTION LEVELS

temperature coefficient (PTC) resistors can be used for over-current protection. Resistors will reduce the prospective current from the surge generator for both the TISPPBLx and the ring/test protector. The TISP7xxxF3 protector has the same protection voltage for any terminal pair. This protector is used when the ring generator configuration may be ground or battery-backed. For dedicated ground-backed ringing generators, the TISP3xxxF3 gives better protection as its inter-conductor protection voltage is twice the conductor to ground value.

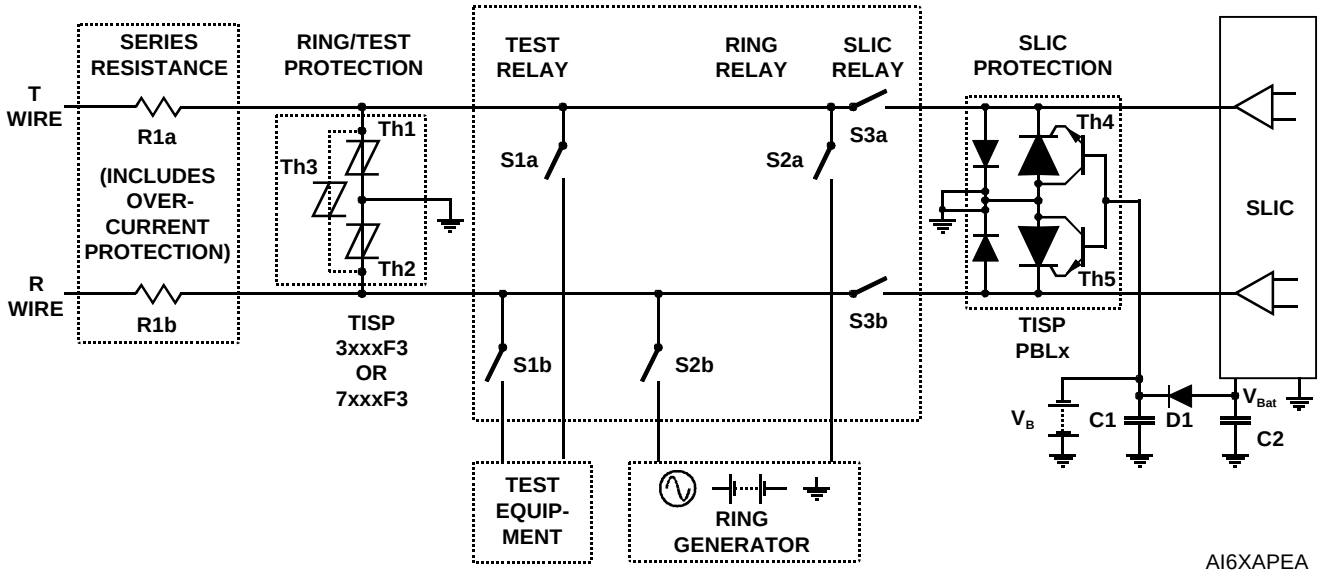


Figure 18 TYPICAL APPLICATION CIRCUIT

Relay contacts 3a and 3b connect the line conductors to the SLIC via the TISPPBLx protector. Closing contacts 3a and 3b connects the TISPPBLx protector in parallel with the ring/test protector. As the ring/test protector requires much higher voltages than the TISPPBLx to operate, it will only operate when the contacts 3a and 3b are open. Both protectors will divert the same levels of peak surge current and their required current ratings should be similar. The TISPPBLx protector gate reference voltage comes from the SLIC negative supply feed (V_B). A local gate capacitor, C1, sources the gate current pulses caused by fast rising impulses.

Earlier protection recommendations

The table below lists the protection recommendations from earlier versions of the TISPPBLx data sheet.

SLIC	TISPPBL1	TISPPBL2
PBL 3796	< 55 mA‡	✓
PBL 3796/2	< 55 mA‡	✓
PBL 3798	< 55 mA‡	✓
PBL 3798/2	< 55 mA‡	✓
PBL 3798/5	< 55 mA‡	✓
PBL 3798/6	✓	✓
PBL 3799	×	✓
PBL 3799/2	×	✓
PBL 386 20/1 ¶	✓	✓
PBL 386 21/1 ¶	✓	✓
PBL 386 30/1 ¶	✓	✓
PBL 386 40/1 ¶	✓	✓
PBL 386 50/1 ¶	✓	✓

¶ Product Change Notification 109 21-PBL 386 xx/1-1 Uen of 06-06-1999 improved the silicon design of the PBL 386 20/1, PBL 386 21/1, PBL 386 30/1, PBL 386 40/1 and PBL 386 50/1. These improved devices are designated by a /2 as PBL 386 20/2, PBL 386 21/2, PBL 386 30/2, PBL 386 40/2 and PBL 386 50/2 respectively.

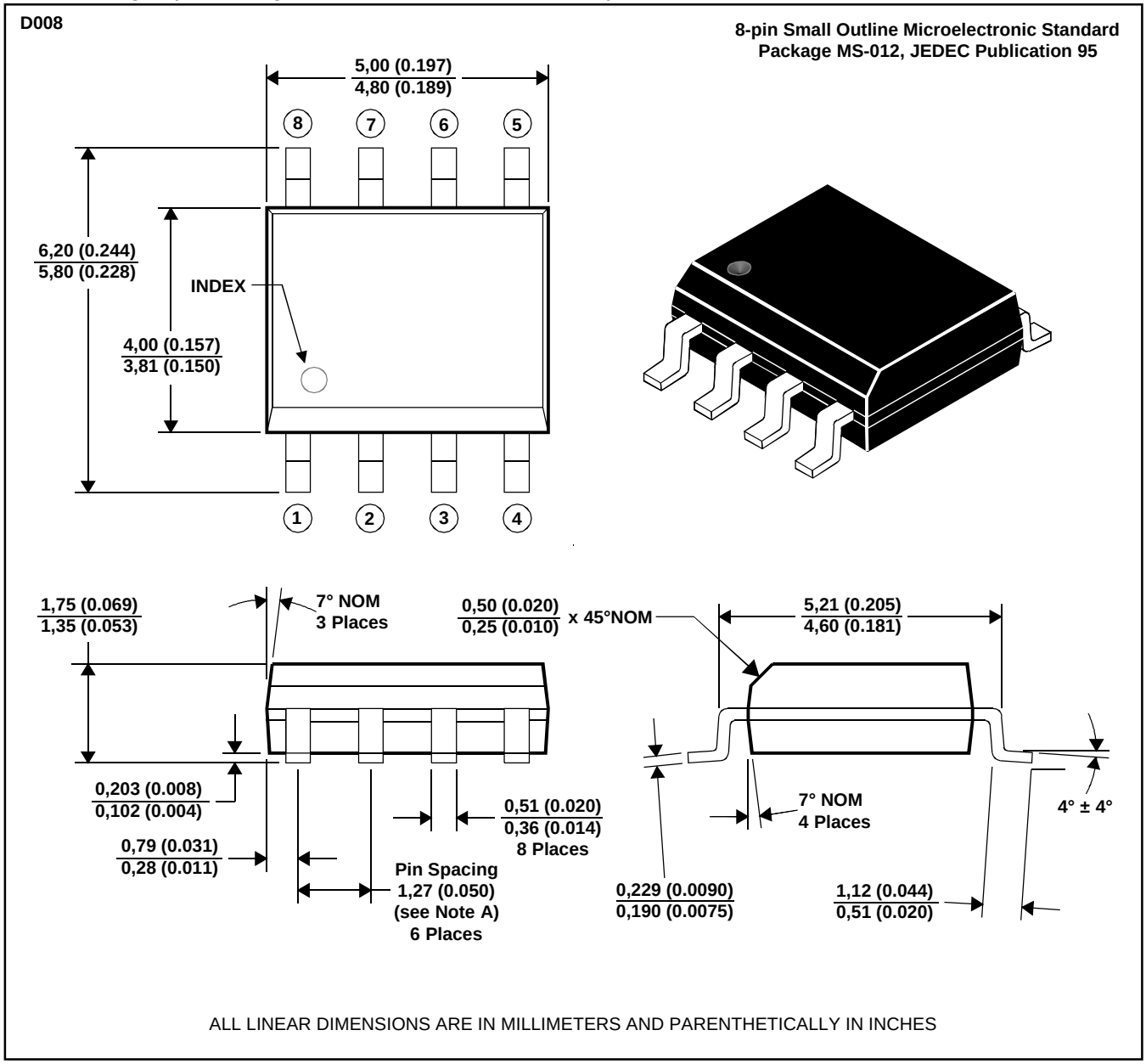
‡ Use TISPPBL2 when programmed line current is above 55 mA

MECHANICAL DATA

D008

plastic small-outline package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



MDXXAAC

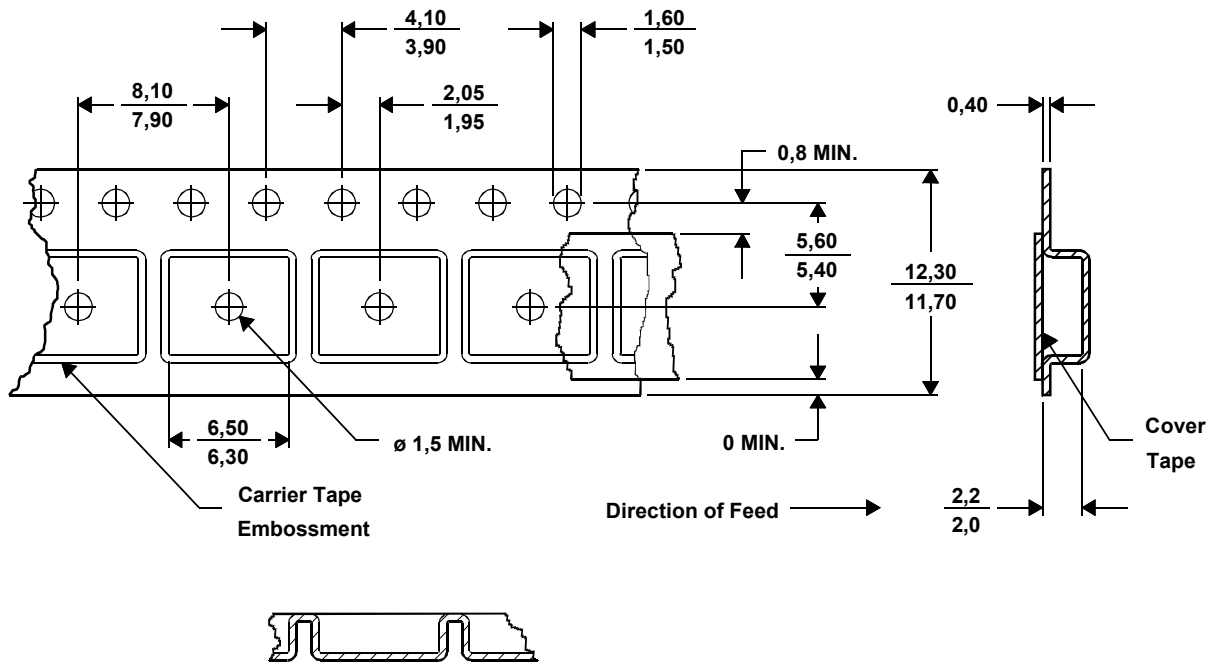
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002).

MECHANICAL DATA

D008

tape dimensions

D008 Package (8-pin Small Outline) Single-Sprocket Tape



ALL LINEAR DIMENSIONS IN MILLIMETERS

NOTES: A. Taped devices are supplied on a reel of the following dimensions:-

MDXXATB

Reel diameter:	330 +0,0/-4,0 mm
Reel hub diameter:	100 ±2,0 mm
Reel axial hole:	13,0 ±0,2 mm

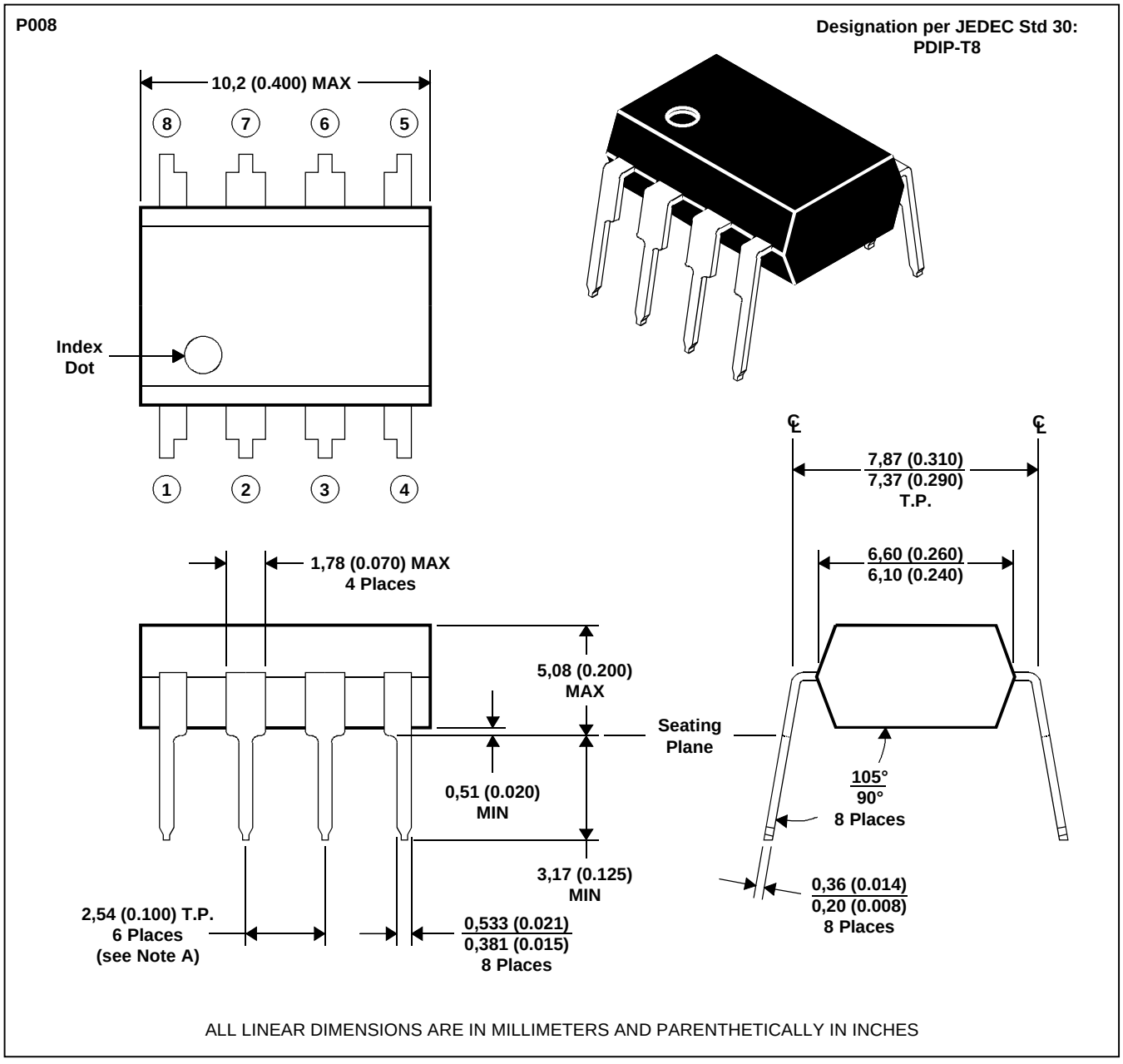
B. 2500 devices are on a reel.

MECHANICAL DATA

P008

plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centres. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position

MDXXABA