



Data sheet acquired from Harris Semiconductor SCHS198C

November 1997 - Revised May 2003

High Speed CMOS Logic Dual 4-Stage Static Shift Register

Features

- Maximum Frequency, Typically 60MHz
 C_L = 15pF, V_{CC} = 5V, T_A = 25°C
- · Positive-Edge Clocking
- Overriding Reset
- · Buffered Inputs and Outputs
- Fanout (Over Temperature Range)
- Wide Operating Temperature Range ... -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V

Description

The 'HC4015 consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent Clock (CP) and Reset (MR) inputs as well as a single serial Data input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the Data input is transferred into the first register stage and shifted over one stage at each positive- going clock transition. Resetting of all stages is accomplished by a high level on the reset line.

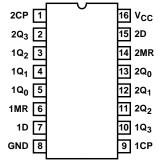
The device can drive up to 10 low power Schottky equivalent loads. The 'HC4015 is an enhanced version of equivalent CMOS types.

Ordering Information

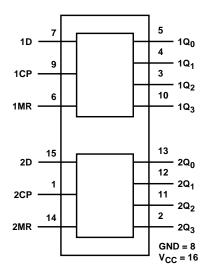
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4015F3A	-55 to 125	16 Ld CERDIP
CD74HC4015E	-55 to 125	16 Ld PDIP
CD74HC4015M	-55 to 125	16 Ld SOIC

Pinout

CD54HC4015 (CERDIP) CD74HC4015 (PDIP, SOIC) TOP VIEW



Functional Diagram



TRUTH TABLE

	INPUTS			OUTPUTS						
СР	D	R	Q ₀	Q ₁	Q ₂	Q_3				
1	I	L	L	q' ₀	q' ₁	q' ₂				
1	h	L	Н	q' ₀	q' ₁	q' ₂				
\downarrow	Х	L	q'o	q' ₁	q' ₂	q'3				
Х	Х	Н	L	L	L	L				

H = High Voltage Level

h = High Voltage Level One Set-up Time Prior to the Low to High Clock Transition

L = Low Voltage Level

I = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition

X = Don't Care.

↑ = Low to High Clock Transition

 \downarrow = High to Low Clock Transition

 q'_n = Lower case letters indicate the state of the referenced output one set-up time prior to the Low to High clock transition.

CD54HC4015, CD74HC4015

Absolute Maximum Ratings Thermal Information θ_{JA} (°C/W) DC Supply Voltage, V_{CC}-0.5V to 7V Thermal Resistance (Typical, Note 1) DC Input Diode Current, I_{IK} M (SOIC) Package..... DC Output Diode Current, IOK For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$±20mA Maximum Storage Temperature Range-65°C to 150°C DC Output Source or Sink Current per Output Pin, IO Maximum Lead Temperature (Soldering 10s)......300°C (SOIC - Lead Tips Only) **Operating Conditions** Temperature Range, T_A -55°C to 125°C Supply Voltage Range, V_{CC} HC Types2V to 6V DC Input or Output Voltage, V_I, V_O 0V to V_{CC} Input Rise and Fall Time 4.5V...... 500ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		TEST CONDITIONS		v _{cc}	25°C			-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
High Level Input	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
Voltage CMOS Loads			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output	1		-	-	-	-	-	-	-	-	-	٧
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	٧
1.12 20000			-5.2	6	5.48	-	-	5.34	-	5.2	-	٧
Low Level Output	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	٧
Voltage CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	٧
000 2000			0.02	6	-	-	0.1	-	0.1	-	0.1	٧
Low Level Output	1		-	-	-	-	-	-	-	-	-	٧
Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	٧
TTE LOads			5.2	6	-	-	0.26	-	0.33	-	0.4	٧
Input Leakage Current	Ι _Ι	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μΑ
Quiescent Device Current	Icc	V _{CC} or GND	0	6	-	ı	8	-	80	-	160	μΑ

CD54HC4015, CD74HC4015

Prerequisite for Switching Specifications

			25	°С	-40°C T	O 85°C	-55°C T		
PARAMETER	SYMBOL	V _{CC} (V)	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Maximum Clock	f _{MAX}	2	6	-	5	-	4	-	MHz
Frequency		4.5	30	-	24	-	20	-	MHz
		6	35	-	28	-	24	-	MHz
Clock Pulse Width	t _W	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
MR Pulse Width	t _W	2	150	-	190	-	225	-	ns
		4.5	30	-	38	-	45	-	ns
		6	26	-	33	-	38	-	ns
MR Recovery Time	tREC	2	50	-	65	-	75	-	ns
		4.5	10	-	13	-	15	-	ns
		6	9	-	11	-	13	-	ns
Set-up Time,	tsul, tsuh	2	60	-	75	-	90	-	ns
Data-In to CP		4.5	12	-	15	-	18	-	ns
		6	10	-	13	-	15	-	ns
Hold Time,	tH	2	0	-	0	-	0	-	ns
Data-In to CP		4.5	0	-	0	-	0	-	ns
		6	0	-	0	-	0	-	ns

Switching Specifications Input t_r , $t_f = 6ns$

		TEST	V _{CC}		25°C		-40°C T	O 85°C	-55°C T	-55°C TO 125°C	
PARAMETER	SYMBOL	CONDITIONS	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Propagation Delay (Figure 1)	t _{PLH,}	C _L = 50pF	2	-	-	175	-	220	-	270	ns
Clock to Q _n	t _{PHL}		4.5	-	-	35	-	44	-	54	ns
		C _L =15pF	5	-	14	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	30	-	37	-	46	ns
MR to Q _n , (Clock High)	t _{PLH} ,	C _L = 50pF	2	-	-	275	-	345	-	415	ns
	t _{PHL}		4.5	-	-	55	-	64	-	83	ns
		C _L =15pF			25	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	47	-	54	-	71	ns
MR to Q _n , (Clock Low)	t _{PLH,} t _{PHL}	C _L = 50pF	2	-	-	325	-	400	-	490	ns
			4.5	-	-	65	-	81	-	98	ns
		C _L =15pF			25	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	55	-	69	-	83	ns
Output Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
(Figure 1)			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF
Maximum Clock Frequency	f _{MAX}	C _L =15pF	5	-	60	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 2, 3)	C _{PD}	C _L =15pF	5	-	43	-	-	-	-	-	pF

- 2. C_{PD} is used to determine the dynamic power consumption, per shift register.

 3. $P_D = V_{CC}^2 f_i + \sum C_L V_{CC}^2$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuit and Waveform

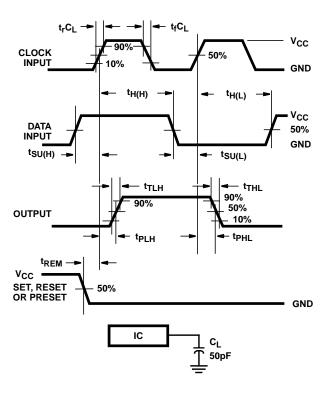


FIGURE 1. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS





5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-8995301EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
CD54HC4015F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD74HC4015E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC4015EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC4015M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4015ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4015MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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5-Sep-2011

OTHER QUALIFIED VERSIONS OF CD54HC4015, CD74HC4015:

● Catalog: CD74HC4015

Military: CD54HC4015

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE

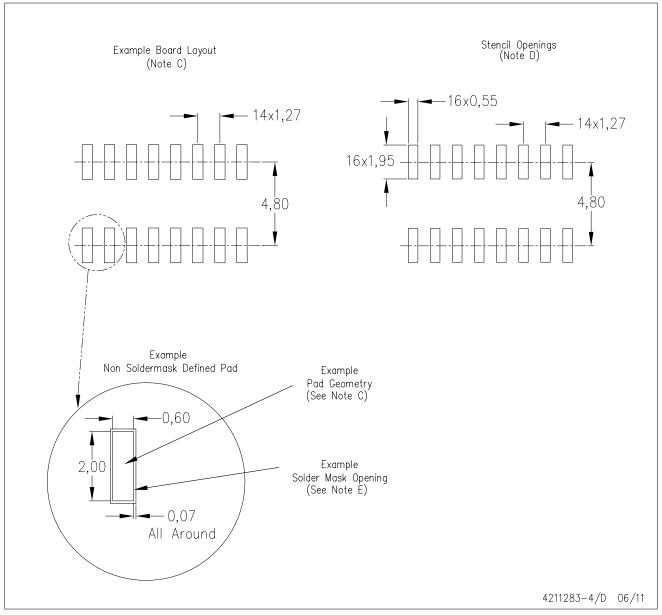


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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